



Data Sheet

π 120M/ π 121M/ π 122M

FEATURES

Ultra low power consumption (1Mbps):

0.58mA/Channel

High data rate: π 12xAxx: 600Mbps

π 12xExx: 200Mbps

π 12xMxx: 10Mbps

π 12xUxx: 150kbps

High common-mode transient immunity: 75 kV/ μ s typical

High robustness to radiated and conducted noise

Low propagation delay:

8 ns typical for 5 V operation

9 ns typical for 3.3 V operation

Isolation voltages:

π 12xx3x: AC 3000Vrms

π 12xx6x: AC 6000Vrms

High ESD rating:

ESDA/JEDEC JS-001-2017

Human body model (HBM) \pm 8kV, all pins

Safety and regulatory approvals (Pending):

UL certificate number: E494497

3000Vrms/6000Vrms for 1 minute per UL 1577

CSA Component Acceptance Notice 5A

VDE certificate number: 40047929

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12

$V_{IORM} = 707V$ peak/1200V peak

CQC certification per GB4943.1-2011

3 V to 5.5 V level translation

Wide temperature range: $-40^{\circ}C$ to $125^{\circ}C$

8/16-lead, RoHS-compliant, (W)SOIC package

APPLICATIONS

General-purpose multichannel isolation

Industrial field bus isolation

GENERAL DESCRIPTION

The π 1xxxx is a 2PaiSemi digital isolators product family that includes over hundreds of digital isolator products. By using matured standard semiconductor CMOS technology and 2PaiSEMI *iDivider* technology, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators.

Intelligent voltage divider technology (*iDivider* technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit voltage signal directly cross the isolator capacitor without signal modulation and demodulation.

The π 1xxxx isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide). The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. The fail-safe state is available in which the outputs transition to a preset state when the input power supply is not applied.

FUNCTIONAL BLOCK DIAGRAMS

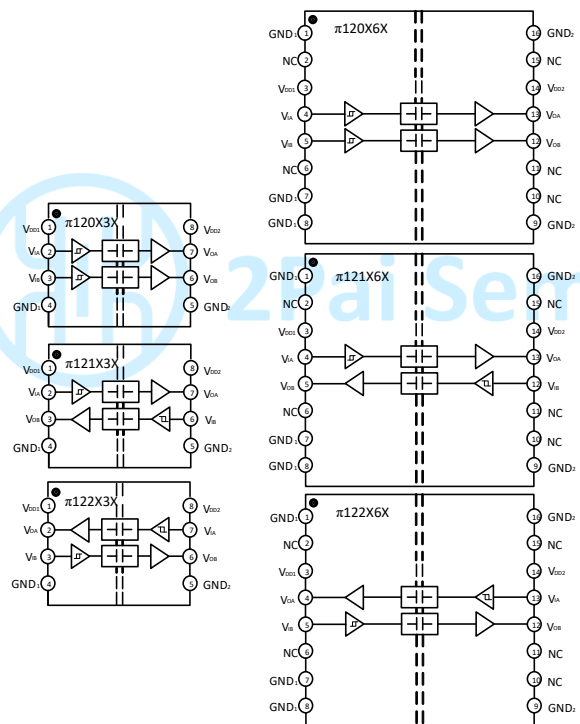


Figure1. π 120xxx/ π 121xxx/ π 122xxx functional Block Diagram

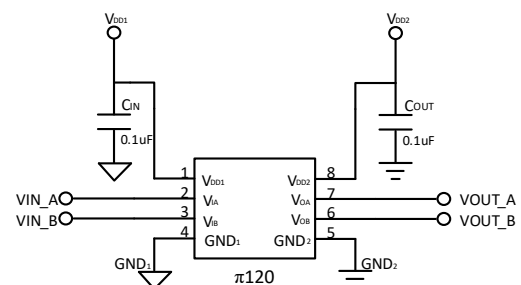


Figure2. π 120xxx Typical Application Circuit

Rev.1

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PIN CONFIGURATIONS AND FUNCTIONS

π 120M3x Pin Function Descriptions

| Pin No. | Name | Description |
|---------|------------------|---|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 2 | V _{IA} | Logic Input A. |
| 3 | V _{IB} | Logic Input B. |
| 4 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 5 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 6 | V _{OB} | Logic Output B. |
| 7 | V _{OA} | Logic Output A. |
| 8 | V _{DD2} | Supply Voltage for Isolator Side 2. |

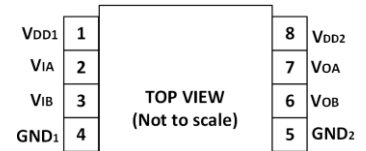


Figure3. π 120M3x Pin Configuration

π 121M3x Pin Function Descriptions

| Pin No. | Name | Description |
|---------|------------------|---|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 2 | V _{IA} | Logic Input A. |
| 3 | V _{OB} | Logic Output B. |
| 4 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 5 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 6 | V _{IB} | Logic Input B. |
| 7 | V _{OA} | Logic Output A. |
| 8 | V _{DD2} | Supply Voltage for Isolator Side 2. |

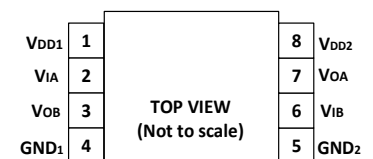


Figure4. π 121M3x Pin Configuration

π 122M3x Pin Function Descriptions

| Pin No. | Name | Description |
|---------|------------------|---|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 2 | V _{OA} | Logic Output A. |
| 3 | V _{IB} | Logic Input B. |
| 4 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 5 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 6 | V _{OB} | Logic Output B. |
| 7 | V _{IA} | Logic Input A. |
| 8 | V _{DD2} | Supply Voltage for Isolator Side 2. |

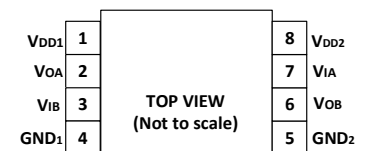


Figure5. π 122M3x Pin Configuration

π 120M6x Pin Function Descriptions

| Pin No. | Name | Description |
|---------|------------------|---|
| 1 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 2 | NC | No connect. |
| 3 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 4 | V _{IA} | Logic Input A. |
| 5 | V _{IB} | Logic Input B. |
| 6 | NC | No Connect. |
| 7 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 8 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 9 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |

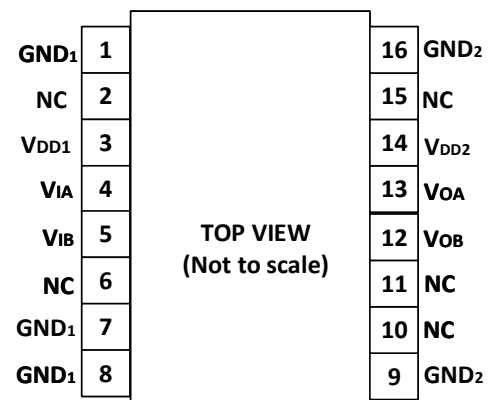


Figure6. π 120M6x Pin Configuration

| | | |
|----|------------------|---|
| 10 | NC | No Connect. |
| 11 | NC | No Connect. |
| 12 | V _{OB} | Logic Output B. |
| 13 | V _{OA} | Logic Output A. |
| 14 | V _{DD2} | Supply Voltage for Isolator Side 2. |
| 15 | NC | No Connect. |
| 16 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |

π 121M6x Pin Function Descriptions

| Pin No. | Name | Description |
|---------|------------------|---|
| 1 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 2 | NC | No Connect. |
| 3 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 4 | V _{IA} | Logic Input A. |
| 5 | V _{OB} | Logic Output B. |
| 6 | NC | No Connect. |
| 7 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 8 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 9 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 10 | NC | No Connect. |
| 11 | NC | No Connect. |
| 12 | V _{IB} | Logic Input B. |
| 13 | V _{OA} | Logic Output A. |
| 14 | V _{DD2} | Supply Voltage for Isolator Side 2. |
| 15 | NC | No Connect. |
| 16 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |

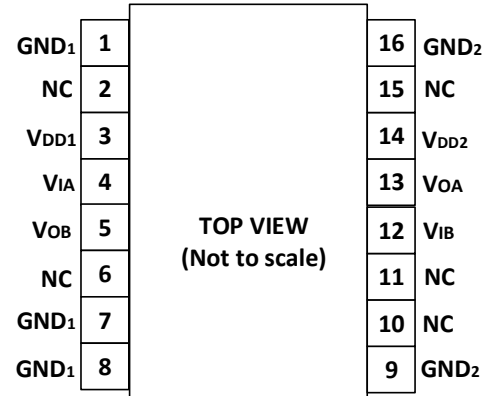


Figure7. π 121M6x Pin Configuration

π 122M6x Pin Function Descriptions

| Pin No. | Name | Description |
|---------|------------------|---|
| 1 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 2 | NC | No Connect. |
| 3 | V _{DD1} | Supply Voltage for Isolator Side 1. |
| 4 | V _{OA} | Logic Output A. |
| 5 | V _{IB} | Logic Input B. |
| 6 | NC | No Connect. |
| 7 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 8 | GND ₁ | Ground 1. This pin is the ground reference for Isolator Side 1. |
| 9 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |
| 10 | NC | No Connect. |
| 11 | NC | No Connect. |
| 12 | V _{OB} | Logic Output B. |
| 13 | V _{IA} | Logic Input A. |
| 14 | V _{DD2} | Supply Voltage for Isolator Side 2. |
| 15 | NC | No Connect. |
| 16 | GND ₂ | Ground 2. This pin is the ground reference for Isolator Side 2. |

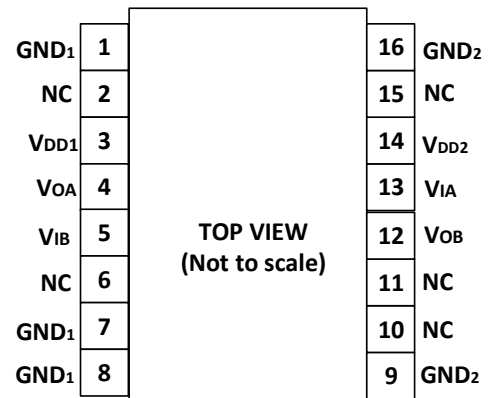


Figure8. π 122M6x Pin Configuration

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1. Absolute Maximum Ratings⁴

| Parameter | Rating |
|--|--|
| Supply Voltages ($V_{DD1-GND1}$, $V_{DD2-GND2}$) | -0.5 V to +7.0 V |
| Input Voltages (V_{IA} , V_{IB}) ¹ | -0.5 V to $V_{DDx} + 0.5$ V |
| Output Voltages (V_{OA} , V_{OB}) ¹ | -0.5 V to $V_{DDx} + 0.5$ V |
| Average Output Current per Pin ² Side 1 Output Current (I_{O1}) | -10 mA to +10 mA |
| Average Output Current per Pin ² Side 2 Output Current (I_{O2}) | -10 mA to +10 mA |
| Common-Mode Transients Immunity ³ | -150 kV/ μs to +150 kV/ μs |
| Storage Temperature (T_{ST}) Range | -65°C to +150°C |
| Ambient Operating Temperature (T_A) Range | -40°C to +125°C |

Notes:

¹ V_{DDx} is the side voltage power supply V_{DD} , where $x = 1$ or 2 .

² See Figure9 for the maximum rated current values for various temperatures.

³ See Figure19 for Common-mode transient immunity (CMTI) measurement.

⁴ Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

RECOMMENDED OPERATING CONDITIONS

Table 2. Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------------|------------------------|------------------------------|-----|------------------------------|------|
| Supply Voltage | V_{DDx} ¹ | 3 | | 5.5 | V |
| High Level Input Signal Voltage | V_{IH} | $0.7 * V_{DDx}$ ¹ | | V_{DDx} ¹ | V |
| Low Level Input Signal Voltage | V_{IL} | 0 | | $0.3 * V_{DDx}$ ¹ | V |
| High Level Output Current | I_{OH} | -6 | | | mA |
| Low Level Output Current | I_{OL} | | | 6 | mA |
| Maximum Data Rate | | 0 | | 10 | Mbps |
| Junction Temperature | T_J | -40 | | 150 | °C |
| Ambient Operating Temperature | T_A | -40 | | 125 | °C |

Notes:

¹ V_{DDx} is the side voltage power supply V_{DD} , where $x = 1$ or 2 .

Truth Tables

Table 3. $\pi 120xxx/\pi 121xxx/\pi 122xxx$ Truth Table

| V_{ix} Input ¹ | V_{DD1} State ¹ | V_{DD0} State ¹ | Default Low V_{ox} Output ¹ | Default High V_{ox} Output ¹ | Test Conditions /Comments |
|-----------------------------|------------------------------|------------------------------|---|--|------------------------------|
| Low | Powered ² | Powered ² | Low | Low | Normal operation |
| High | Powered ² | Powered ² | High | High | Normal operation |
| Open | Powered ² | Powered ² | Low | High | Default output |
| Don't Care ⁴ | Unpowered ³ | Powered ² | Low | High | Default output ⁵ |
| Don't Care ⁴ | Powered ² | Unpowered ³ | High Impedance | High Impedance | |

Notes:

¹ V_{ix}/V_{ox} are the input/output signals of a given channel (A or B). V_{DD1}/V_{DD0} are the supply voltages on the input/output signal sides of this given channel.

² Powered means $V_{DDx} \geq 2.9$ V

³ Unpowered means $V_{DDx} < 2.3$ V

⁴ Input signal (V_{ix}) must be in a low state to avoid powering the given V_{DD1} through its ESD protection circuitry.

⁵ If the V_{DD1} goes into unpowered status, the channel outputs the default logic signal after around 1 μ s. If the V_{DD1} goes into powered status, the channel outputs the input status logic signal after around 1 μ s.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Table 4. Switching Specifications

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$ or $5V_{DC} \pm 10\%$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----------------------|-----|---------|------|------------------------|---|
| Minimum Pulse Width | PW | | | 100 | ns | Within pulse width distortion (PWD) limit |
| Maximum Data Rate | | 10 | | | Mbps | Within PWD limit |
| Propagation Delay Time ^{1,4} | t_{pHL} , t_{pLH} | 5.5 | 8 | 12.5 | ns | The different time between 50% input signal to 50% output signal 50% @ $5V_{DC}$ supply |
| | | 6.5 | 9 | 13.5 | ns | @ $3.3V_{DC}$ supply |
| Pulse Width Distortion ⁴ | PWD | 0 | 0.3 | 0.8 | ns | The max different time between t_{pHL} and t_{pLH} @ $5V_{DC}$ supply. And The value is $ t_{pHL} - t_{pLH} $ |
| | | 0 | 0.3 | 0.8 | ns | @ $3.3V_{DC}$ supply |
| Part to Part Propagation Delay Skew ⁴ | t_{PSK} | | | 1 | ns | The max different propagation delay time between any two devices at the same temperature, load and voltage @ $5V_{DC}$ supply |
| | | | | 1 | ns | @ $3.3V_{DC}$ supply |
| Channel to Channel Propagation Delay Skew ⁴ | t_{CSK} | | 0 | 1 | ns | The max amount propagation delay time differs between any two output channels in the single device @ $5V_{DC}$ supply. |
| | | | 0 | 0.8 | ns | @ $3.3V_{DC}$ supply |
| Output Signal Rise/Fall Time ⁴ | t_r/t_f | | 1.5 | | ns | 10% to 90% signal terminated 50Ω , See figure15. |
| Dynamic Input Supply Current per Channel | $I_{DDI(D)}$ | | 9 | | μA /Mbps | Inputs switching, 50% duty cycle square wave, $CL = 0$ pF @ $5V_{DC}$ Supply |
| Dynamic Output Supply Current per Channel | $I_{DDO(D)}$ | | 38 | | μA /Mbps | Inputs switching, 50% duty cycle square wave, $CL = 0$ pF @ $5V_{DC}$ Supply |
| Dynamic Input Supply Current per Channel | $I_{DDI(D)}$ | | 5 | | μA /Mbps | Inputs switching, 50% duty cycle square wave, $CL = 0$ pF @ $3.3V_{DC}$ Supply |
| Dynamic Output Supply Current per Channel | $I_{DDO(D)}$ | | 23 | | μA /Mbps | Inputs switching, 50% duty cycle square wave, $CL = 0$ pF @ $3.3V_{DC}$ Supply |
| Common-Mode Transient Immunity ³ | CMTI | | 75 | | kV/ μs | $V_{IN} = V_{DDx}^2$ or 0V, $V_{CM} = 1000$ V. |
| Jitter | | | 120 | | ps p-p | See the Jitter Measurement section |
| | | | 20 | | ps rms | See the Jitter Measurement section |
| ESD (HBM - Human body model) | ESD | | ± 8 | | kV | All pins |

Notes:

¹ t_{pLH} = low-to-high propagation delay time, t_{pHL} = high-to-low propagation delay time. See figure 16.

² V_{DDx} is the side voltage power supply V_{DD} , where $x = 1$ or 2 .

³ See Figure19 for Common-mode transient immunity (CMTI) measurement.

⁴ Output Signal Terminated 50Ω .

Table 5. DC Specifications
 $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$ or $5V_{DC} \pm 10\%$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|--------------|-------------------|-------------------|-------------------|---------------|--|
| Rising Input Signal Voltage Threshold | V_{IT+} | | $0.6 * V_{DDx}^1$ | $0.7 * V_{DDx}^1$ | V | |
| Falling Input Signal Voltage Threshold | V_{IT-} | $0.3 * V_{DDx}^1$ | $0.4 * V_{DDx}^1$ | | V | |
| High Level Output Voltage | V_{OH}^1 | $V_{DDx} - 0.1$ | V_{DDx} | | V | -20 μA output current |
| | | $V_{DDx} - 0.2$ | $V_{DDx} - 0.1$ | | V | -2 mA output current |
| Low Level Output Voltage | V_{OL} | | 0 | 0.1 | V | 20 μA output current |
| | | | 0.1 | 0.2 | V | 2 mA output current |
| Input Current per Signal Channel | I_{IN} | -10 | 0.5 | 10 | μA | $0\text{ V} \leq \text{Signal voltage} \leq V_{DDx}^1$ |
| V_{DDx}^1 Undervoltage Rising Threshold | V_{DDxUV+} | 2.45 | 2.65 | 2.9 | V | |
| V_{DDx}^1 Undervoltage Falling Threshold | V_{DDxUV-} | 2.3 | 2.5 | 2.75 | V | |
| V_{DDx}^1 Hysteresis | V_{DDxUVH} | | 0.15 | | V | |

Notes:

¹ V_{DDx} is the side voltage power supply V_{DD} , where $x = 1$ or 2 .**Table 6. Quiescent Supply Current**
 $V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$ or $5V_{DC} \pm 10\%$, $T_A = 25^\circ\text{C}$, $C_L = 0\text{ pF}$, unless otherwise noted.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions | |
|---|----------------------|---------------|-----|------|---------------|-----------------|-------------------|
| $\pi 120\text{Mxx}$ Quiescent Supply Current @ $5V_{DC}$ Supply | $I_{DD1} (Q)$ | 64 | 80 | 104 | μA | 0V Input signal | |
| | $I_{DD2} (Q)$ | 781 | 976 | 1269 | μA | 0V Input signal | |
| | $I_{DD1} (Q)$ | 158 | 197 | 256 | μA | 5V Input signal | |
| | $I_{DD2} (Q)$ | 738 | 923 | 1200 | μA | 5V Input signal | |
| | @ $3.3V_{DC}$ Supply | $I_{DD1} (Q)$ | 63 | 79 | 103 | μA | 0V Input signal |
| | | $I_{DD2} (Q)$ | 772 | 965 | 1255 | μA | 0V Input signal |
| | | $I_{DD1} (Q)$ | 116 | 145 | 189 | μA | 3.3V Input signal |
| | | $I_{DD2} (Q)$ | 709 | 886 | 1152 | μA | 3.3V Input signal |
| $\pi 121\text{Mxx}$ Quiescent Supply Current @ $5V_{DC}$ Supply | $I_{DD1} (Q)$ | 419 | 524 | 681 | μA | 0V Input signal | |
| | $I_{DD2} (Q)$ | 419 | 524 | 681 | μA | 0V Input signal | |
| | $I_{DD1} (Q)$ | 436 | 545 | 709 | μA | 5V Input signal | |
| | $I_{DD2} (Q)$ | 436 | 545 | 709 | μA | 5V Input signal | |
| | @ $3.3V_{DC}$ Supply | $I_{DD1} (Q)$ | 414 | 518 | 673 | μA | 0V Input signal |
| | | $I_{DD2} (Q)$ | 414 | 518 | 673 | μA | 0V Input signal |
| | | $I_{DD1} (Q)$ | 408 | 510 | 663 | μA | 3.3V Input signal |
| | | $I_{DD2} (Q)$ | 408 | 510 | 663 | μA | 3.3V Input signal |
| $\pi 122\text{Mxx}$ Quiescent Supply Current @ $5V_{DC}$ Supply | $I_{DD1} (Q)$ | 419 | 524 | 681 | μA | 0V Input signal | |
| | $I_{DD2} (Q)$ | 419 | 524 | 681 | μA | 0V Input signal | |
| | $I_{DD1} (Q)$ | 436 | 545 | 709 | μA | 5V Input signal | |
| | $I_{DD2} (Q)$ | 436 | 545 | 709 | μA | 5V Input signal | |
| | @ $3.3V_{DC}$ Supply | $I_{DD1} (Q)$ | 414 | 518 | 673 | μA | 0V Input signal |
| | | $I_{DD2} (Q)$ | 414 | 518 | 673 | μA | 0V Input signal |

| | | | | | |
|---------------|-----|-----|-----|---------|-------------------|
| I_{DD1} (Q) | 408 | 510 | 663 | μ A | 3.3V Input signal |
| I_{DD2} (Q) | 408 | 510 | 663 | μ A | 3.3V Input signal |

Table 7. Total Supply Current vs. Data Throughput ($C_L = 0$ pF)

$V_{DD1} - V_{GND1} = V_{DD2} - V_{GND2} = 3.3V_{DC} \pm 10\%$ or $5V_{DC} \pm 10\%$, $T_A = 25^\circ\text{C}$, $C_L = 0$ pF, unless otherwise noted.

| Parameter | Symbol | 150 Kbps | | | 1 Mbps | | | 10 Mbps | | | Unit | |
|---|---------------|-----------|------|------|--------|------|------|---------|------|------|------|----|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | | |
| π 120Mxx Supply Current @ $5V_{DC}$ | I_{DD1} | | 0.14 | 0.21 | | 0.15 | 0.22 | | 0.24 | 0.36 | mA | |
| | I_{DD2} | | 0.95 | 1.43 | | 1.02 | 1.52 | | 1.76 | 2.63 | mA | |
| | @ $3.3V_{DC}$ | I_{DD1} | | 0.11 | 0.17 | | 0.12 | 0.17 | | 0.18 | 0.27 | mA |
| | | I_{DD2} | | 0.93 | 1.40 | | 0.97 | 1.46 | | 1.43 | 2.14 | mA |
| π 121Mxx Supply Current @ $5V_{DC}$ | I_{DD1} | | 0.54 | 0.81 | | 0.58 | 0.86 | | 0.97 | 1.46 | mA | |
| | I_{DD2} | | 0.54 | 0.81 | | 0.58 | 0.86 | | 0.97 | 1.46 | mA | |
| | @ $3.3V_{DC}$ | I_{DD1} | | 0.52 | 0.78 | | 0.54 | 0.81 | | 0.77 | 1.16 | mA |
| | | I_{DD2} | | 0.52 | 0.78 | | 0.54 | 0.81 | | 0.77 | 1.16 | mA |
| π 122Mxx Supply Current @ $5V_{DC}$ | I_{DD1} | | 0.54 | 0.81 | | 0.58 | 0.86 | | 0.97 | 1.60 | mA | |
| | I_{DD2} | | 0.54 | 0.81 | | 0.58 | 0.86 | | 0.97 | 1.60 | mA | |
| | @ $3.3V_{DC}$ | I_{DD1} | | 0.52 | 0.78 | | 0.54 | 0.81 | | 0.77 | 1.20 | mA |
| | | I_{DD2} | | 0.52 | 0.78 | | 0.54 | 0.81 | | 0.77 | 1.20 | mA |

INSULATION AND SAFETY RELATED SPECIFICATIONS**Table 8. Insulation Specifications**

| Parameter | Symbol | Value | | Unit | Test Conditions/Comments |
|--|---------|--------------|--------------|-------------|--|
| | | π 12xM3x | π 12xM6x | | |
| Rated Dielectric Insulation Voltage | | 3000 | 6000 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance) | L (CLR) | 4 | 8 | mm min | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L (CRP) | 4 | 8 | mm min | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 11 | 21 | μ m min | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | >400 | V | DIN IEC 112/VDE 0303 Part 1 |
| Material Group | | II | II | | Material Group (DIN VDE 0110, 1/89, Table 1) |

PACKAGE CHARACTERISTICS**Table 9. Package Characteristics**

| Parameter | Symbol | Typical Value | | Unit | Test Conditions/Comments |
|--|---------------|---------------|--------------|---------------------------|---|
| | | π 12xM3x | π 12xM6x | | |
| Resistance (Input to Output) ¹ | R_{I-O} | 10^{11} | 10^{11} | Ω | |
| Capacitance (Input to Output) ¹ | C_{I-O} | 0.6 | 0.6 | pF | @1MHz |
| Input Capacitance ² | C_I | 3 | 3 | pF | @1MHz |
| IC Junction to Ambient Thermal Resistance | θ_{JA} | 100 | 45 | $^\circ\text{C}/\text{W}$ | Thermocouple located at center of package underside |

Notes:

¹The device is considered a 2-terminal device; SOIC-8 Pin 1 - Pin 4 (WSOIC-16 Pin 1-Pin8) are shorted together as the one terminal, and SOIC-8 Pin 5 - Pin 8 (WSOIC-16 Pin 9-Pin16) are shorted together as the other terminal.

²Testing from the input signal pin to ground.

REGULATORY INFORMATION

See Table 10 and the Insulation Lifetime section for details regarding recommended maximum working voltages for specific cross isolation waveforms and insulation levels.

Table 10. Regulatory

| Regulatory | π 12xM3x | π 12xM6x |
|------------|---|--|
| UL | Recognized under UL 1577 Component Recognition Program ¹ Single Protection, 3000 V rms Isolation Voltage File (E494497) | Recognized under UL 1577 Component Recognition Program ¹ Single Protection, 6000V rms Isolation Voltage File (pending) |
| CSA | Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 500 V rms (707 V peak) Reinforced insulation at 250 V rms (353 V peak) File (pending) | Approved under CSA Component Acceptance Notice 5A CSA 60950-1-07+A1+A2 and IEC 60950-1, second edition, +A1+A2: Basic insulation at 845 V rms (1200 V peak) Reinforced insulation at 422 V rms (600 V peak) File (pending) |
| VDE | DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ² Basic insulation, $V_{IORM} = 707$ V peak, $V_{IOSM} = 4615$ V peak File (40047929) | DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 ² Basic insulation, $V_{IORM} = 1200$ V peak, $V_{IOSM} = 7000$ V peak File (pending) |
| CQC | Certified under CQC11-471543-2012 GB4943.1-2011 Basic insulation at 500 V rms (707 V peak) working voltage Reinforced insulation at 250 V rms (353 V peak) File (pending) | Certified under CQC11-471543-2012 GB4943.1-2011 Basic insulation at 845 V rms (1200 V peak) working voltage Reinforced insulation at 422 V rms (600 V peak) File (pending) |

Notes:

¹ In accordance with UL 1577, each π 120M3x/ π 121M3x/ π 122M3x is proof tested by applying an insulation test voltage ≥ 3600 V rms for 1 sec; each π 120M6x/ π 121M6x/ π 122M6x is proof tested by applying an insulation test voltage ≥ 7200 V rms for 1 sec

² In accordance with DIN V VDE V 0884-10, each π 120M3x/ π 121M3x/ π 122M3x is proof tested by applying an insulation test voltage ≥ 1326 V peak for 1 sec (partial discharge detection limit = 5 pC); each π 120M6x/ π 121M6x/ π 122M6x is proof tested by ≥ 2250 V peak for 1 sec. The * marking branded on the component designates DIN V VDE V 0884-10 approval.

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

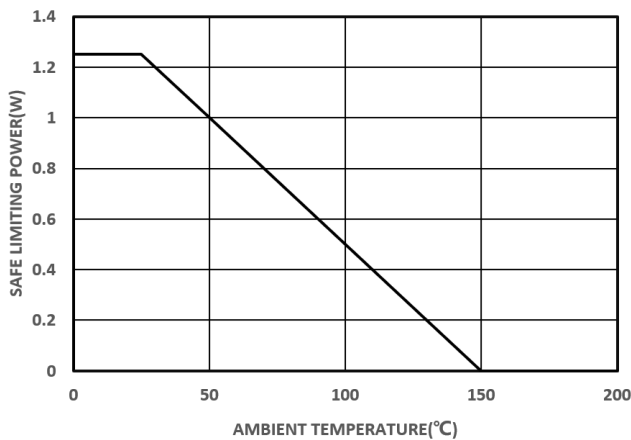
These isolators are suitable for reinforced electrical isolation only within the safety limit data. Protective circuits ensure the maintenance of the safety data. The * marking on packages denotes DIN V VDE V 0884-10 approval.

Table 11. VDE Insulation Characteristics

| Description | Test Conditions/Comments | Symbol | Characteristic | | Unit |
|--|--------------------------|--------|----------------|--------------|------|
| | | | π 12xM3x | π 12xM6x | |
| Installation Classification per DIN VDE 0110 | | | | | |
| For Rated Mains Voltage ≤ 150 V rms | | | I to IV | I to IV | |
| For Rated Mains Voltage ≤ 300 V rms | | | I to III | I to III | |
| For Rated Mains Voltage ≤ 400 V rms | | | I to III | I to III | |
| Climatic Classification | | | 40/105/21 | 40/105/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | 2 | |

| | | | | | |
|--|---|-------------|------------------|------------------|--------------|
| Maximum Working Insulation Voltage | | V_{IORM} | 707 | 1200 | V peak |
| Input to Output Test Voltage, Method B1 | $V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC | $V_{pd(m)}$ | 1326 | 2250 | V peak |
| Input to Output Test Voltage, Method A | | | | | |
| After Environmental Tests Subgroup 1 | $V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC | $V_{pd(m)}$ | 1061 | 1800 | V peak |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC | | 849 | 1440 | V peak |
| Highest Allowable Overvoltage | | V_{IOTM} | 4200 | 8500 | V peak |
| Surge Isolation Voltage Basic | Basic insulation, 1.2 μ s rise time, 50 μ s, 50% fall time | V_{IOSM} | 4615 | 7000 | V peak |
| Surge Isolation Voltage Reinforced | Reinforced insulation, 1.2 μ s rise time, 50 μ s, 50% fall time | V_{IOSM} | | | V peak |
| Safety Limiting Values | Maximum value allowed in the event of a failure (see Figure 9) | | | | |
| Maximum Junction Temperature | | T_S | 150 | 150 | $^{\circ}$ C |
| Total Power Dissipation at 25 $^{\circ}$ C | | P_S | 1.56 | 2.78 | W |
| Insulation Resistance at T_S | $V_{IO} = 800$ V | R_S | >10 ⁹ | >10 ⁹ | Ω |

π 12xM3x



π 12xM6x

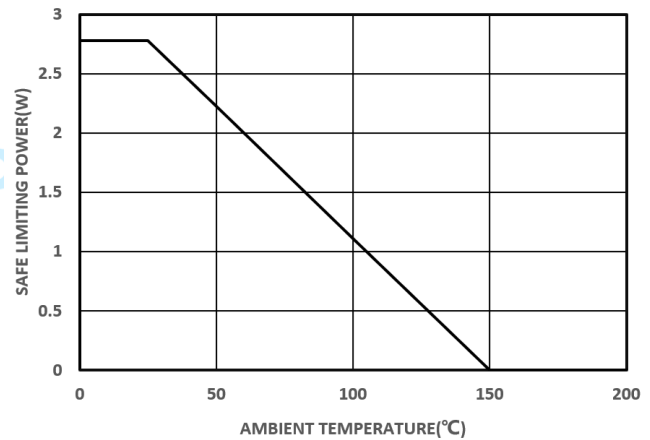


Figure9. Thermal Derating Curve, Dependence of Safety Limiting Values with Ambient Temperature per VDE

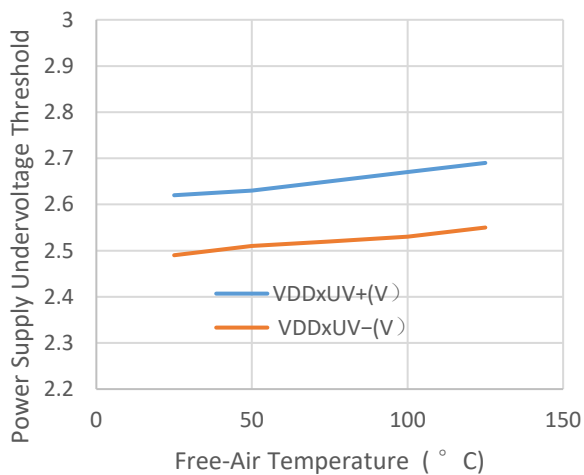


Figure10. UVLO vs. Free-Air Temperature

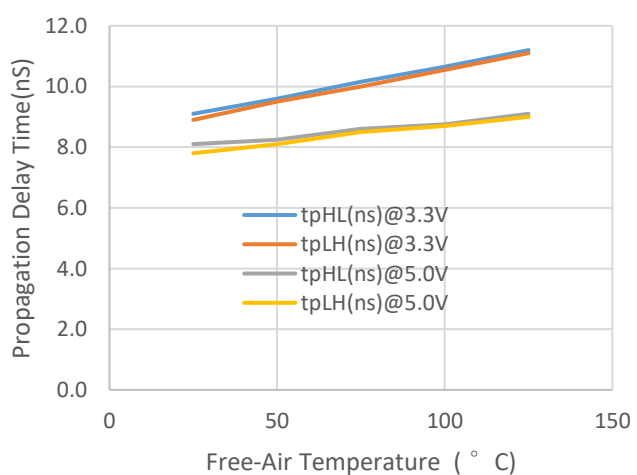


Figure11. Propagation Delay Time vs. Free-Air Temperature

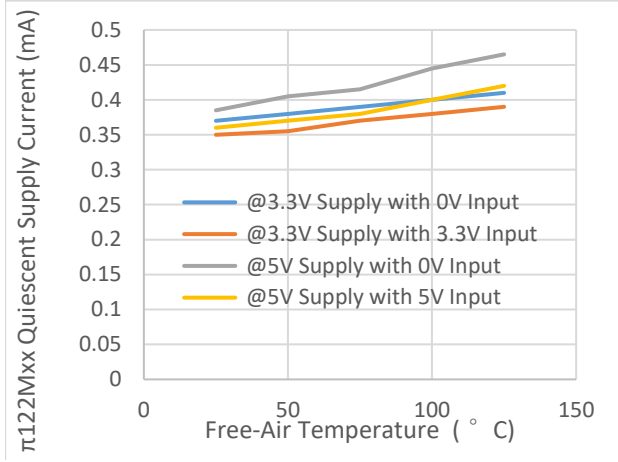


Figure12. π 121Mxx/ π 122Mxx Quiescent Supply Current vs. Free-Air Temperature

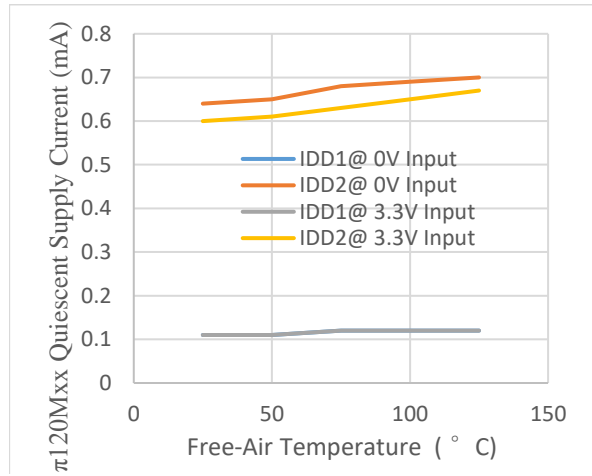


Figure13. π 120Mxx Quiescent Supply Current with 3.3V Supply vs. Free-Air Temperature

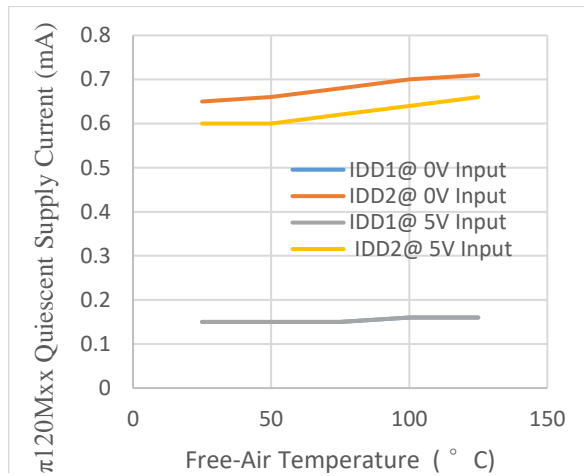


Figure14. π 120Mxx Quiescent Supply Current with 5V Supply vs. Free-Air Temperature

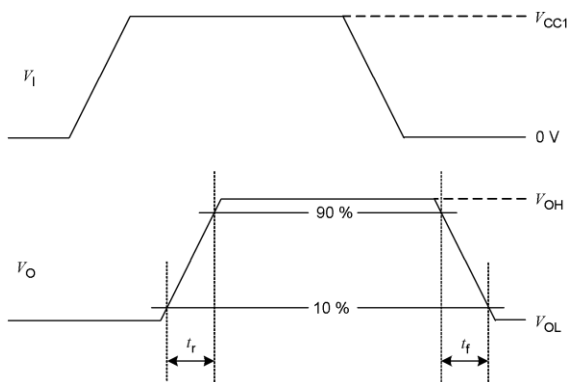


Figure15. Transition time waveform measurement

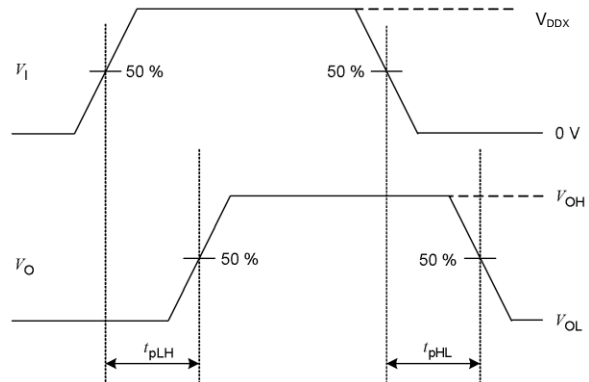


Figure16. Propagation delay time waveform measurement

APPLICATIONS INFORMATION

OVERVIEW

The $\pi 1xxxx$ are 2PaiSemi digital isolators product family based on 2PaiSEMI unique **iDivider** technology. Intelligent voltage **Divider** technology (**iDivider** technology) is a new generation digital isolator technology invented by 2PaiSEMI. It uses the principle of capacitor voltage divider to transmit signal directly cross the isolator capacitor without signal modulation and demodulation. Compare to the traditional Opto-couple technology, icoupler technology, OOK technology, **iDivider** is a more essential and concise isolation signal transmit technology which leads to greatly simplification on circuit design and therefore significantly improves device performance, such as lower power consumption, faster speed, enhanced anti-interference ability, lower noise.

By using matured standard semiconductor CMOS technology and the innovative **iDivider** design, these isolation components provide outstanding performance characteristics and reliability superior to alternatives such as optocoupler devices and other integrated isolators. The $\pi 1xxxx$ isolator data channels are independent and are available in a variety of configurations with a withstand voltage rating of 1.5 kV rms to 6.0 kV rms and the data rate from DC up to 600Mbps (see the Ordering Guide).

The $\pi 120Mxx/\pi 121Mxx/\pi 122Mxx$ are the outstanding 10 Mbps dual-channel digital isolators with the enhanced ESD capability. the devices transmit data across an isolation barrier by layers of silicon dioxide isolation.

The devices operate with the supply voltage on either side ranging from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic.

The $\pi 120Mxx/\pi 121Mxx/\pi 122Mxx$ have very low propagation delay and high speed. The input/output design techniques allow logic and supply voltages over a wide range from 3.0 V to 5.5 V, offering voltage translation of 3.3 V and 5 V logic. The architecture is designed for high common-mode transient immunity and high immunity to electrical noise and magnetic interference.

See the Ordering Guide for the model numbers that have the fail-safe output state of low or high.

PCB LAYOUT

The low-ESR ceramic bypass capacitors must be connected between V_{DD1} and GND_1 and between V_{DD2} and GND_2 . The bypass capacitors are placed on the PCB as close to the isolator device as possible. The recommended bypass capacitor value is between 0.1 μF and 10 μF . To enhance the robustness of a design,

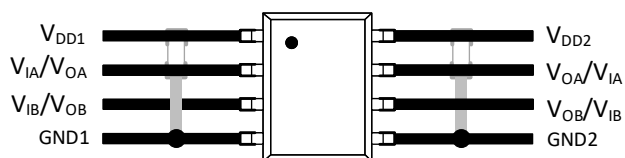


Figure17. Recommended Printed Circuit Board Layout

the user may also include resistors (50–300 Ω) in series with the inputs and outputs if the system is excessively noisy.

Avoid reducing the isolation capability, Keep the space underneath the isolator device free from metal such as planes, pads, traces and vias.

To minimize the impedance of the signal return loop, keep the solid ground plane directly underneath the high-speed signal path, the closer the better. The return path will couple between the nearest ground plane to the signal path. Keep suitable trace width for controlled impedance transmission lines interconnect.

To reduce the rise time degradation, keep the length of input/output signal traces as short as possible, and route low inductance loop for the signal path and It's return path.

JITTER MEASUREMENT

The eye diagram shown in the figure18 provides the jitter measurement result for the $\pi 120Mxx/\pi 121Mxx/\pi 122Mxx$. The Keysight 81160A pulse function arbitrary generator works as the data source for the $\pi 120Mxx/\pi 121Mxx/\pi 122Mxx$, which generates 10Mbps pseudo random bit sequence (PRBS). The Keysight DSOS104A digital storage oscilloscope captures the $\pi 120Mxx/\pi 121Mxx/\pi 122Mxx$ output waveform and recovers the eye diagram with the SDA jitter tools and eye diagram analysis tools. The result shows a typical measurement 120ps p-p jitter.

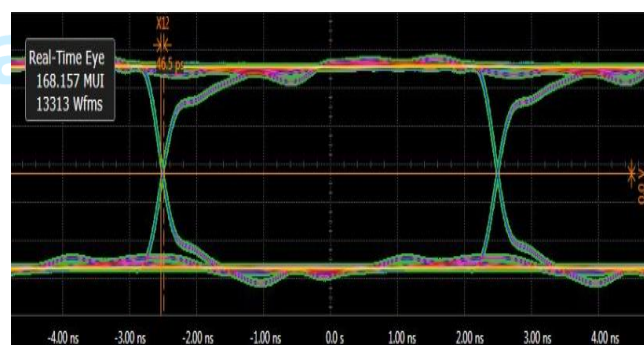


Figure18. $\pi 120Mxx/\pi 121Mxx/\pi 122Mxx$ Eye Diagram

CMTI MEASUREMENT

To measure the Common-Mode Transient Immunity (CMTI) of $\pi 1xxxx$ isolator under specified common-mode pulse magnitude (V_{CM}) and specified slew rate of the common-mode pulse (dV_{CM}/dt) and other specified test or ambient conditions, The

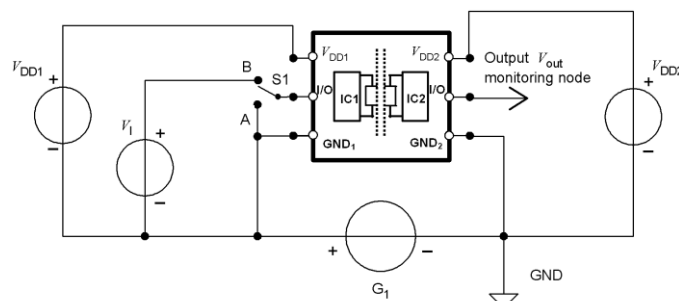
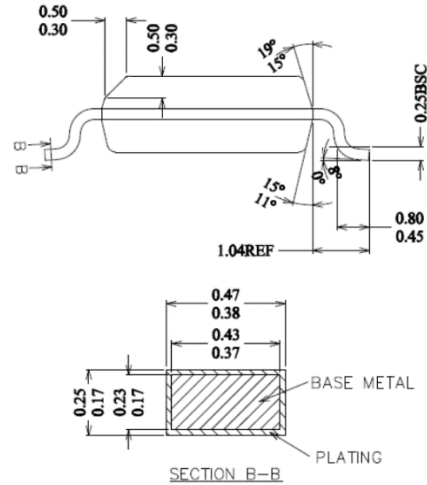
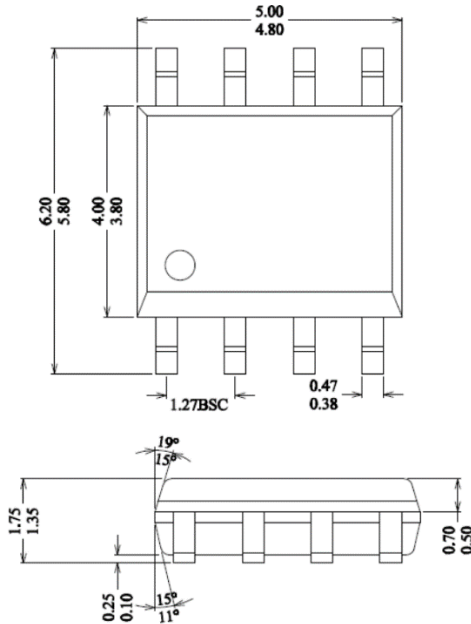


Figure19. Common-mode transient immunity (CMTI) measurement

common-mode pulse generator (G_1) will be capable of providing fast rising and falling pulses of specified magnitude and duration of the common-mode pulse (V_{CM}) and the maximum common-mode slew rates (dV_{CM}/dt) can be applied to π 1xxxxx isolator

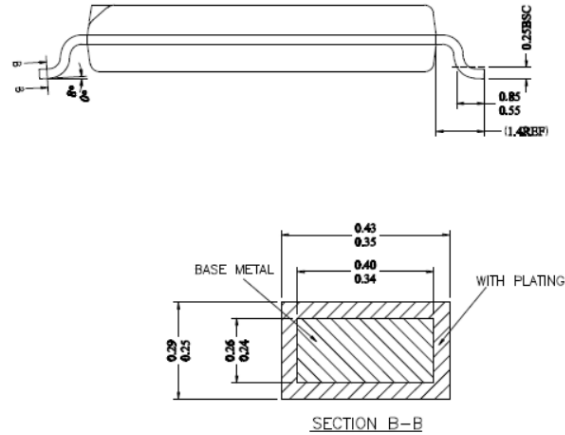
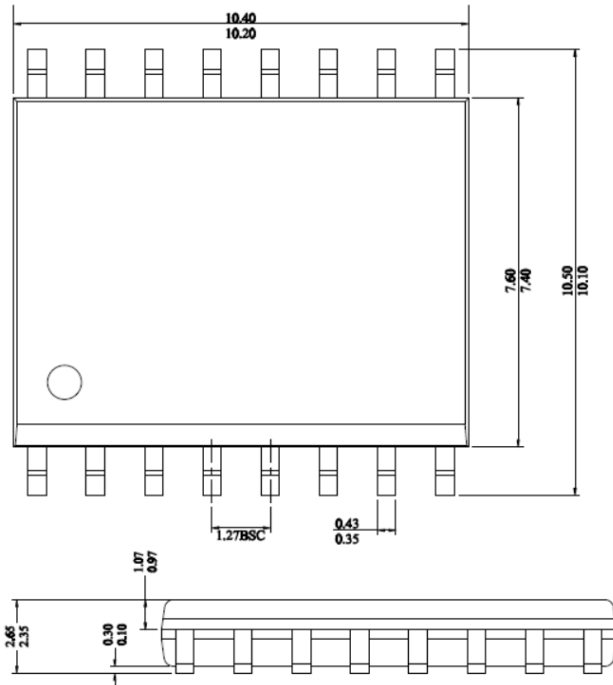
coupler under measurement. The common-mode pulse is applied between one side ground GND1 and the other side ground GND2 of π 1xxxxx isolator and shall be capable of providing positive transients as well as negative transients.

OUTLINE DIMENSIONS



NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MS-012 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSION.

Figure20. 8-Lead Standard Small Outline Package [8-Lead SOIC_N]

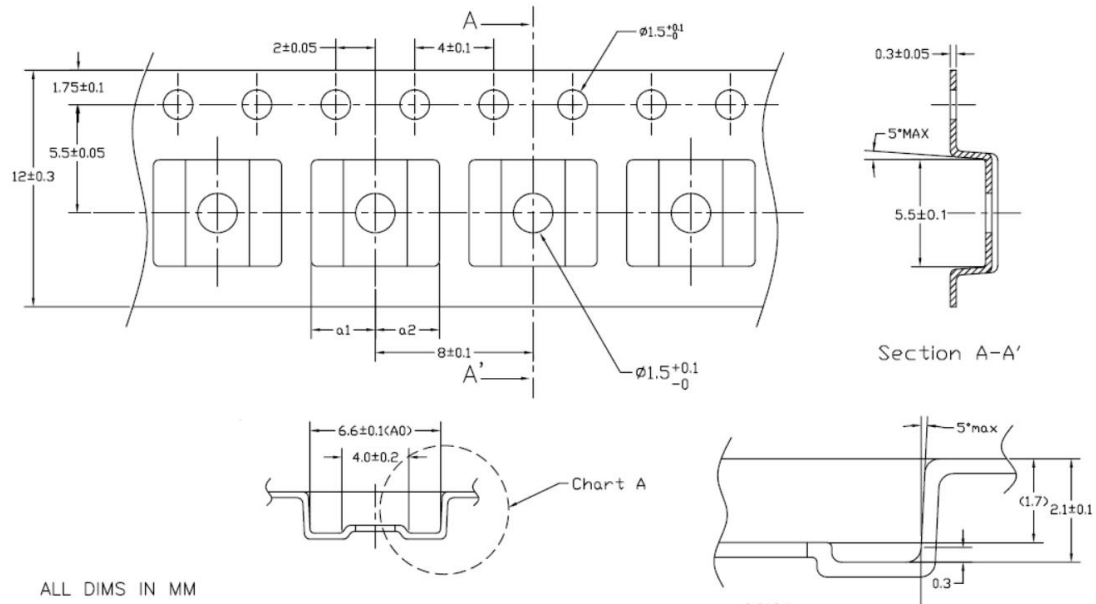


NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS-013 AA
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

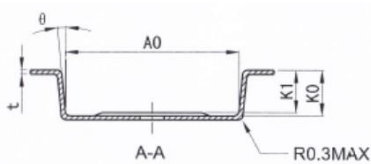
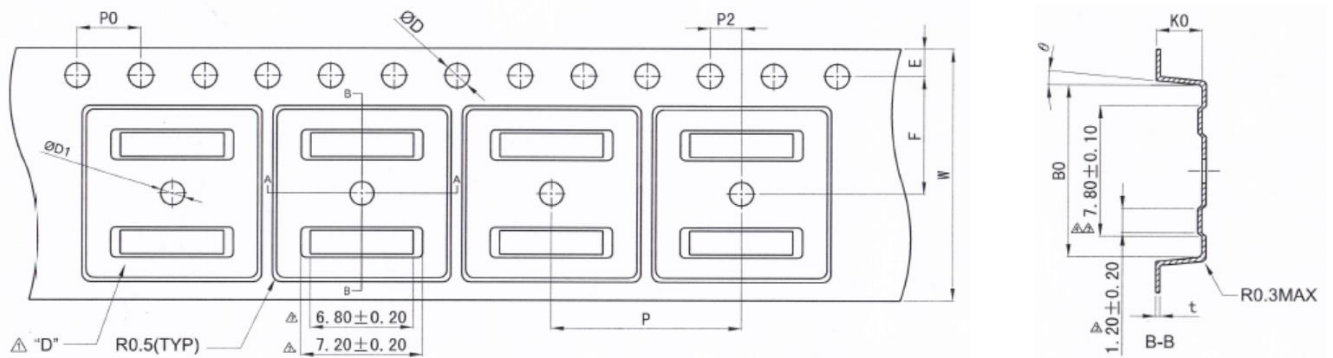
Figure21. 16-Lead Wide Body Outline Package [16-Lead SOIC_W]

REEL INFORMATION

8-Lead SOIC_N



16-Lead SOIC_W



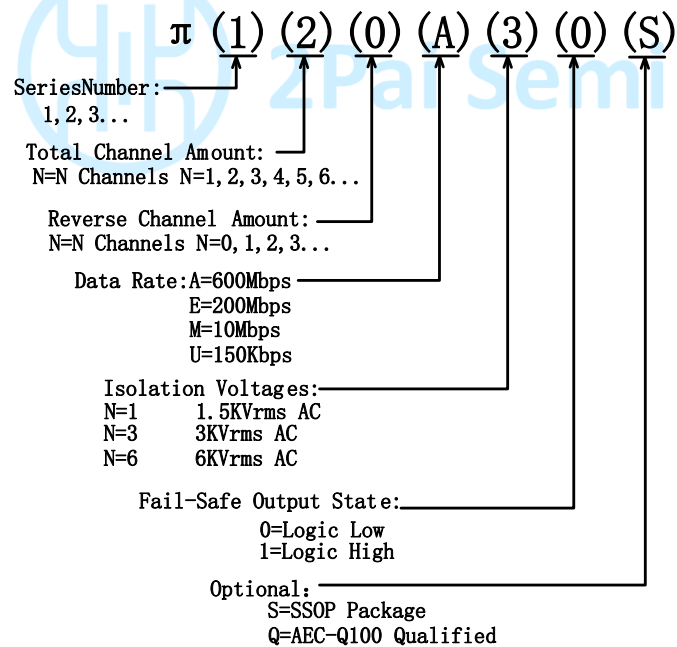
| Items | Size(mm) |
|-------|------------|
| E | 1.75±0.10 |
| F | 7.50±0.05 |
| P2 | 2.00±0.05 |
| D | 1.55±0.05 |
| D1 | 1.5±0.10 |
| P0 | 4.00±0.10 |
| 10P0 | 40.00±0.20 |

| Items | Size(mm) |
|-------|------------|
| W | 16.00±0.30 |
| P | 12.00±0.10 |
| A0 | 10.90±0.10 |
| B0 | 10.80±0.10 |
| K0 | 3.00±0.10 |
| t | 0.30±0.05 |
| K1 | 2.70±0.10 |
| θ | 5° TYP |

ORDERING GUIDE

| Model Name | | Temperature Range | No. of Inputs, V _{DD1} Side | No. of Inputs, V _{DD2} Side | Withstand Voltage Rating (kV rms) | Fail-Safe Output State | Package Description | Package Option | Quantity |
|--------------|-----------|-------------------|--------------------------------------|--------------------------------------|-----------------------------------|------------------------|---------------------|----------------|---------------|
| π 120M31 | Pai120M31 | -40°C to +125°C | 2 | 0 | 3 | High | 8-Lead SOIC_N | S-8-N | 4000 per reel |
| π 120M30 | Pai120M30 | -40°C to +125°C | 2 | 0 | 3 | Low | 8-Lead SOIC_N | S-8-N | 4000 per reel |
| π 121M31 | Pai121M31 | -40°C to +125°C | 1 | 1 | 3 | High | 8-Lead SOIC_N | S-8-N | 4000 per reel |
| π 121M30 | Pai121M30 | -40°C to +125°C | 1 | 1 | 3 | Low | 8-Lead SOIC_N | S-8-N | 4000 per reel |
| π 122M31 | Pai122M31 | -40°C to +125°C | 1 | 1 | 3 | High | 8-Lead SOIC_N | S-8-N | 4000 per reel |
| π 122M30 | Pai122M30 | -40°C to +125°C | 1 | 1 | 3 | Low | 8-Lead SOIC_N | S-8-N | 4000 per reel |
| π 120M61 | Pai120M61 | -40°C to +125°C | 2 | 0 | 6 | High | 16-Lead SOIC_W | S-16-W | 1500 per reel |
| π 120M60 | Pai120M60 | -40°C to +125°C | 2 | 0 | 6 | Low | 16-Lead SOIC_W | S-16-W | 1500 per reel |
| π 121M61 | Pai121M61 | -40°C to +125°C | 1 | 1 | 6 | High | 16-Lead SOIC_W | S-16-W | 1500 per reel |
| π 121M60 | Pai121M60 | -40°C to +125°C | 1 | 1 | 6 | Low | 16-Lead SOIC_W | S-16-W | 1500 per reel |
| π 122M61 | Pai122M61 | -40°C to +125°C | 1 | 1 | 6 | High | 16-Lead SOIC_W | S-16-W | 1500 per reel |
| π 122M60 | Pai122M60 | -40°C to +125°C | 1 | 1 | 6 | Low | 16-Lead SOIC_W | S-16-W | 1500 per reel |

PART NUMBER NAMED RULE



Notes:

Pai12xxxx is equals to π 12xxxx in the customer BOM

REVISION HISTORY

| Revision | Updated | Date | Page | Change Record |
|----------|---------|------------|----------------|---|
| 1 | Jason | 2018/09/17 | All | Initial version |
| 2 | Jason | 2018/11/28 | P11 | Changed the recommended bypass capacitor value from between 0.1 μ F and 1 μ F to between 0.1 μ F and 10 μ F. |
| 3 | Devin | 2019/09/08 | P1,P11,P13,P14 | <p>P1: Changed the address from 'Room 19307, Building 8, No.498, GuoShouJing Road' to 'Room 308-309, No.22, Boxia Road'; Add iDivider technology description in General Description.</p> <p>Changed propagation delay for 5V from 7.5ns to 8ns.</p> <p>Changed CMTI from 50KV/us to 75KV/us.</p> <p>Changed ESD(HBM) from 7KV to 8KV.</p> <p>P11: Add iDivider technology description in overview.</p> <p>P13: Updated 16-Lead SOIC_W reel drawing.</p> <p>P14: Add character 'S' and 'Q' in part number named rule; Changed the SOIC_W quantity from '1000 per reel' to '1500 per reel'.</p> |



2Pai Semi