12V/4A Standalone Switching Li+ Battery Charger

DESCRIPTION

The ETA6911 is a new generation of highly integrated synchronous switch-mode charger, featuring integrated synchronous FETs, high switching frequency and high charging efficiency. With ETA's proprietary current sense technology, by eliminating external sense resistor, it is capable of delivering charge current up to 4A. Furthermore, it has a very small footprint of 1.7mmx2mm and only requires small external components; therefore, it is ideal for extremely space-limited portable applications powered by 1-cell Li-ion or Li-polymer batteries.

ETA6911 also has a feature that in high impedance mode, the IC stops charging and consumes very low current from VBUS, thereby effectively reducing the standby power consumption of upstream power source.

The ETA6911's charge current and termination current can also be programmed by two separated external resistors. A NTC function is also provided to allow flexible thermal charging profiles. A STAT pin provides charging status indications.

ETA6911 is available in a small QFNFC1.7x2-20 and QFN4x4-24 package.

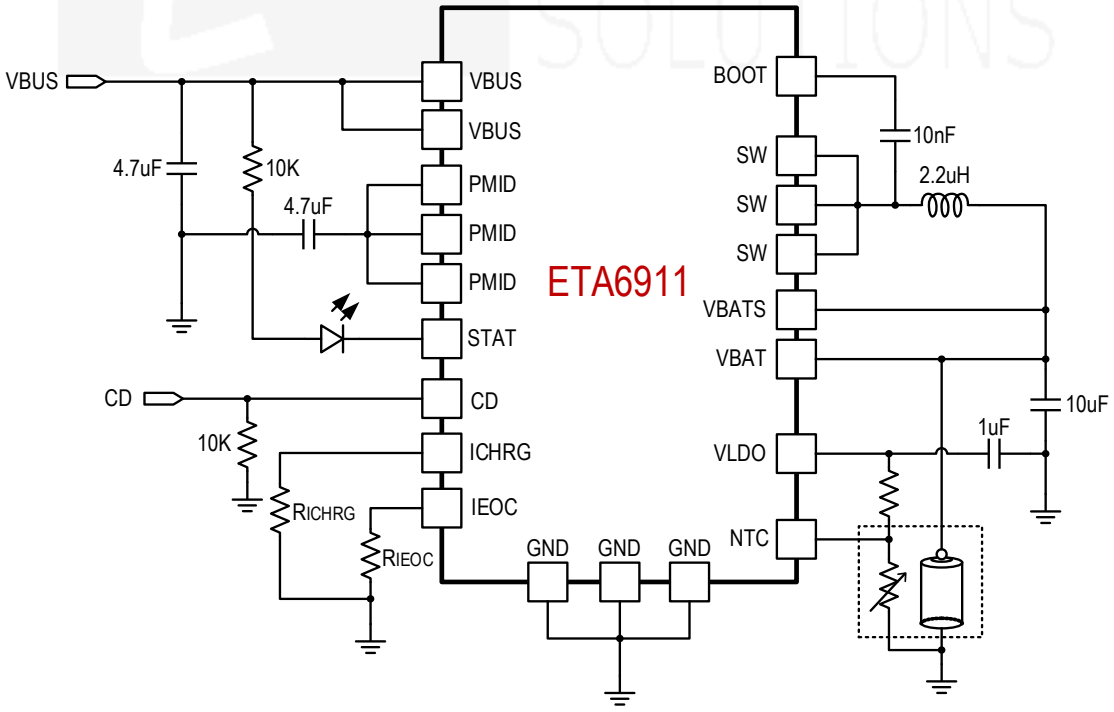
FEATURES

- Up to 4A Max Charging Current Switching Charger
- 93% Charging Efficiency at 5V Input 2A CC Current
- 12V Input Operating Voltage
- 20V Input Standoff Voltage
- 12V Battery Output Standoff Voltage
- No External Sense Resistor
- Integrate Linear Charger for Accurate Iterm Control
- Input DPPM
- Input Current Limiting
- Bad Adaptor Detection
- No-Battery Detection
- Status Output for Charging and Faults
- Input OVP
- Reverse Leakage Protection for Battery
- RoHS Compliant

APPLICATIONS

- Smart Phone
- Tablet, MID
- E-cigarette

TYPICAL APPLICATION

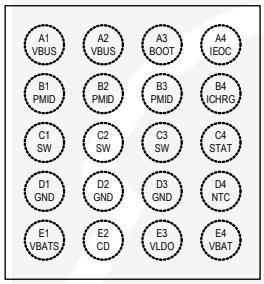


ORDERING INFORMATION

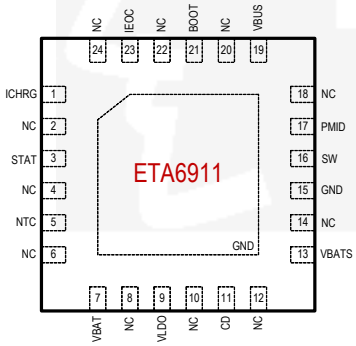
PART No.	PACKAGE	TOP MARK	Pcs/Reel
ETA6911FQHU	QFNFC1.7x2-20	BLYW	3000
ETA6911V435FQHU	QFNFC1.7x2-20	BVYW	3000
ETA6911Q4Y	QFN4x4-24	ETA6911 420 YWW2L	5000
ETA6911V435Q4Y	QFN4x4-24	ETA6911 435 YWW2L	5000

PIN CONFIGURATION

Top View



QFNFC1.7x2-20



QFN4x4-24

ABSOLUTE MAXIMUM RATINGS

(Note: Exceeding these limits may damage the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.)

VBUS, PMID, STAT to GND Voltage ..... –0.3V to 20V
SW to GND Voltage..... –0.3V to 20V
VBAT, VBATS to GND Voltage .....–0.3V to 13V
BOOT to SW Voltage..... –0.3V to 6V
All Other Pin to GND Voltage ..... –0.3V to 6V
SW, VBUS, VBAT, VBATS to GND current.. Internally limited
Operating Temperature Range .....–40°C to 85°C
Storage Temperature Range .....–55°C to 150°C
Thermal Resistance θ_{JA}
QFNFC1.7X2-20……..……35…..…….. °C/W
QFN4x4-24……..……35…..…….. °C/W
Lead Temperature (Soldering,10sec) .....260°C

ELECTRICAL CHARACTERISTICS

PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
INPUT CURRENTS					
VBUS Supply Current Control	V_{BUS}> V_{BUS_MIN}, PWM switching		10		mA
	V_{BUS}> V_{BUS_MIN}, PWM NOT switching			5	mA
	0°C < T_J<85°C, CD = 1		25		μA
	V_{BUS}> V_{BUS_MIN}, EOC Stage		200		μA
Battery Leakage Current in EOC	V_{BUS}> V_{BUS_MIN}, EOC Stage			5	μA
Battery Leakage Current when no VBUS	0°C < T_J< 85°C, V_{BAT} = 4.2V, High Impedance mode, V_{BUS}=0V		13		μA

PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
VOLTAGE REGULATION					
Battery Standoff Voltage				12	V
Battery Termination Voltage	ETA6911	4.179	4.2	4.221	V
	ETA6911V435	4.329	4.35	4.371	V
CURRENT REGULATION					
Fast Charge Current	$V_{PRECOND} \le V_{BAT} < V_{OREG}$, $V_{BUS} > V_{SLP}$, $R_{ICHARGE}$ = 50K		1500		mA
Precondition Charge Current	$V_{SHORT} \le V_{BAT} < V_{PRECOND}$, $V_{BUS} > V_{SLP}$		150		mA
Battery Short Charge Current	$V_{BAT} < V_{SHORT}$, $V_{BUS} > V_{SLP}$		50		mA
LOGIC INPUT THRESHOLD (CD)					
Input Low Level Threshold	Falling			0.4	V
Input High Level Threshold	Rising	1.2			V
Input Bias Current	Voltage on control pin is 5V			1	μA
CHARGE TERMINATION DETECTION					
Termination Charge Current Programmable Range	$V_{BAT} > V_{OREG} - V_{RECH}$, $V_{BUS} > V_{SLP}$, Programmable	25		400	mA
Deglitch Time for Charge Termination	Both rising and falling, 2mV overdrive, t_{RISE}, t_{FALL}= 100ns		30		ms
BAD ADAPTOR DETECTION					
Input Voltage Lower Limit	Bad Adaptor Detection		3.8		V
Hysteresis for V_{IN_MIN}	Input Voltage Rising		150		mV
Deglitch Time for VBUS Rising above V_{IN_MIN}	Rising Voltage, 2mV overdrive, t_{RISE}=100ns		30		ms
Detect Current to GND	During bad adaptor detection		30		mA
Detection Interval	Input power source detection		2		S
INPUT BASED DYNAMIC POWER MANAGEMENT					
V_{INDPM} Threshold			4.52		V
INPUT CURRENT LIMITING					
Input Current Limiting			5000		mA
VLDO REGULATOR					
Internal Bias Regulator Voltage	V_{PMID}> 5.1V, I_{VLDO} = 1mA, C_{LDO}=1μF		4.9		V
V_{LDO} Output Short Current Limit	V_{VLDO} = 90% regulation		50		mA
BATTERY RECHARGE THRESHOLD					
Recharge Voltage Threshold	Below V_{OREG}		120		mV
Deglitch Time	V_{BAT} decreasing below threshold, t_{FALL}=100ns, 10mV overdrive		30		ms
STAT OUTPUTS					
Low-level Output Saturation voltage for STAT	I_{STAT} = 10mA, sink current			0.55	V
High-level Leakage Current for STAT	V_{STAT} = 16V			1	μA

PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
BATTERY DETECTION					
Battery Detection Current before Charge Done,(sink current)	Begins after termination detected, $V_{BAT} \le V_{OREG}$		-0.5		mA
Battery Detection Time			262		ms
SLEEP COMPARATOR					
Sleep-mode Entry Threshold, V_{BUS} - V_{BAT}	$2.3V \le V_{BAT} \le V_{OREG}$, V_{BUS} falling		60		mV
Sleep-mode Exit Hysteresis	$2.3V \le V_{BAT} \le V_{OREG}$		200		mV
Deglitch Time for VBUS Rising above V_{SLP}+V_{SLP_EXIT}	Rising voltage, 2mV overdrive, t_{RISE}=100ns		30		ms
UNDER VOLTAGE LOCKOUT (UVLO)					
IC Active Threshold voltage	VBUS rising - Exits UVLO		3.3		V
IC Active Hysteresis	VBUS falling below UVLO – Enters UVLO		150		mV
PWM					
Voltage from BOOT pin to SW pin	During charge operation		4		V
Internal Top Reverse Blocking MOSFET On-resistance	I_{IN_LIMIT} = 500mA, Measured from VBUS to PMID		55		mΩ
Internal Top N-channel Switching MOSFET On-resistance	Measured from PMID to SW, V_{BOOT}– V_{SW} = 4V		60		mΩ
Maximum Duty Cycle			99		%
CHARGE MODE PROTECTION					
Input OVP Voltage Threshold	VBUS threshold to turn off converter during charge		16.0		V
OVP Threshold Hysteresis	VBUS falling		1		V
Output OVP Voltage Threshold	VBAT threshold over V_{OREG} to turn off charger during charge		117		%V_{OREG}
V_{BAT_OVP} Hysteresis	Lower limit for V_{BAT} falling from above V_{BAT_OVP}		11		%V_{OREG}
Precond to Fast Charge Threshold	V_{BAT} rising, typical application		3		V
$V_{PRECOND}$ Hysteresis	V_{BAT} falling below $V_{PRECOND}$, typical application		100		mV
Trickle to Precond Charge Threshold	V_{BAT} rising, typical application		2.1		V
V_{SHORT} hysteresis	V_{BAT} falling below V_{SHORT}, typical application		100		mV
THERMAL CHARACTERISTICS					
Thermal Trip			165		˚C
Thermal Hysteresis			30		˚C
Thermal Regulation Threshold	Charge current begins to reduce		120		˚C
NTC Cold Temperature Threshold	VNTC Rising, As percentage of VLDO	63	65	67	%

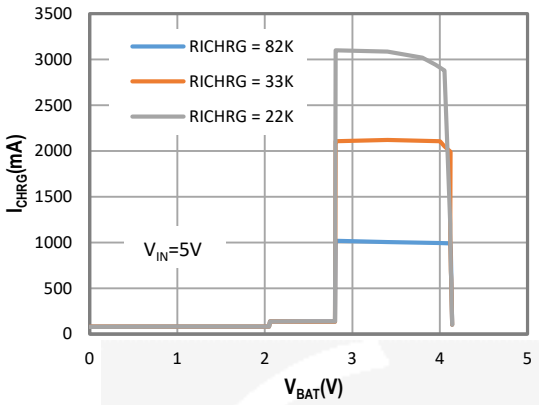
PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
NTC Cold Temperature Hysteresis	VNTC Falling		30		mV
NTC Hot Temperature Threshold	VNTC Falling, As percentage of VLDO	31	33	35	%
NTC Hot Temperature Hysteresis	VNTC Rising		70		mV
NTC Hot Temperature Threshold for PCB OTP	VNTC Falling, As percentage of VLDO	30	32	34	%
NTC Hot Temperature Hysteresis for PCB OTP	VNTC Rising		85		mV

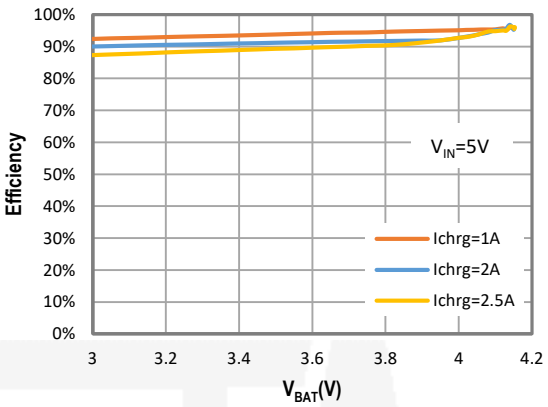
PIN DESCRIPTION

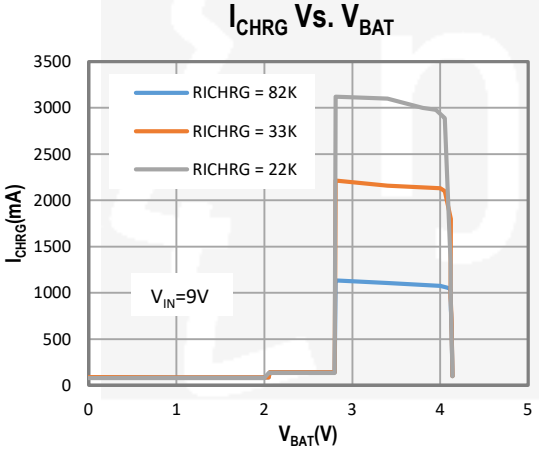
QFNFC1.7x2-20 PIN#	QFN4x4-24 PIN#	NAME	DESCRIPTION
A1, A2	19	VBUS	Charger input voltage. Bypass it with a 4.7μF ceramic capacitor from VBUS to GND.
A3	21	BOOT	Bootstrap capacitor connection for the high-side FET gate driver. Connect a 10nF ceramic capacitor (voltage rating ≥ 10 V) from BOOT pin to SW pin.
A4	23	IEOC	Termination charge current setting pin. Connect a resistor between this pin and GND to set the charge current value during EOC stage.
B1, B2, B3	17	PMID	Connection point between reverse blocking FET and high-side switching FET. Bypass it with a minimum of 4.7μF capacitor from PMID to GND.
B4	1	ICHRG	Fast charge current setting pin. Connect a resistor between this pin and GND to set the charge current value during CC stage.
C1, C2, C3	16	SW	Internal switch to output inductor connection.
C4	3	STAT	Charge status pin. Pull low when charge in progress. Open drain for other conditions.
D1, D2, D3	15	GND	Ground
D4	5	NTC	Battery temperature monitoring input pin. It sets the valid temperature operating range for the battery charging.
E1	13	VBATS	VBATS pin is always shorted to VBAT pin.
E2	11	CD	Charge disable control pin. CD=0, charge is enabled. CD=1, charge is disabled and VBUS pin is high impedance to GND.
E3	9	VLDO	LDO output voltage. Bypass it with 1μF capacitor from VLDO to GND.
E4	7	VBAT	Positive battery terminal.
	2,4,6,8,10,12, 14,18,20,22,24	NC	None connection.

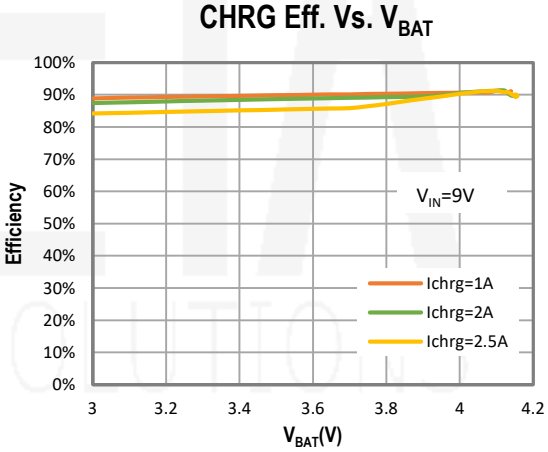
TYPICAL CHARACTERISTICS

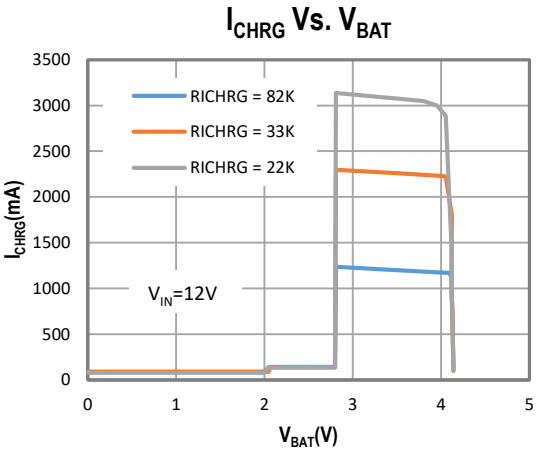
(Typical values are at T_A = 25°C unless otherwise specified.)

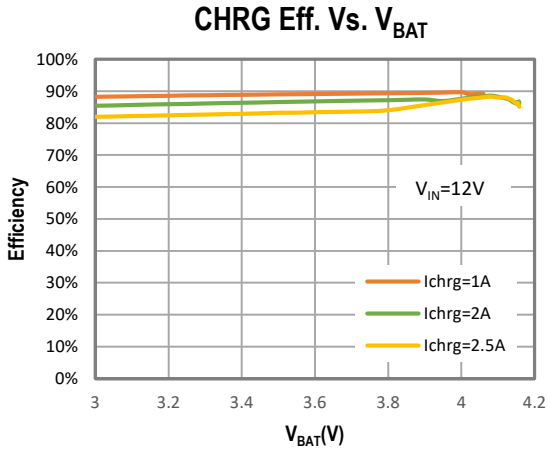












APPLICATION INFORMATION

BATTERY TERMINATION CURRENT

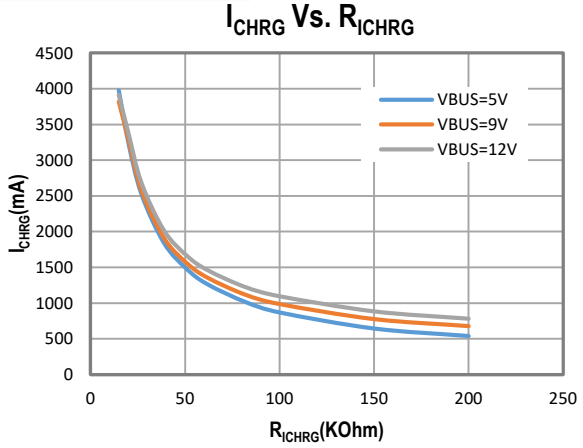
ETA6911 is allowed to program termination current by an external resistor RIEOC. Follow the below table to select a suitable resistor.

RIEOC(KOhm)	IEOC(mA)
25	25
50	50
100	100
200	200
400	400

BATTERY CHARGE CURRENT

ETA6911 can program charge current by an external resistor RICHRG. Follow the below table to select a suitable resistor.

VBUS = 5V		VBUS = 9V		VBUS = 12V	
RICHRG (KOhm)	ICHRG (mA)	RICHRG (KOhm)	ICHRG (mA)	RICHRG (KOhm)	ICHRG (mA)
200	540	200	680	200	779
150	645	150	778	150	882
100	870	100	988	100	1094
82	1016	82	1118	82	1222
62	1263	62	1356	62	1459
51	1477	51	1559	51	1662
39	1839	39	1908	39	2012
27	2525	27	2577	27	2683
20	3256	20	3302	20	3392
15	3977	15	3817	15	3915



BAD ADAPTOR DETECTION

IC performs the bad adaptor detection by applying a current sink to VBUS. If the VBUS is higher than V_{IN_MIN} for 30ms, the adaptor is good and the charge process begins. Otherwise, if the VBUS drops below V_{IN_MIN}, a bad adaptor is detected. After a holding time in 2s, the IC repeats adaptor detection process. IC repeats this process until the VBUS passes the condition that VBUS is higher than V_{IN_MIN}.

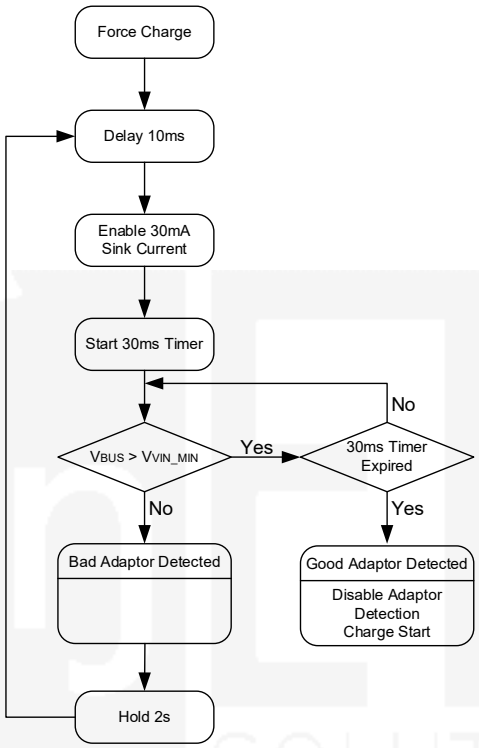


Figure 1: Bad Adaptor Detection Process Flow Chart

CHARGING PROFILE

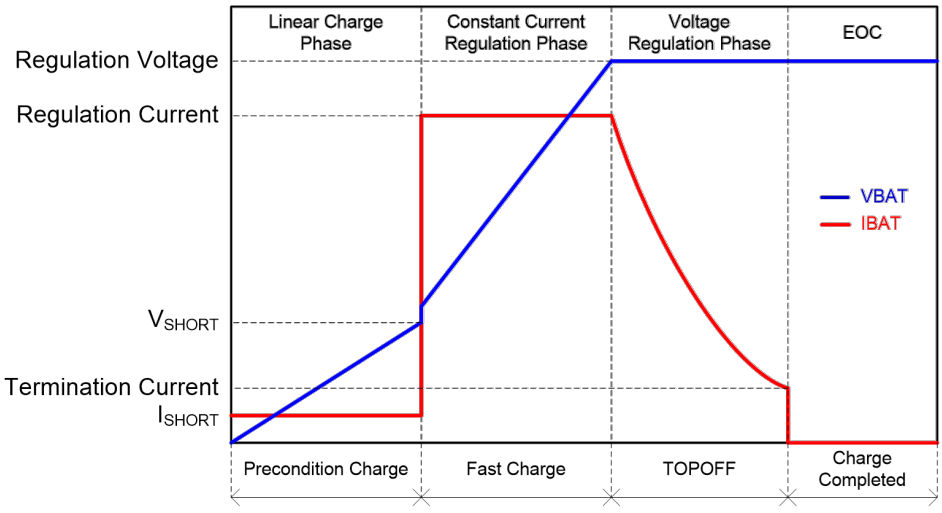


Figure 2: Typical Charging Profile. Case of being without Input Current Limit

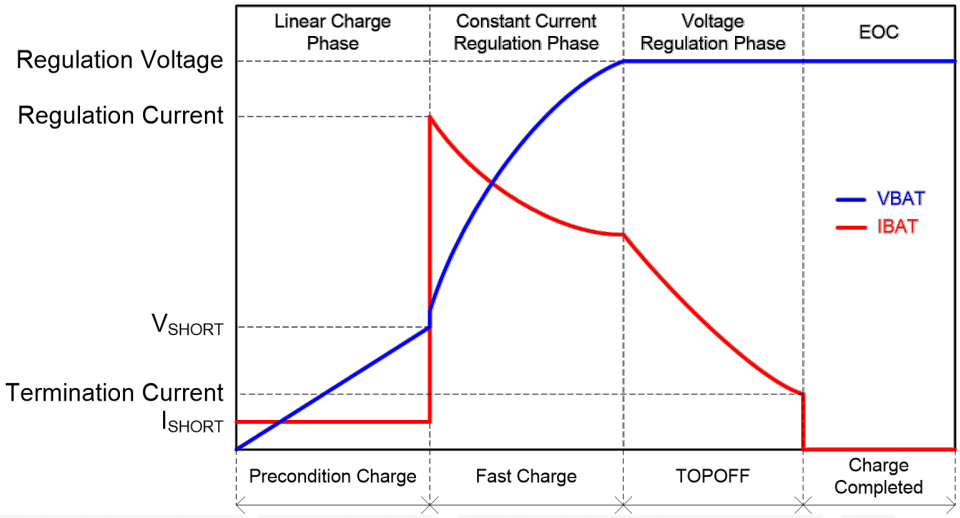


Figure 3: Typical Charging Profile. Case of being with Input Current Limit

INPUT CURRENT LIMIT REGULATION

During the charging process, if the Q1 current exceeds input current limit, Q1 will be controlled into limit loop, PMID voltage will decrease. Once charge detects PMID voltage drop for more than I_{IN_LIM} * R_{Q1},), the charge current begins to taper down to prevent any further drop of PMID voltage. When the IC enters this mode, the charge current is lower than the set value and the VIN_ILIM bits are set. This feature makes the part be not over power that heat the part much.

DYNAMIC POWER MANAGEMENT

During the charging process, if the input power source is not able to support the programmed or default charging current, the VBUS voltage will decrease. Once the VBUS drops to VIN_DPM (default 4.52V), the charge current begins to taper down to prevent any further drop of VBUS. When the IC enters this mode, the charge current is lower than the set value and the special charger bit is set. This feature makes the IC compatible with adapters having different current capabilities.

THERMAL REGULATION

During the charging process, if the junction temperature is above T_{FB} (120°C), the charge current is reduced. Charge current is reduced to minimum level (550mA) when junction temperature hits 130°C. This feature makes the IC be not over temperature during high charge current at low battery voltage. When battery voltage high enough, power crosses the part is lower, junction temperature is lower, then battery is charged with full set current.

Beside the thermal regulation, part is protected by second temperature protection, thermal shutdown. When junction temperature hit T_{SHUT}, IC will be turn off until part cold down 30°C.

LINEAR CHARGE – PRECONDITION CHARGE

When battery voltage is between V_{BAT_SHORT} – $V_{BAT\_PRECOND}$, battery will be charge by a linear current $I_{PRECOND}$.

To prevent battery from explosion when the voltage is too low, under V_{BAT_SHORT}, IC charges battery with a linear current, I_{SHORT}. I_{SHORT} is programmed by level of VBUS.

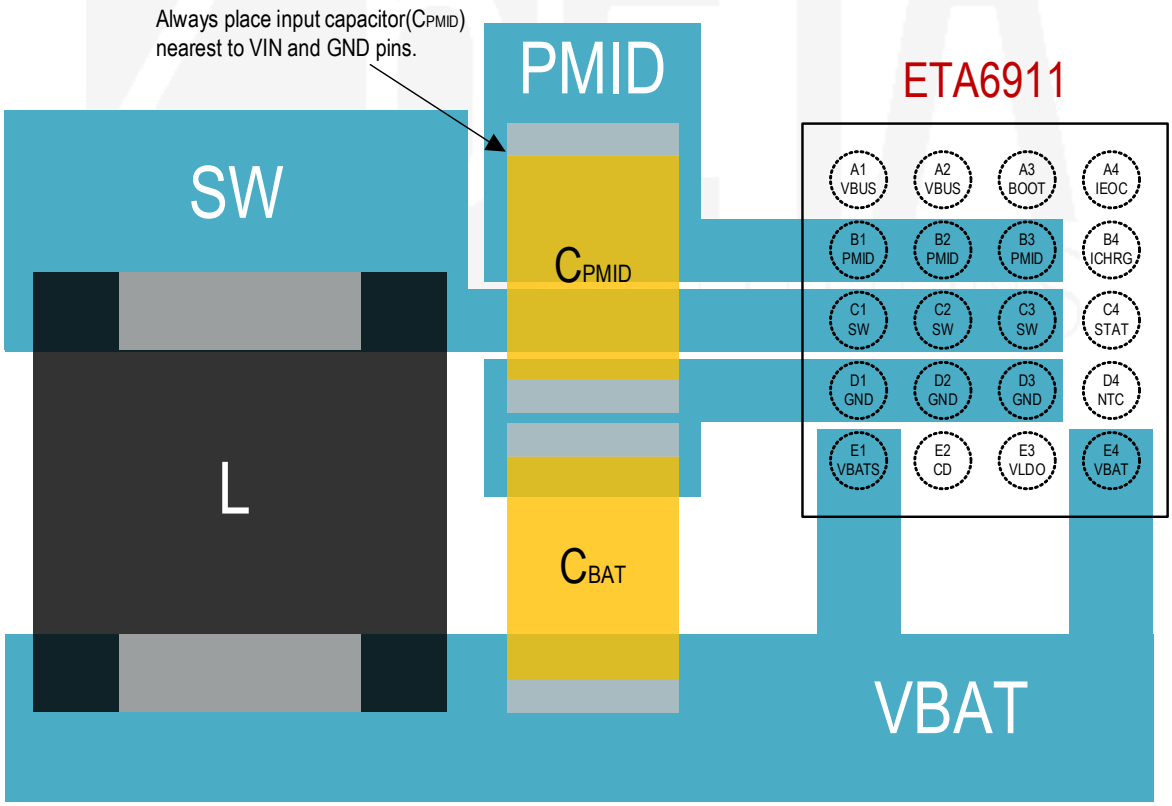
CHARGE COMPLETE

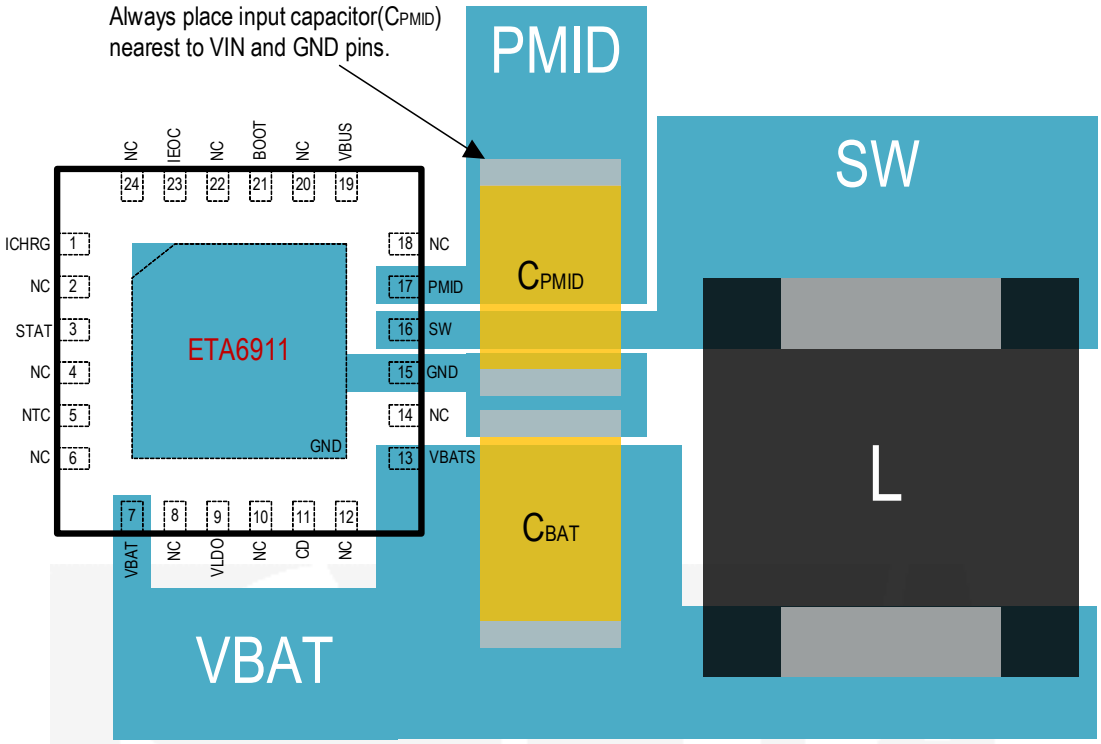
When Charge Current hits termination threshold and IC still detect valid battery, IC indicates charge complete as release STAT. In this, IC allows to recharge when battery voltage drops below recharge threshold.

PCB GUIDELINES

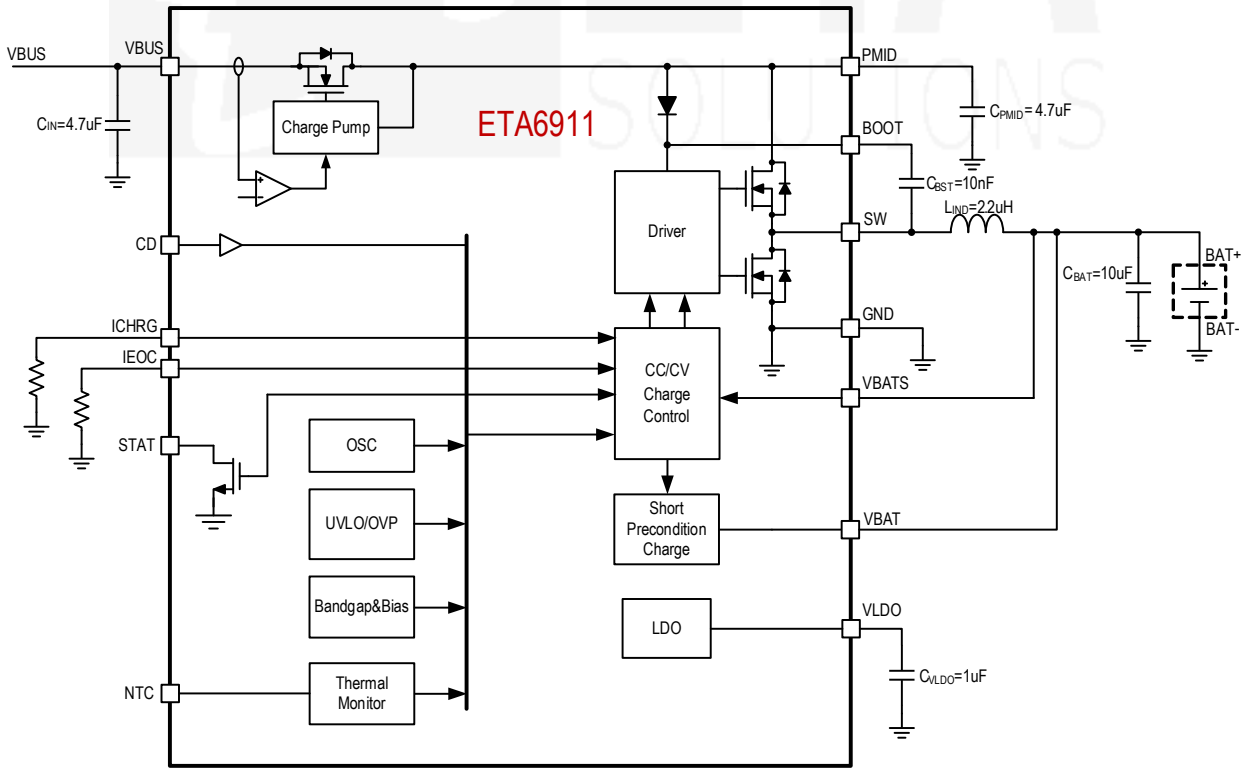
Please always put PMID capacitor closest to the PMID pins and GND pins. As such PMID capacitor serves as the input capacitor of switching charger, and if the capacitor is connected to the GND pins thru ground plane, 2 serial vias (capacitor to ground plane and ground plane to GND pins) are introduced, which means a serial parasitic inductor is placed between the input capacitor and the real input pins. And thus, the decoupling function of such input capacitor is compromised. So, lots of switching noise may no longer be filtered by the input capacitor, and it leads to instability of the switching charger.

The following illustration shows the correct way to place the input capacitor.



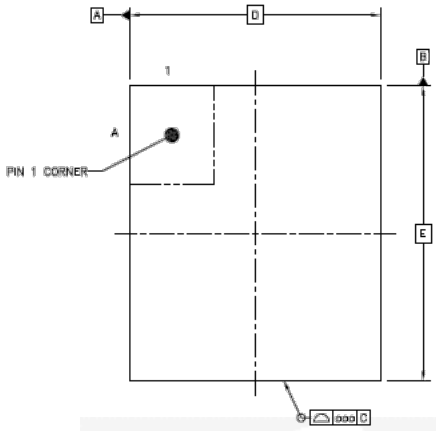


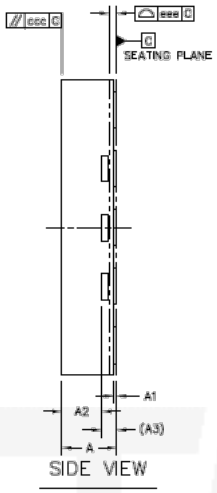
BLOCK DIAGRAM

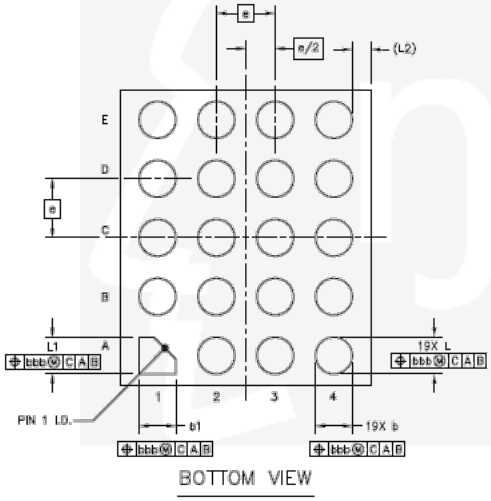


PACKAGE OUTLINE

Package:QFNFC1.7x2-20

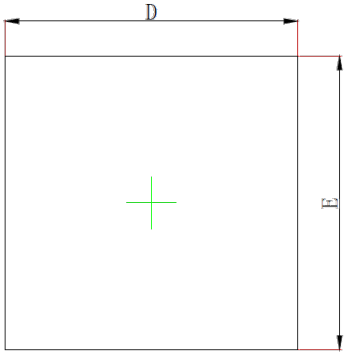




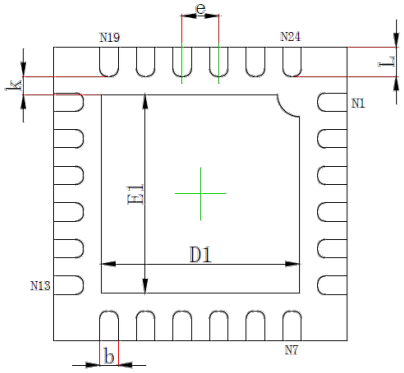


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.32	0.37	0.4
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.27	---
L/F THICKNESS		A3		0.102 REF	
LEAD WIDTH		b	0.2	0.25	0.3
		b1	0.15	0.25	0.35
BODY SIZE	X	D		1.7 BSC	
	Y	E		2 BSC	
LEAD PITCH		e		0.4 BSC	
LEAD LENGTH		L	0.2	0.25	0.3
		L1	0.15	0.25	0.35
LEAD EDGE TO PACKAGE EDGE		L2		0.125 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.05	
LEAD OFFSET		bbb		0.07	

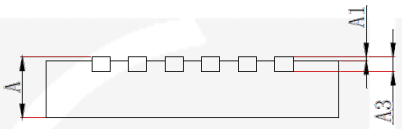
Package:QFN4x4-24



Top View



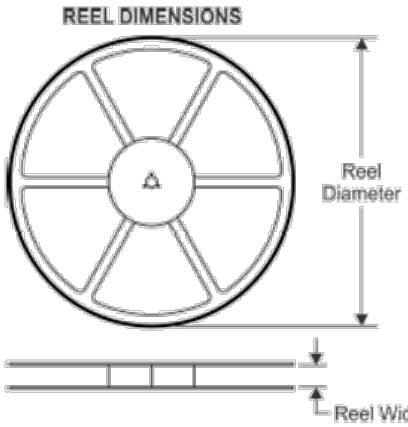
Bottom View

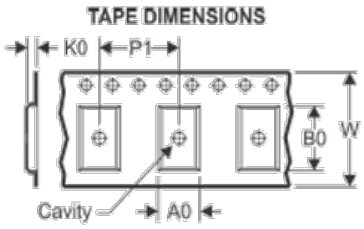


Side View

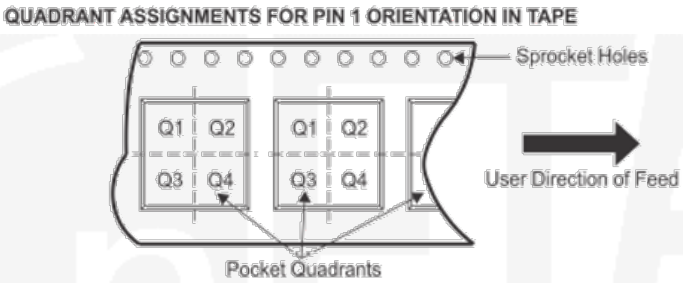
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.600	2.800	0.102	0.110
E1	2.600	2.800	0.102	0.110
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ETA6911FQHU	QFNFC1.7x2-20	20	3000	180	9.5	1.95	2.25	0.43	4	8	Q1
ETA6911V435FQHU	QFNFC1.7x2-20	20	3000	180	9.5	1.95	2.25	0.43	4	8	Q1
ETA6911Q4Y	QFN4x4-24	24	5000	330	12.4	4.3	4.3	1.1	8	12	Q1
ETA6911V435Q4Y	QFN4x4-24	24	5000	330	12.4	4.3	4.3	1.1	8	12	Q1