

## HD3SS214 8.1Gbps DisplayPort 1.4 2:1/1:2 差动开关

### 1 特性

- 符合 Displayport 1.4 电气标准
- 2:1 和 1:2 开关最高支持 8.1Gbps 的数据速率
- 支持热插拔检测 (HPD)、辅助 (AUX) 和显示数据通道 (DDC) 间的切换
- 8GHz 的宽差分带宽 (BW)
- 出色的动态电气特性
- $V_{DD}$  工作范围:  $3.3V \pm 10\%$
- 扩展的工业温度范围:  
-40°C 至 105°C
- 5mm x 5mm, 50 焊球  $\mu$ BGA 封装
- 输出使能 (OE) 引脚禁用开关以省电
- 功耗
  - 工作模式:  $< 2mW$  (典型值)
  - 待机模式:  $< 10\mu W$  (典型值) (OE = 低电平  
时)

### 2 应用范围

- 笔记本电脑
- 台式机/一体化计算机
- 集线站
- 数字电视

### 3 说明

HD3SS214 是一款高速无源开关，能够在应用中将两个完全 DisplayPort 4 通道端口从两个源之一切换到一个目标位置。它还将一个源切换到两个接收设备中的一个。对于 DisplayPort 应用，采用 ZQE 封装的 HD3SS214 支持在辅助 (AUX)、显示数据通道 (DDC) 和热插拔检测 (HPD) 信号间切换。

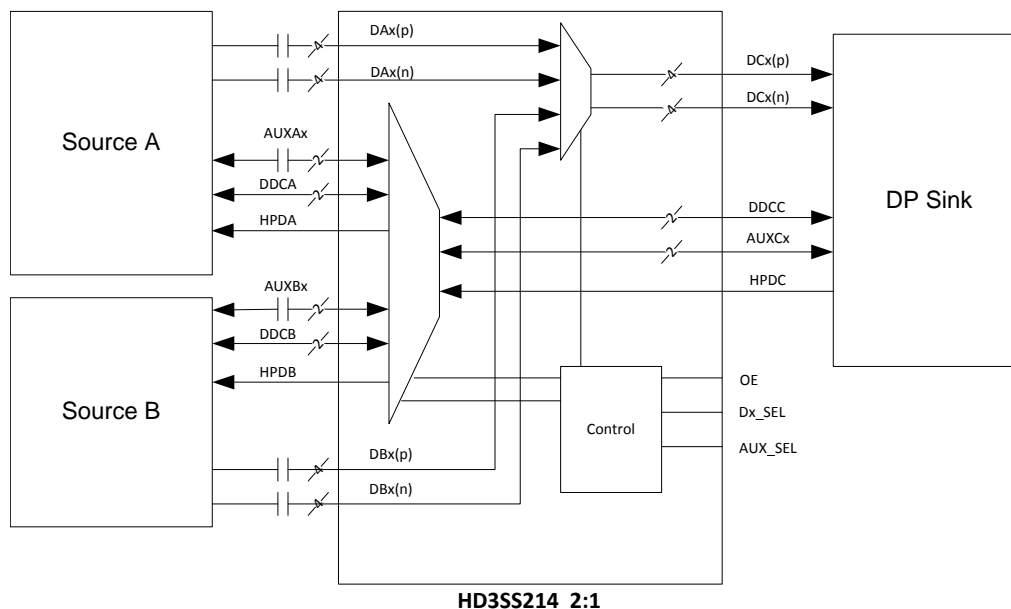
一个典型应用就是包含 2 个图形处理单元 (GPU) 的母板，此处理单元需要驱动一个 DisplayPort 负输出。GPU 由  $Dx\_SEL$  引脚选择。另外的应用是一个源需要在两个负输出间切换，其中的一个例子就是一个侧面连接器和一个扩展坞连接器。此切换由  $Dx\_SEL$  和  $AUX\_SEL$  引脚控制。HD3SS214 在 -40°C 至 105°C 的扩展工业温度范围内由 3.3V 单电源供电运行。

#### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
HD3SS214	$\mu$ BGA (50)	5.00mm x 5.00mm
HD3SS214I		

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化原理图



Copyright © 2016, Texas Instruments Incorporated



## 目录

<b>1</b>	特性 .....	<b>1</b>	7.3	Feature Description .....	<b>9</b>
<b>2</b>	应用范围 .....	<b>1</b>	7.4	Device Functional Modes .....	<b>10</b>
<b>3</b>	说明 .....	<b>1</b>	<b>8</b>	<b>Application and Implementation</b> .....	<b>11</b>
<b>4</b>	修订历史记录 .....	<b>2</b>	8.1	Application Information .....	<b>11</b>
<b>5</b>	<b>Pin Configuration and Functions</b> .....	<b>3</b>	8.2	Typical Application .....	<b>11</b>
<b>6</b>	<b>Specifications</b> .....	<b>5</b>	<b>9</b>	<b>Power Supply Recommendations</b> .....	<b>16</b>
6.1	Absolute Maximum Ratings .....	<b>5</b>	<b>10</b>	<b>Layout</b> .....	<b>16</b>
6.2	ESD Ratings .....	<b>5</b>	10.1	Layout Guidelines .....	<b>16</b>
6.3	Recommended Operating Conditions .....	<b>5</b>	10.2	Layout Example .....	<b>17</b>
6.4	Thermal Information .....	<b>5</b>	<b>11</b>	器件和文档支持 .....	<b>19</b>
6.5	Electrical Characteristics .....	<b>6</b>	11.1	器件支持 .....	<b>19</b>
6.6	Electrical Characteristics, Device Parameters .....	<b>6</b>	11.2	接收文档更新通知 .....	<b>19</b>
6.7	Timing Requirements .....	<b>7</b>	11.3	社区资源 .....	<b>19</b>
6.8	Typical Characteristics .....	<b>7</b>	11.4	商标 .....	<b>19</b>
<b>7</b>	<b>Detailed Description</b> .....	<b>8</b>	11.5	静电放电警告 .....	<b>19</b>
7.1	Overview .....	<b>8</b>	11.6	Glossary .....	<b>19</b>
7.2	Functional Block Diagram .....	<b>9</b>	<b>12</b>	机械、封装和可订购信息 .....	<b>19</b>

## 4 修订历史记录

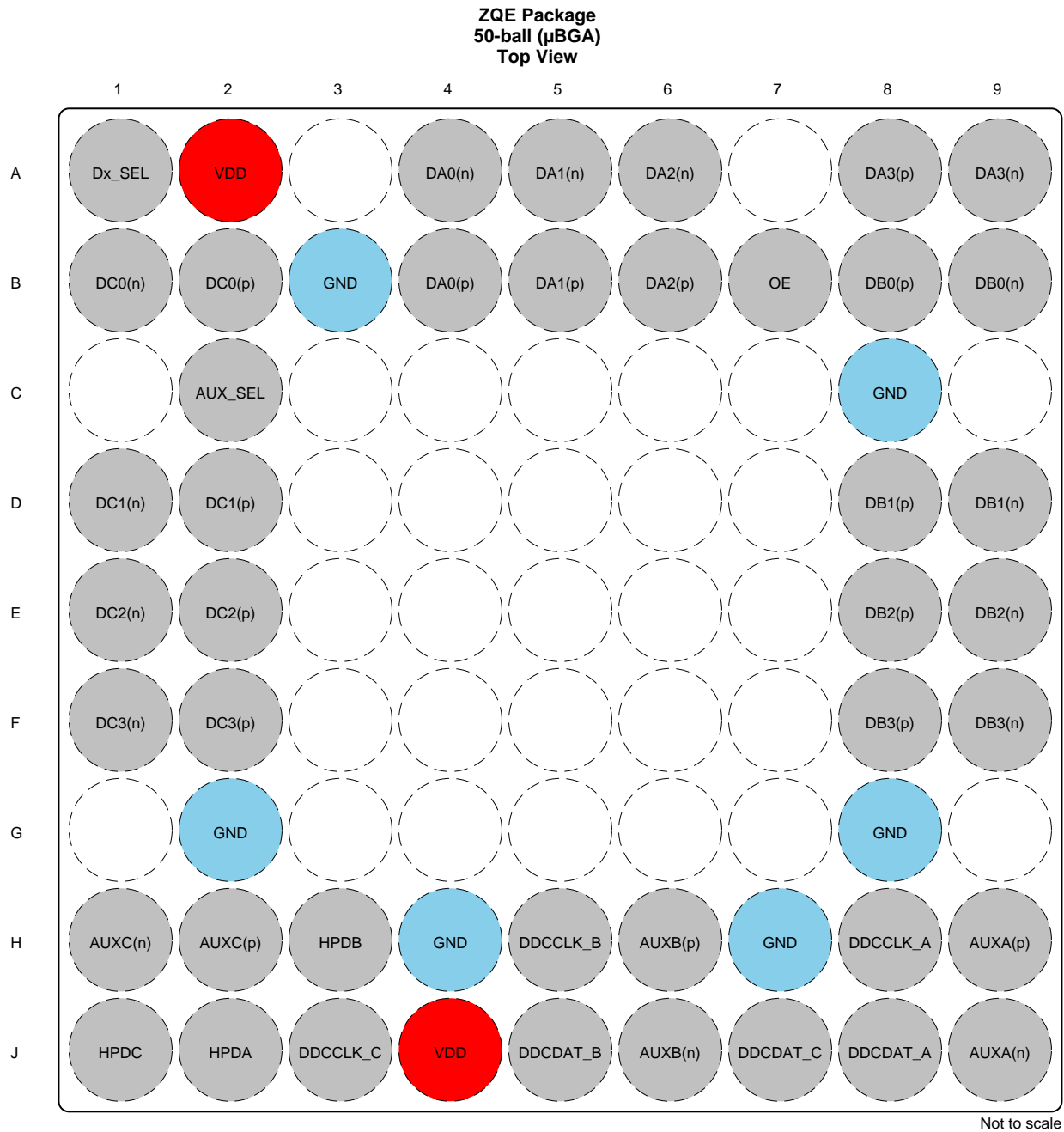
### Changes from Revision A (July 2016) to Revision B Page

•	将标题和特性从 DisplayPort 1.3 改为 DisplayPort 1.4 .....	<b>1</b>
---	--	----------

### Changes from Original (December 2015) to Revision A Page

•	Changed DC2(p) to DC2(n) in Pin Functions .....	<b>4</b>
•	Changed DC2(n) to DC2(p) in Pin Functions .....	<b>4</b>

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION <sup>(1)</sup>
NO.	NAME		
A1	Dx_SEL	Control I	High Speed Port Selection Control Pins
A2,J4	VDD	Supply	3.3 V Positive power supply voltage
A4	DA0(n)	I/O	Port A, Channel 0, High Speed Negative Signal
A5	DA1(n)	I/O	Port A, Channel 1, High Speed Negative Signal

(1) The high speed data ports incorporate 20-kΩ pull down resistors that are switched in when a port is not selected and switched out when the port is selected.

**Pin Functions (continued)**

PIN		I/O	DESCRIPTION <sup>(1)</sup>
NO.	NAME		
A6	DA2(n)	I/O	Port A, Channel 2, High Speed Negative Signal
A8	DA3(p)	I/O	Port A, Channel 3, High Speed Positive Signal
A9	DA3(n)	I/O	Port A, Channel 3, High Speed Negative Signal
B1	DC0(n)	I/O	Port C, Channel 0, High Speed Negative Signal
B2	DC0(p)	I/O	Port C, Channel 0, High Speed Positive Signal
B3,C8,G2,G8,H4,H7	GND	Supply	Ground
B4	DA0(p)	I/O	Port A, Channel 0, High Speed Positive Signal
B5	DA1(p)	I/O	Port A, Channel 1, High Speed Positive Signal
B6	DA2(p)	I/O	Port A, Channel 2, High Speed Positive Signal
B7	OE	I	Output Enable: OE = V <sub>IH</sub> : Normal Operation OE = V <sub>IL</sub> : Standby Mode
B8	DB0(p)	I/O	Port B, Channel 0, High Speed Positive Signal
B9	DB0(n)	I/O	Port B, Channel 0, High Speed Negative Signal
C2	AUX_SEL	Control I	AUX/DDC Selection Control Pin in Conjunction with Dx_SEL Pin
D1	DC1(n)	I/O	Port C, Channel 1, High Speed Negative Signal
D2	DC1(p)	I/O	Port C, Channel 1, High Speed Positive Signal
D8	DB1(p)	I/O	Port B, Channel 1, High Speed Positive Signal
D9	DB1(n)	I/O	Port B, Channel 1, High Speed Negative Signal
E1	DC2(n)	I/O	Port C, Channel 2, High Speed Negative Signal
E2	DC2(p)	I/O	Port C, Channel 2, High Speed Positive Signal
E8	DB2(p)	I/O	Port B, Channel 2, High Speed Positive Signal
E9	DB2(n)	I/O	Port B, Channel 2, High Speed Negative Signal
F1	DC3(n)	I/O	Port C, Channel 3, High Speed Negative Signal
F2	DC3(p)	I/O	Port C, Channel 3, High Speed Positive Signal
F8	DB3(p)	I/O	Port B, Channel 3, High Speed Positive Signal
F9	DB3(n)	I/O	Port B, Channel 3, High Speed Negative Signal
H1	AUXC(n)	I/O	Port C AUX Negative Signal
H2	AUXC(p)	I/O	Port C AUX Positive Signal
H3	HPDB	I/O	Port B Hot Plug Detect
H6	AUXB(p)	I/O	Port B AUX Positive Signal
H5	DDCCLK_B	I/O	Port B DDC Clock Signal
H8	DDCCLK_A	I/O	Port A DDC Clock Signal
H9	AUXA(p)	I/O	Port A AUX Positive Signal
J1	HPDC	I/O	Port C Hot Plug Detect
J2	HPDA	I/O	Port A Hot Plug Detect
J3	DDCCLK_C	I/O	Port C DDC Clock Signal
J5	DDCDAT_B	I/O	Port B DDC Data Signal
J6	AUXB(n)	I/O	Port B AUX Negative Signal
J7	DDCDAT_C	I/O	Port C DDC Data Signal
J8	DDCDAT_A	I/O	Port A DDC Data Signal
J9	AUXA(n)	I/O	Port A AUX Negative Signal

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)(2)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range <sup>(3)</sup>	V <sub>DD</sub>	-0.5	4	V
Voltage range	Differential I/O	-0.5	4	V
	Control pin	-0.5	V <sub>DD</sub> + 0.5	
Continuous power dissipation		See <a href="#">Thermal Information</a>		

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values, except differential voltages, are with respect to network ground terminal.
- (3) Tested in accordance with JEDEC Standard 22, Test Method A114-B

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

Typical values for all parameters are at V<sub>CC</sub> = 3.3 V and T<sub>A</sub> = 25°C. All temperature limits are specified by design.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>DD</sub>	Supply voltage		3	3.3	3.6	V
V <sub>IH</sub>	Input high voltage	Control Pins, Signal Pins (D <sub>x</sub> _SEL, AUX_SEL, MODE, OE)	2		V <sub>DD</sub>	V
V <sub>IM</sub>	Input mid level voltage	AUX_SEL Pin	V <sub>DD</sub> /2 -300 mV	V <sub>DD</sub> /2	V <sub>DD</sub> /2 -300 mV	V
V <sub>IL</sub>	Input low voltage	Control Pins, Signal Pins (D <sub>x</sub> _SEL, AUX_SEL, MODE, OE)	-0.1		0.8	V
V <sub>I/O_Diff</sub>	Differential voltage (D <sub>x</sub> , AUX <sub>x</sub> )	Switch I/O diff voltage	0		1.8	V <sub>pp</sub>
V <sub>I/O_CM</sub>	D <sub>x</sub> switching I/O Common mode voltage	Switch I/O common mode voltage	0		2	V
	AUX <sub>x</sub> (1) switching I/O Common mode voltage		0		3.6	
Operating free-air temperature		HD3SS214	0		70	°C
		HD3SS214I	-40		105	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		HD3SS214	UNIT
		ZQE (µBGA)	
		50 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	90.5	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	41.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	53.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	53.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{IH}$	Input High Current (Dx_SEL, AUX_SEL)	$V_{DD} = 3.6\text{ V}$ , $V_{IN} = V_{DD}$			1	$\mu\text{A}$
$I_{IM}$	Input Mid Current (AUX_SEL)	$V_{DD} = 3.6\text{ V}$ , $V_{IN} = V_{DD}/2$			1	$\mu\text{A}$
$I_{IL}$	Input Low Current (Dx_SEL, AUX_SEL)	$V_{DD} = 3.6\text{ V}$ , $V_{IN} = \text{GND}$			1	$\mu\text{A}$
$I_{LKG}$	Leakage Current (Dx_SEL, AUX_SEL)	$V_{DD} = 3.3\text{ V}$ , $V_{IN} = 2\text{ V}$ , $\text{OE} = 3.3\text{ V}$			1	$\mu\text{A}$
	Leakage Current (HPDx)	$V_{DD} = 3.3\text{ V}$ , $V_{IN} = 2\text{ V}$ , $\text{OE} = 3.3\text{ V}$ ; $\text{Dx\_SEL} = 3.3\text{ V}$			1	$\mu\text{A}$
	Leakage Current (HPDx)	$V_{DD} = 3.3\text{ V}$ , $V_{IN} = 2\text{ V}$ , $\text{OE} = 3.3\text{ V}$ ; $\text{Dx\_SEL} = \text{GND}$			1	$\mu\text{A}$
$I_{OFF}$	Device Shut Down Current	$V_{DD} = 3.6\text{ V}$ , $\text{OE} = \text{GND}$			2.5	$\mu\text{A}$
$I_{DD}$	Supply Current	$V_{DD} = 3.6\text{ V}$ , $\text{Dx\_SEL/AUX\_SEL} = \text{VDD/GND}$		0.6	1	$\text{mA}$
<b>DA, DB, DC HIGH SPEED SIGNAL PATH</b>						
$C_{ON}$	Outputs ON Capacitance	$V_{IN} = 0\text{ V}$ , Outputs Open, Switch ON		0.6		$\text{pF}$
$C_{OFF}$	Outputs OFF Capacitance	$V_{IN} = 0\text{ V}$ , Outputs Open, Switch OFF		0.8		$\text{pF}$
$R_{ON}$	ON resistance	$V_{DD} = 3.3\text{ V}$ , $V_{CM} = 0.5\text{ V} - 1.5\text{ V}$ , $I_O = -40\text{ mA}$		8	12	$\Omega$
$\Delta R_{ON}$	On resistance match between pairs of the same channel	$V_{DD} = 3.3\text{ V}$ , $V_{CM} = 0.5\text{ V} \leq V_{IN} \leq 1.2\text{ V}$ , $I_O = -40\text{ mA}$			1.5	$\Omega$
$R_{(\text{FLAT\_ON})}$	On resistance flatness ( $R_{ON(\text{MAX})} - R_{ON(\text{MAIN})}$ )	$V_{DD} = 3.3\text{ V}$ , $V_{CM} = 0.5\text{ V} \leq V_{IN} \leq 1.2\text{ V}$		1.3		$\Omega$
<b>AUX, DDC, SIGNAL PATH</b>						
$R_{ON(\text{AUX})}$	ON resistance on AUX channel	$V_{DD} = 3.3\text{ V}$ , $V_{CM} = 0\text{ V} - V_{DD}$ , $I_O = -8\text{ mA}$		6	10	$\Omega$
$R_{ON(\text{DDC})}$	ON resistance on DDC channel	$V_{DD} = 3.3\text{ V}$ , $V_{CM} = 0.4\text{ V}$ , $I_O = -3\text{ mA}$		20	30	$\Omega$

## 6.6 Electrical Characteristics, Device Parameters

over operating free-air temperature range (unless otherwise noted)

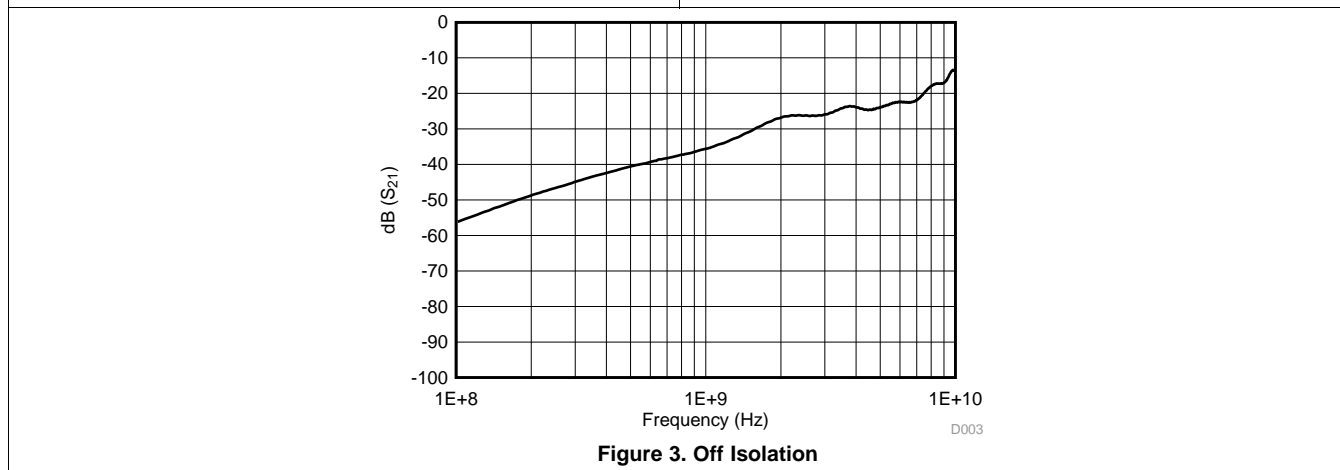
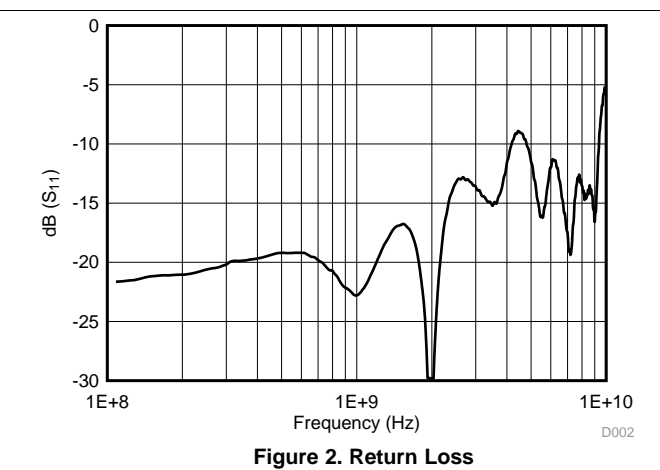
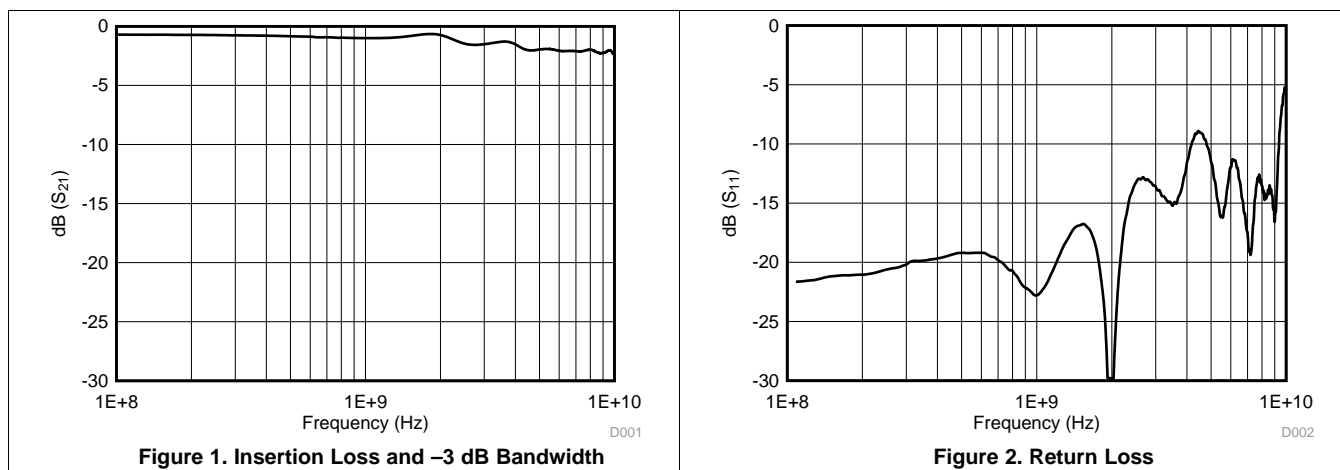
PARAMETER <sup>(1)</sup>		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_L$	Dx Differential Insertion Loss	1.35 GHz		-0.9		$\text{dB}$
		2.7 GHz		-1.4		$\text{dB}$
		4.05 GHz		-1.6		$\text{dB}$
$R_L$	Dx Differential Return Loss	1.35 GHz		-17		$\text{dB}$
		2.7 GHz		-13		$\text{dB}$
		4.05 GHz		-11		$\text{dB}$
$X_{\text{TALK}}$	Dx Differential Crosstalk	1.35 GHz				$\text{dB}$
		2.7 GHz		-53		$\text{dB}$
		4.05 GHz		-47		$\text{dB}$
$O_{\text{IRR}}$	Dx Differential Off-Isolation	1.35 GHz				$\text{dB}$
		2.7 GHz		-26		$\text{dB}$
		4.05 GHz		-24		$\text{dB}$
AUX Bandwidth				500		$\text{MHz}$

- (1) For Return Loss, Crosstalk, Off-Isolation, and Insertion Loss values the data was collected on a Rogers material board with minimum length traces on the input and output of the device under test.

### 6.7 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PD}$	Switch propagation delay	$R_{SC}$ and $R_L = 50 \Omega$			100	ps
$t_{on}$	Dx_SEL/AUX_SEL-to-Switch $t_{on}$ (Data and AUX and DDC)	$R_{SC}$ and $R_L = 50 \Omega$		0.7	1	$\mu s$
$t_{off}$	Dx_SEL/AUX_SEL-to-Switch $t_{off}$ (Data and AUX and DDC)			0.7	1	
$t_{on}$	Dx_SEL/AUX_SEL-to-Switch $t_{on}$ (HPD)	$R_L = 1 k\Omega$		0.7	1	$\mu s$
$t_{off}$	Dx_SEL/AUX_SEL-to-Switch $t_{off}$ (HPD)			0.7	1	
$t_{SK(O)}$	Inter-Pair Output Skew (CH-CH)	$R_{SC}$ and $R_L = 50 k\Omega$			30	ps
$t_{SK(b-b)}$	Intra-Pair Skew added (Bit-Bit)			1	5	ps

### 6.8 Typical Characteristics



## 7 Detailed Description

### 7.1 Overview

The HD3SS214 is an analog, differential passive switch that can work for any high speed interface applications, as long as it is biased at a common mode voltage range of 0 V to 2 V and has differential signaling with differential amplitude up to 1800 mVpp.

---

#### NOTE

HD3SS214 MUX does not provide common mode biasing for the channel. Therefore, it is required that the device is biased from either side for all active channels.

---

In high-speed applications and data paths, signal integrity is an important concern. The switch offers excellent dynamic performance such as high isolation, crosstalk immunity, and minimal bit-bit skew. These characteristics allow the device to function seamlessly in the system without compromising signal integrity. The 2:1/1:2, mux/demux device operates with ports A or B switched to port C, or port C switched to either port A or B. This flexibility allows an application to select between one of two Sources on ports A and B and send the output to the sink on port C. Similarly, a Source on port C can select between one of two Sink devices on ports A and B to send the data.

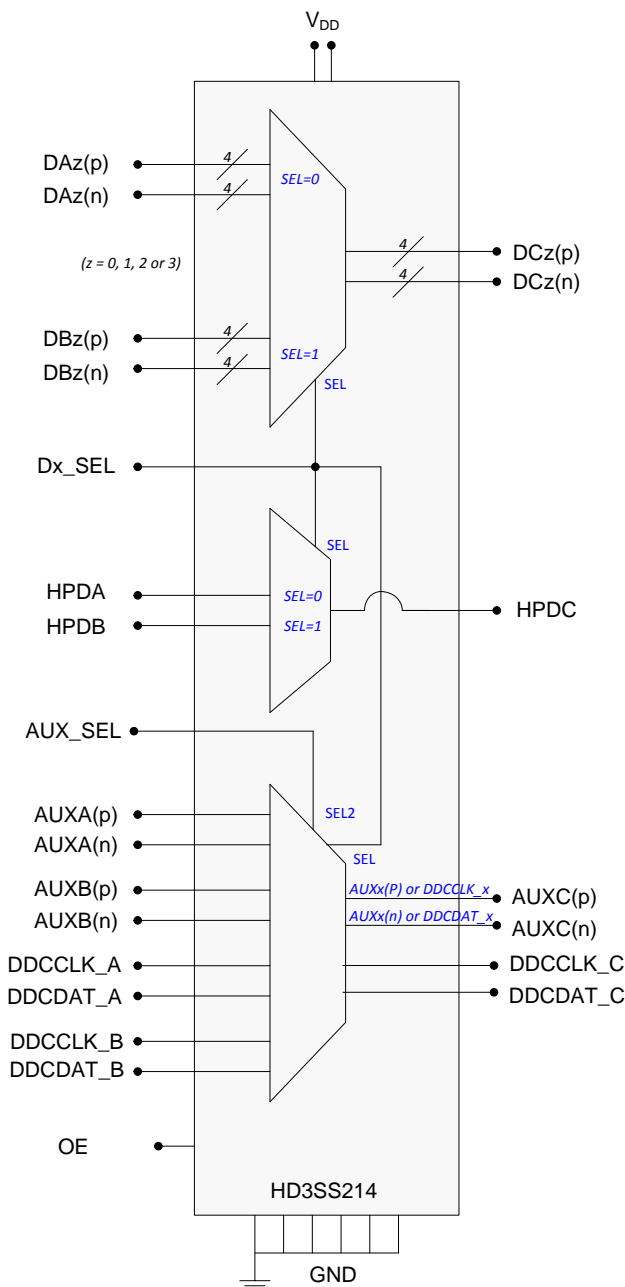
The HPD and data signals are both switched through the Dx\_SEL pin. AUX and DDC are controlled with AUX\_SEL and Dx\_SEL.

With an OE control pin, the HD3SS214 is operational, with low active current, when this pin is high. When OE is pulled low, the device goes into standby mode and draws very little current in order to save power consumption in the application.

HD3SS214 high speed MUX channels have independent adaptive common mode tracking allowing four data paths to have different common mode voltage, simplifying system implementation and avoid inter-op issues.



## 7.2 Functional Block Diagram



Copyright © 2016, Texas Instruments Incorporated

## 7.3 Feature Description

### 7.3.1 High Speed Switching

The HD3SS214 supports switching of 8.1 Gbps data rates. The high speed mux is designed with a wide –3dB differential bandwidth of 8 GHz and industry leading dynamic characteristics. All of these attributes help maintain signal integrity in the application. Each high speed port incorporates 20-kΩ pull down resistors that are switched in when the port is not selected and switched out when the port is selected. Additionally, high speed differential pairs at port C have internal 20-kΩ resistor between positive and negative pins

## Feature Description (continued)

### 7.3.2 HPD, AUX, and DDC Switching

HPD, AUX, and DDC switching is supported through the HD3SS214. This enables the device to work in multiple application scenarios within multiple electrical standards. The AUXA/B and DDCA/B lines can both be switched to the AUXC port. This feature supports DP++ or AUX only adapters. For HDMI applications, the DDC channels are switched to the DDC\_C port only and the AUX channel can remain active or the end user can make it float.

### 7.3.3 Output Enable and Power Savings

The HD3SS214 has two power modes, active/normal operating mode, and standby mode. During standby mode, the device consumes very little current to save the maximum power. To enter standby mode, the OE control pin is pulled low and must remain low. For active/normal operation, the OE control pin should be pulled high to VDD through a resistor.

## 7.4 Device Functional Modes

The HD3SS214 behaves as a two to one or one to two using high bandwidth pass gates. The input ports are selected using the Dx\_SEL pin and Dx\_SEL pin which are shown in [Table 1](#).

**Table 1. AUX/DDC Switch Control Logic<sup>(1)</sup>**

CONTROL LINES		SWITCHED I/O PINS <sup>(2)</sup>								
AUX_SEL	Dx_SEL	DCz(p) Pin z = 0, 1, 2 or 3	DCz(n) Pin z = 0, 1, 2 or 3	HPDC Pin	AUXA	AUXB	AUXC	DDCA	DDCB	DDCC
L	L	DAz(p)	DAz(n)	HPDA	To/From AUXC	Z	To/From AUXA	Z	Z	Z
L	H	DBz(p)	DBz(n)	HPDB	Z	To/From AUXC	To/From AUXB	Z	Z	Z
H	L	DAz(p)	DAz(n)	HPDA	Z	Z	To/From DDCA	To/From AUXC	Z	Z
H	H	DBz(p)	DBz(n)	HPDB	Z	Z	To/From DDCB	Z	To/From AUXC	Z
M <sup>(2)</sup>	L	DAz(p)	DAz(n)	HPDA	To/From AUXC	Z	To/From AUXA	To/From DDCC	Z	To/From DDCA
M <sup>(2)</sup>	H	DBz(p)	DBz(p)	HPDB	Z	To/From AUXC	To/From AUXB	Z	To/From DDCC	To/From DDCB

(1) OE pin - For normal operation, drive OE high. Driving the OE pin low will disable the switch. Note: The ports which are not selected by the control lines will be in high impedance status.

(2) Z = High Impedance

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The HD3SS214 is a 1:2/2:1 DP switch that supports 8.1 Gbps data rates and DP++. This switch is bi-directional, so it can be used to switch two inputs to one output or one input to one of two outputs. In addition to main link switching, this switch also supports AUX and DDC switching, which simplifies DP++ implementation. 3.3 V is used to supply power to the switch.

### 8.2 Typical Application

#### 8.2.1 Dual GPU With Docking Station Support

Many consumer devices require multiple video sources to be routed to multiple output sinks. One example of these devices is a dual-GPU laptop with docking station support. The laptop has two video sources that can be chosen: one low-power integrated GPU and one high-power discrete GPU. The video stream from one of these sources needs to be routed to one of two outputs: the docking station port or the laptop DisplayPort video port. In order to support this functionality, a high data rate, multi-input/multi-output switch system is required.

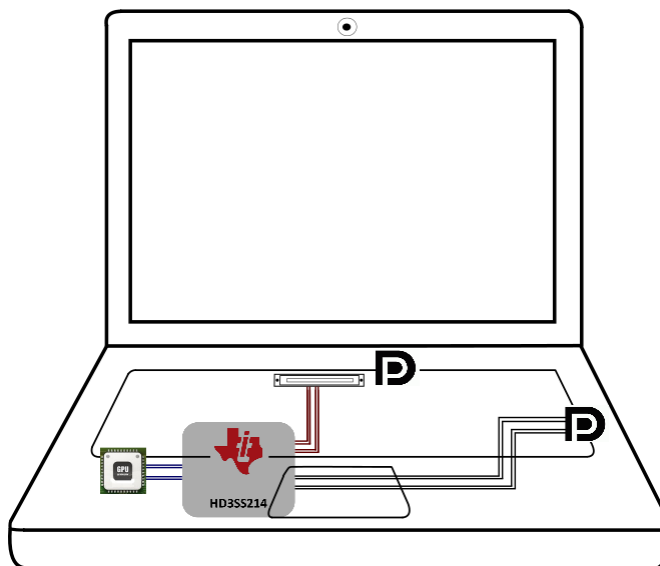


Figure 4. Dual GPU with Docking Station Support

#### 8.2.2 Design Requirements

For this design example, use the parameters shown in [Table 2](#).

Table 2. Design Parameters

PARAMETER	VALUE
$V_{DD}$	3.3 V
Source	DP x1
Sink	DP x2
AUX_SEL Level	M
DP++ Support	No

## 8.2.3 Detailed Design Procedure

### 8.2.3.1 DP Inputs

The HD3SS214 is used as a 1:2 DP switch, the DCx[p/n] are connected to the GPU; the outputs (DAX[p/n] and DBx[p/n] ) are routed to the ++DP connectors of the platform.

#### NOTE

This application information is only to show the principles of operation of the HD3SS214 and not the requirements of all the implementation. Many implementations will require external circuitry to compensate for signal loss (like a DP re-driver).

### 8.2.3.2 Source Selection Interface

Two control pins on the HD3SS214 are responsible for selecting the incoming DP signal: Dx\_SEL and AUX\_SEL. Dx\_SEL controls which high speed ports are selected. A low signal on Dx\_SEL corresponds to Port A routed to Port C and a high signal corresponds to Port B routed to Port C. A slide switch is used to select the level for this signal. In an embedded application, this switch can be replaced by a GPIO signal from a microcontroller.

AUX channel is controlled by AUX\_SEL. This pin configures the switch to route the incoming AUX signal to the outgoing AUX path, when AUX\_SEL = 0 the AUXA channel will be routed to AUXC, when AUX\_SEL = 1 the AUXB channel will be routed to AUXC. [Figure 5](#) shows the selection circuitry.

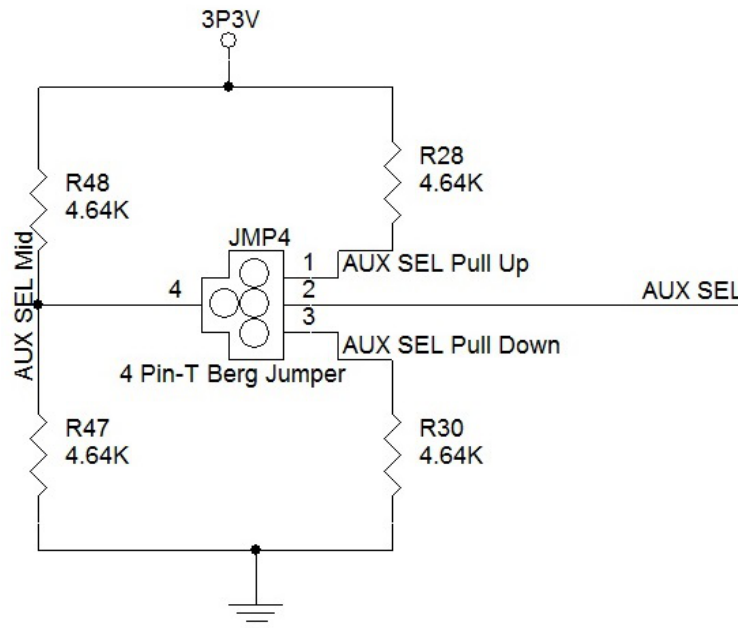


Figure 5. AUX\_SEL Schematic

### 8.2.4 DP++ Support

The HD3SS214 supports DP++ implementations.

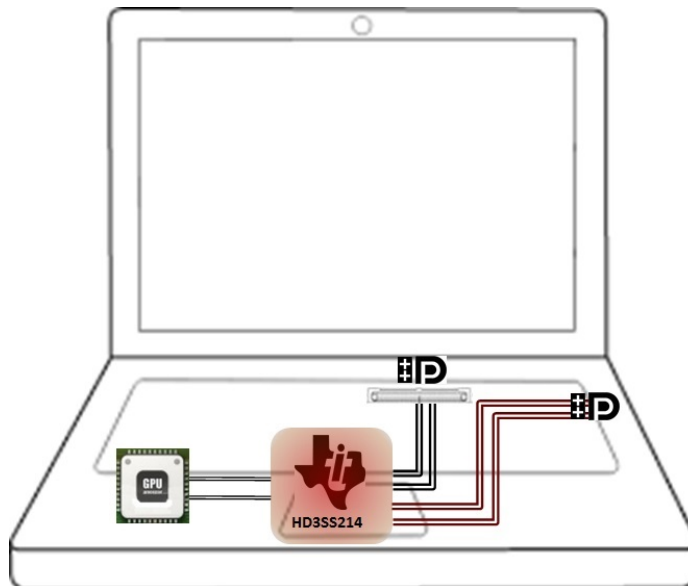


Figure 6. DP++ Docking Station Support

#### 8.2.4.1 Design Requirements

For this example, use the parameters shown in [Table 3](#)

Table 3. Design Parameters

PARAMETER	VALUE
V <sub>DD</sub>	3.3 V
Source	DP x1
Sink	DP x2
AUX_SEL Level	M
DP++ Support	Yes

#### 8.2.4.2 Detailed Design Procedure

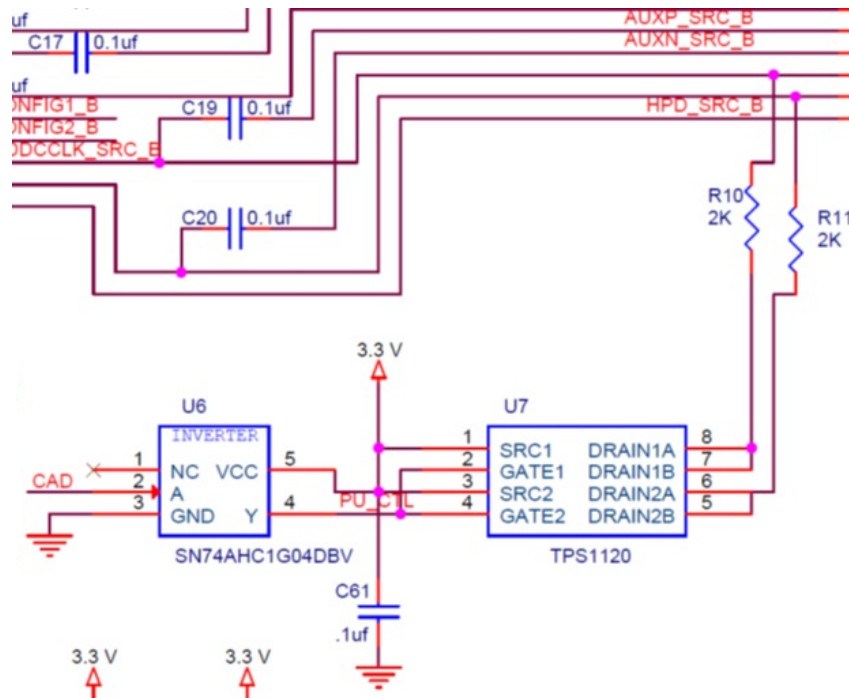
For applications involving DP++ support, following design procedures must be followed.

##### 8.2.4.2.1 AUX and DDC Switching

The HD3SS214 supports DP++ implementations.

According to the DP++ standard, the DP AUX line is repurposed as the DDC line when HDMI signals are being transmitted. Unfortunately, the AUX and DDC signals have very different electrical requirements. AUX is a differential signal that requires AC coupling, while DDC uses I<sup>2</sup>C protocol, which needs pull-up resistors. As a result, these signals are electrically incompatible if extra circuitry is not designed to accommodate the signals.

The source selection design block uses conditional pull-up resistors to support AUX and DDC signals on a unified line. [Figure 7](#) illustrates the circuit that was used to enable the signal.



**Figure 7. Combined AUX/DDC Circuitry**

In this circuit, the unified AUX/DDC lines are split into two branches prior to entering the HD3SS214. One branch is AC coupled and is connected to the AUX inputs of the HD3SS214. The other is connected to the DDC inputs. AUX\_SEL is configured so that the HD3SS214 transmits both of these through the switch. A conditional pull-up resistor system is connected to the DDC branch of the line. This resistor system will enable the pull-up resistors on the line only when HDMI/DVI signals are being transmitted, that is, when AUX is transmitting DDC signals. This prevents the AUX signal from being interfered with during standard DP mode and enables I2C DDC signaling during HDMI/DVI mode.

The control input for the conditional pull-up circuit is the Cable Adaptor Detect (CAD) signal. When an HDMI or DVI sink is being used, this signal goes high, which indicates that the AUX line must transmit the DDC signal. When a standard DP sink is being used, the CAD signal goes low, indicating that the AUX line is transmitting its normal AUX signal. In this way, the CAD signal indicates when the AUX/DDC lines need pull-up resistors and when they do not.

The conditional pull-up circuit consists of an inverter, a p-type MOSFET, and two pull-up resistors. The FET acts as a switch between the pull-up resistors. When CAD is high (indicating that pull-up resistors are needed), the inverter outputs a low signal, which brings the Vgs of the FET below the FET's threshold voltage. Pulling Vgs below the threshold voltage turns the p-type FET on. When the FET turns on, it connects the AUX line's pull-up resistors to VCC, which enables them.

The chosen inverter is a Texas Instruments SN74AHC1G04 inverter, which has very fast response times and very good electrical characteristics for V<sub>OH</sub> and V<sub>OL</sub>. The MOSFET chosen is a Texas Instruments TPS1120 (SLVS080). This device has a convenient dual transistor package, an ideal threshold voltage and very low drain-to-source resistance when on. Together, these two devices have a desirable noise margin of 0.9 V.

8.2.4.2.2 CONFIG1 and CONFIG2 Routing

The HD3SS214 only routes the high speed main link, AUX, and Hot Plug Detect (HPD) lines, which means CONFIG1 and CONFIG2 lines need to be routed externally. This is necessary because these lines are important for DP++ as CONFIG1 carries the CAD signal.

A Texas Instruments TS3USB221 (SCDS263) is used to route these signals. It is a 2:1/1:2 USB switch that operates similarly to the HD3SS214. Each port has two inputs, so it is ideal for the CONFIG signals. SRC\_SEL is used to select which source the CONFIG signals are from. The circuit for routing these signals can be seen in Figure 8.

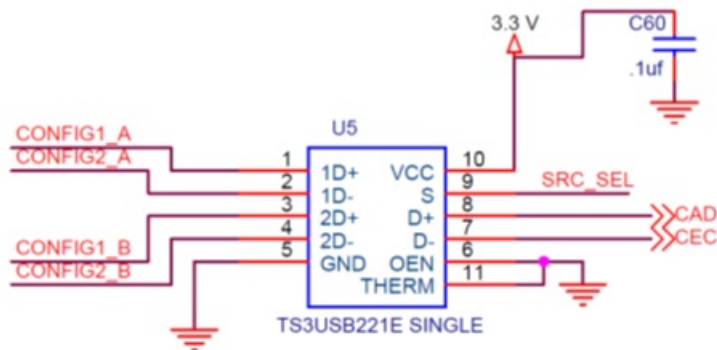


Figure 8. CONFIG Signal Routing

## 9 Power Supply Recommendations

There is no power supply sequence required for HD3SS214. However, it is recommended that OE is asserted high after device supply VDD is stable and in spec. It is also recommended that ample decoupling capacitors are placed at the device VCC near the pin.

## 10 Layout

### 10.1 Layout Guidelines

#### 10.1.1 Layer Stack

Routing the high-speed differential signal traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects from the DisplayPort connectors to the repeater inputs and from the repeater output to the subsequent receiver circuit.

Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.

Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance.

Routing the fast-edged control signals on the bottom layer by prevents them from cross-talking into the high-speed signal traces and minimizes EMI.

If the receiver requires a supply voltage different from the one of the repeater, add a second power/ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also, the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly. Finally, a second power/ground system provides added isolation between the signal layers.

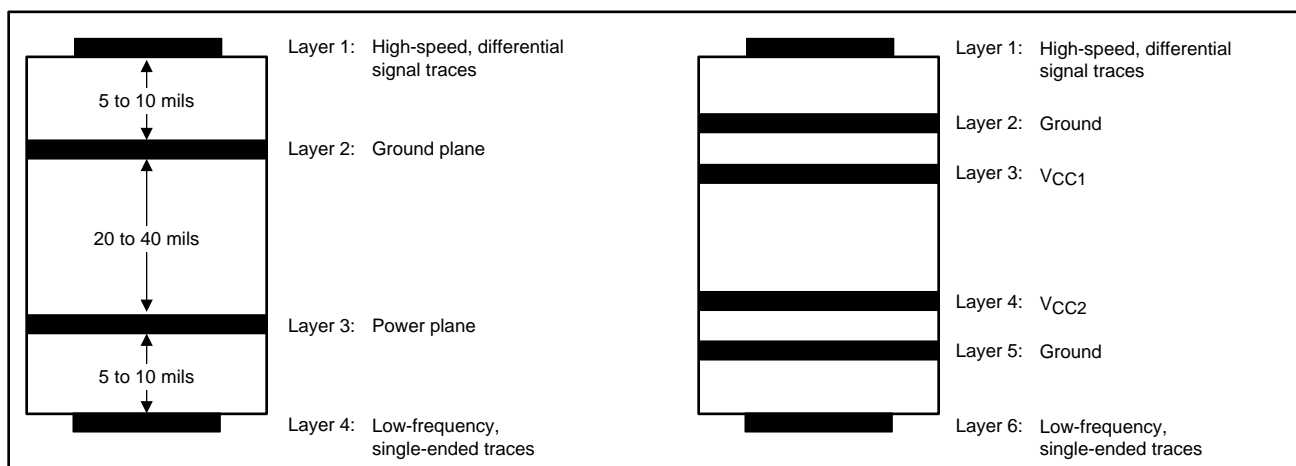


Figure 9. Recommended 4- or 6-Layer (0.062") Stack for a Receiver PCB Design



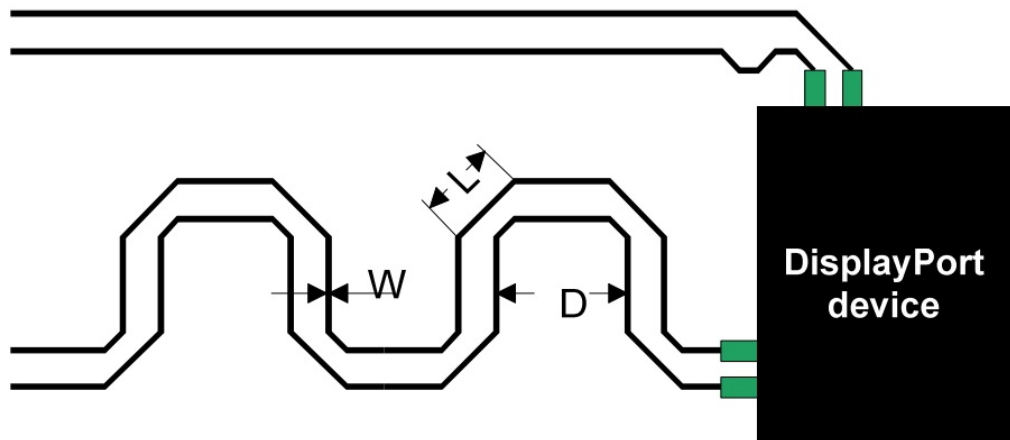
## Layout Guidelines (continued)

### 10.1.2 Differential Traces

Guidelines for routing PCB traces are necessary when trying to maintain signal integrity and lower EMI. Although there seems to be an endless number of precautions to be taken, this section provides only a few main recommendations as layout guidance.

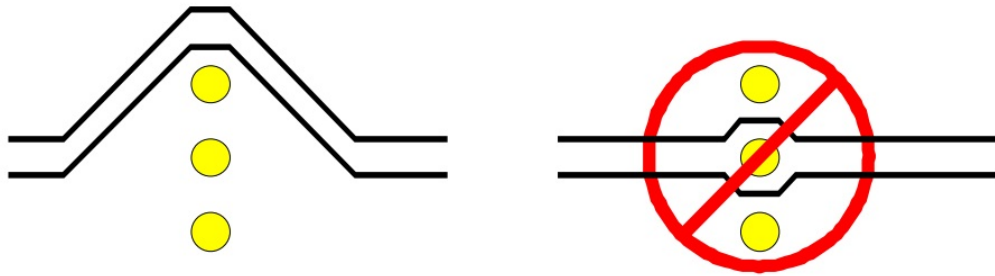
1. Reduce intra-pair skew in a differential trace by introducing small meandering corrections at the point of mismatch.
2. Reduce inter-pair skew, caused by component placement and IC pinouts, by making larger meandering correction along the signal path. Use chamfered corners with a length-to-trace width ratio of between 3 and 5. The distance between bends should be 8 to 10 times the trace width.
3. Use 45 degree bends (chamfered corners), instead of right-angle (90°) bends. Right-angle bends increase the effective trace width, which changes the differential trace impedance creating large discontinuities. A 45° bend is seen as a smaller discontinuity.
4. When routing around an object, route both trace of a pair in parallel. Splitting the traces changes the line-to-line spacing, thus causing the differential impedance to change and discontinuities to occur.
5. Place passive components within the signal path, such as source-matching resistors or ac-coupling capacitors, next to each other. Routing as in case a) creates wider trace spacing than in b), the resulting discontinuity, however, is limited to a far narrower area.
6. When routing traces next to a via or between an array of vias, make sure that the via clearance section does not interrupt the path of the return current on the ground plane below.
7. Avoid metal layers and traces underneath or between the pads off the DisplayPort connectors for better impedance matching. Otherwise they will cause the differential impedance to drop below 75  $\Omega$  and fail the board during TDR testing.
8. Use the smallest size possible for signal trace vias and DisplayPort connector pads as they have less impact on the 100  $\Omega$  differential impedance. Large vias and pads can cause the impedance to drop below 85  $\Omega$ .
9. Use solid power and ground planes for 100  $\Omega$  impedance control and minimum power noise.
10. For 100  $\Omega$  differential impedance, use the smallest trace spacing possible, which is usually specified by the PCB vendor.
11. Keep the trace length between the DisplayPort connector and the DisplayPort device as short as possible to minimize attenuation.
12. Use good DisplayPort connectors whose impedances meet the specifications.
13. Place bulk capacitors (for example, 10  $\mu\text{F}$ ) close to power sources, such as voltage regulators or where the power is supplied to the PCB.
14. Place smaller 0.1  $\mu\text{F}$  or 0.01  $\mu\text{F}$  capacitors at the device.

### 10.2 Layout Example

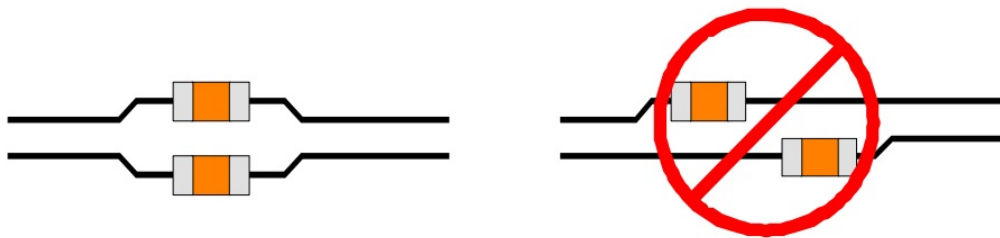


**Figure 10. Skew Seduction via Meandering Using Chamfered Corners**

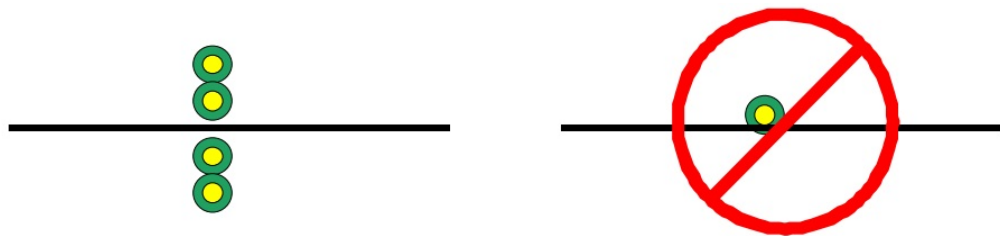
**Layout Example (continued)**



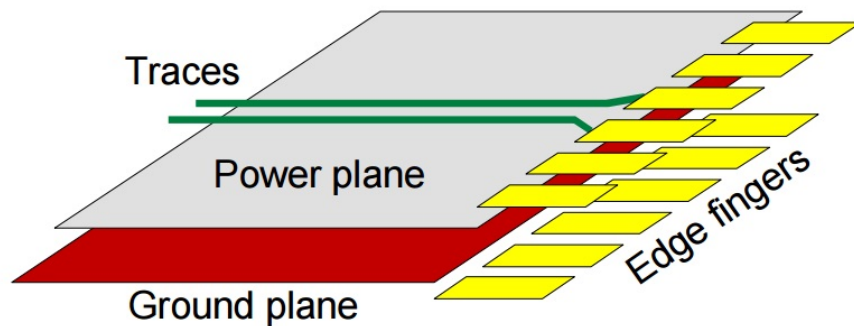
**Figure 11. Routing Around an Object**



**Figure 12. Lumping Discontinuities**



**Figure 13. Avoiding via Clearance Sections**



**Figure 14. Keeping Planes out of the Area Between Edge-fingers**

## 11 器件和文档支持

### 11.1 器件支持

#### 11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

#### 11.2 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com](http://TI.com) 上的器件产品文件夹。请单击右上角的通知我 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

#### 11.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

**TI E2E™ 在线社区** *TI 的工程师对工程师 (E2E) 社区*。此社区的创建目的在于促进工程师之间的协作。在 [e2e.ti.com](http://e2e.ti.com) 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

**设计支持** *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

#### 11.4 商标

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

#### 11.5 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

#### 11.6 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
HD3SS214IZXHR	ACTIVE	NFBGA	ZXH	50	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 105	HD3SS214I	<a href="#">Samples</a>
HD3SS214ZXHR	ACTIVE	NFBGA	ZXH	50	2500	RoHS & Green	SNAGCU	Level-3-260C-168 HR	0 to 70	HD3SS214	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

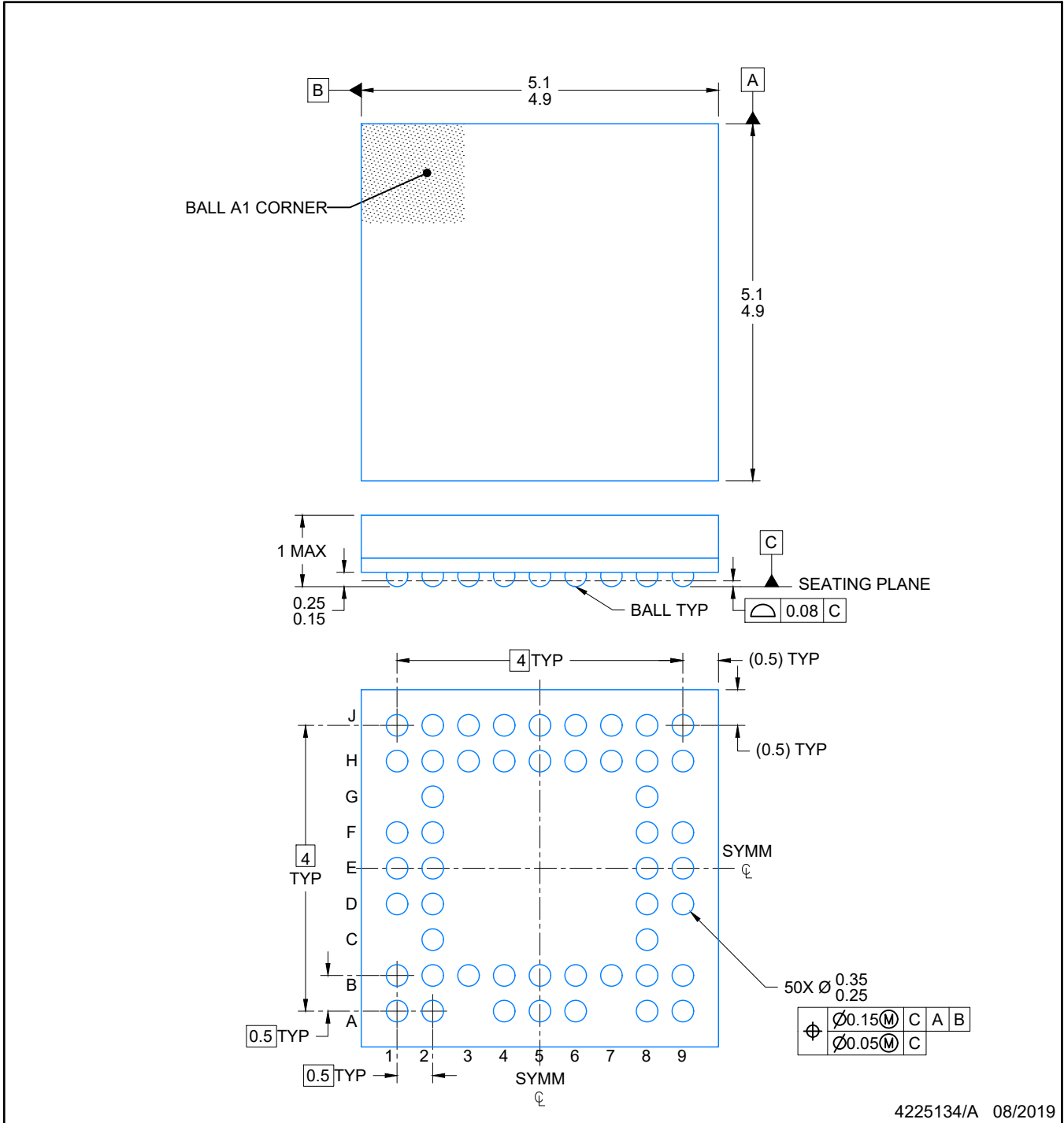

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
HD3SS214IZXHR	NFBGA	ZXH	50	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1
HD3SS214ZXHR	NFBGA	ZXH	50	2500	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
HD3SS214IZXHR	NFBGA	ZXH	50	2500	336.6	336.6	31.8
HD3SS214ZXHR	NFBGA	ZXH	50	2500	336.6	336.6	31.8



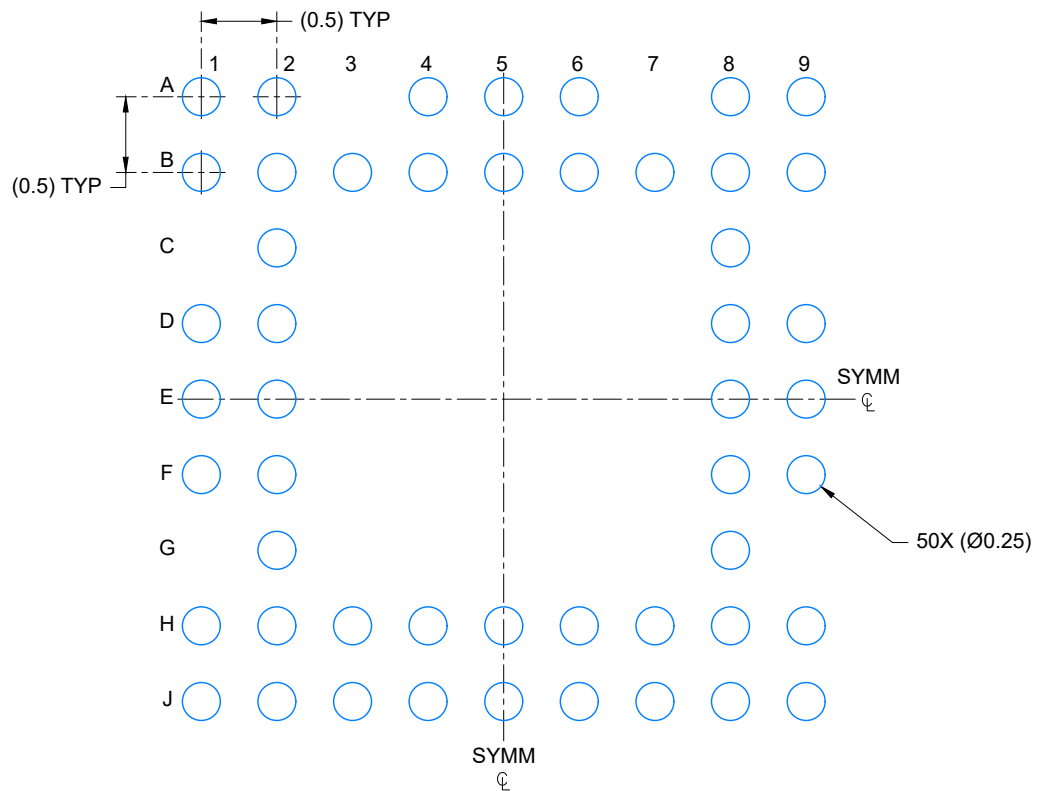
4225134/A 08/2019

NOTES:

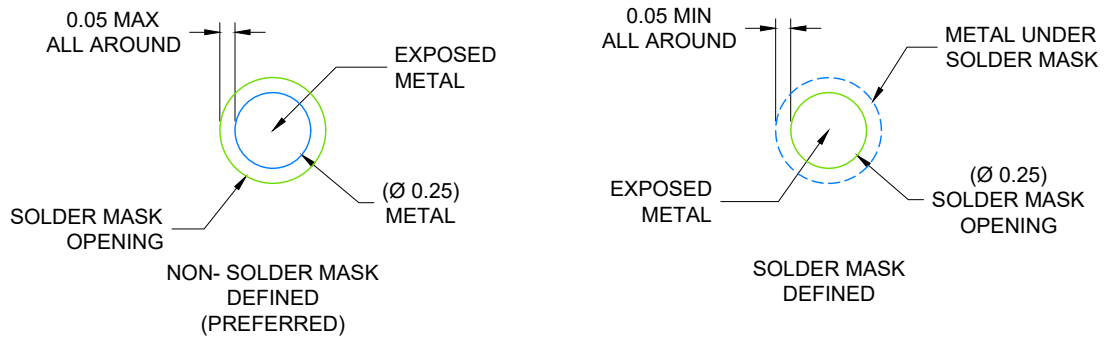
NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.





LAND PATTERN EXAMPLE  
SCALE: 20X

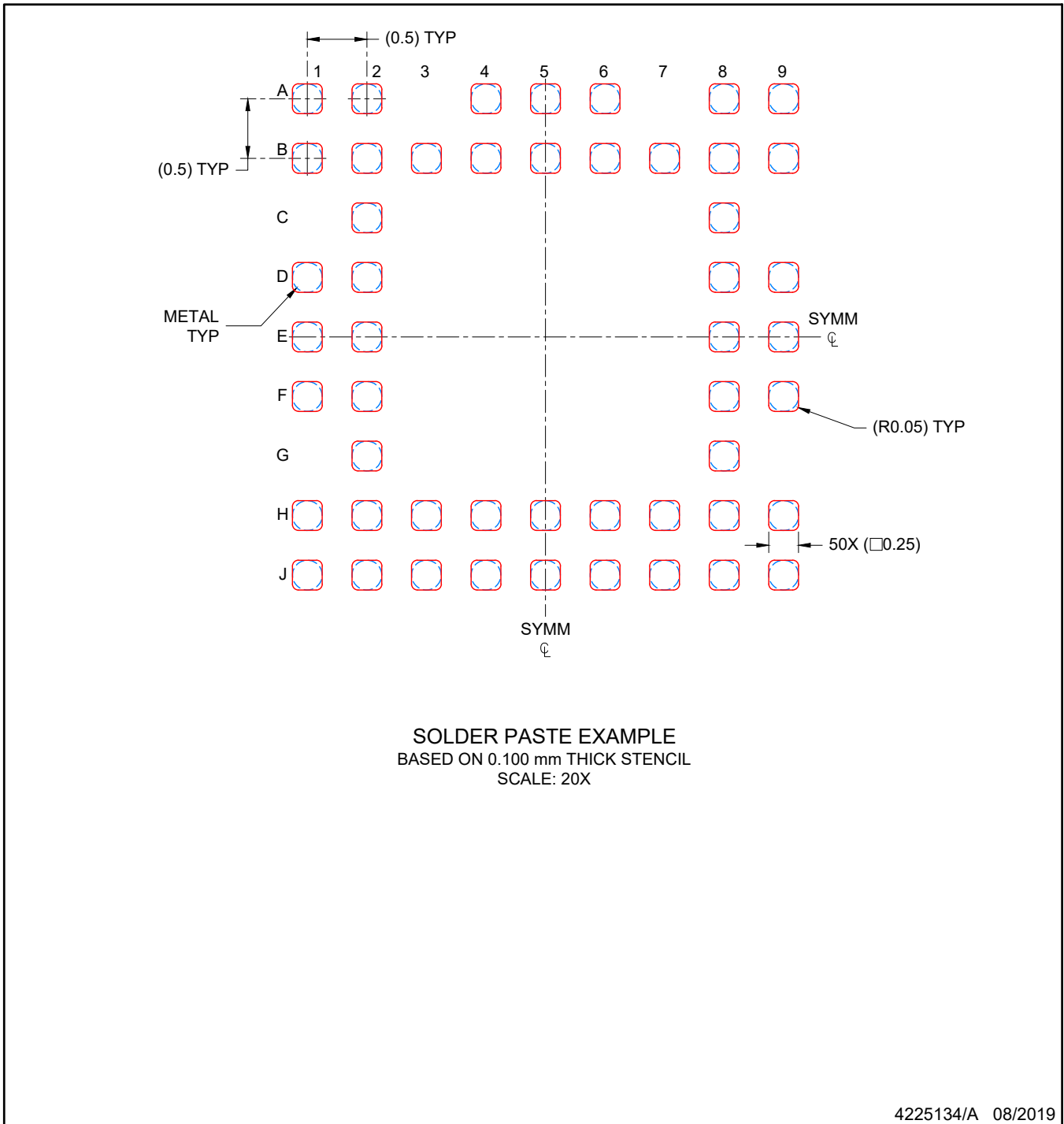


SOLDER MASK DETAILS  
NOT TO SCALE

4225134/A 08/2019

NOTES: (continued)

- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).



NOTES: (continued)

- 4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

## 重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2022，德州仪器 (TI) 公司