DESCRIPTION

The LTC5228 is an advanced CMOS analog switch fabricated in Sub–micron silicon gate CMOS technology. The part also features guaranteed Break Before Make (BBM) switching, assuring the switches never short the driver. The switches can handle negative signal down to - 2V.

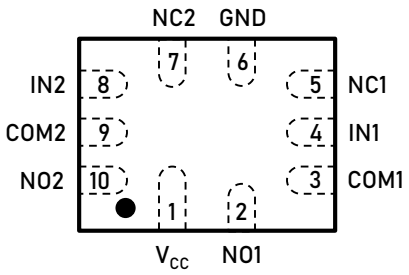
FEATURES

- Low R_{ON}: 0.4 Ω @ V_{CC} = 3 V Typically
- Wide Supply Voltage Range: 1.65 V ~ 5.5 V
- Full -2 V ~ V_{CC} Signal Handling Capability
- High Off - Channel Isolation
- Low Standby Current
- Low Distortion
- Break-Before-Make (BBM) Switching
- High Continuous Current Capability: ±300 mA Through Each Switch
- Applications in
  - Cell Phone Audio Block
  - Speaker and Earphone Switching Ring-Tone Chip
  - Amplifier Switching
  - Modems
- Available Packages: QFN1.8×1.4-10L, MSOP-10L

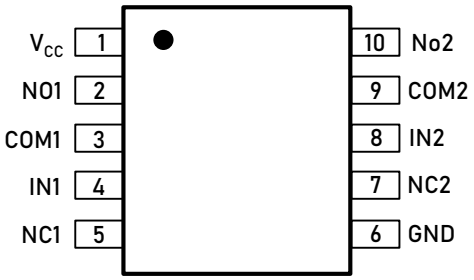
Order Information

Model	Package	Ordering Number Note1	Packing Option
LTC5228	QFN1.8×1.4-10L	LTC5228YFS10	Tape and Reel, 3000
	MSOP-10L	LTC5228YV10	Tape and Reel, 4000

PIN CONFIGURATION (Top View)



QFN 1.8 X 1.4-10L



MSOP-10L

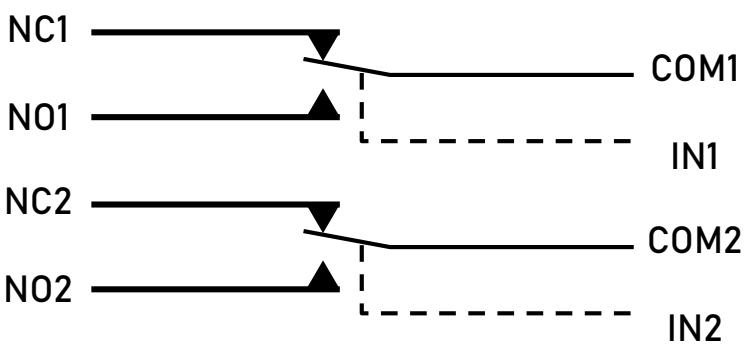
PIN DESCRIPTIONS

Pin	Symbol	Description
1	V_{CC}	Power Supply
2	NO1	Independent Channels
3	COM1	Common Channels
4	IN1	Controls
5	NC1	Independent Channels
6	GND	Ground
7	NC2	Independent Channels
8	IN2	Controls
9	COM2	Common Channels
10	NO2	Independent Channels

TRUTH TABLE

IN1, IN2	NO1, NO2	NC1, NC2
0	OFF	ON
1	ON	OFF

Analog Symbol



RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Min	Max	Unit
DC Supply Voltag	V_{CC}	1.65	5.5	V
Digital Select Input Voltage	V_{IN}	GND	5.0	V
Analog Input Voltage	V_{IS}	-2.0	VCC	V
Operating Temperature Range	T_A	-45	+85	℃
Input Rise or Fall Time , SELECT	t_R t_F	0	20	ns/V

RECOMMENDED OPERATING CONDITIONS

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	-0.5 to +6.0	V
Analog Input Voltage	V_{IS}	-2.5 ~ V_{CC} + 0.3 $\|V_{CC} - V_{IS}\| < 6.5$ V	V
Digital Select Input Voltage	V_{IN}	-0.5 to + 6.0	V
Output Voltage	V_{OUT}	-2.5 ~ V_{CC} + 0.3 $\|V_{CC} - V_O\| < 6.5$ V	V
Continuous DC Current from COM to NC/NO	I_{an1}	±300	mA
Peak Current from COM to NC/NO, 10 duty cycle (Note 1)	$I_{an1-pk1}$	±500	mA
Continuous DC Current into COM/NO/NC with respect to V_{CC} or GND	I_{dmp}	±100	mA

Stresses beyond those listed under “Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1. Defined as 10% ON, 90% OFF duty cycle.

Functional Description

This integrated circuit can be damaged by ESD if you don't pay attention to ESD protection. Linearin recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Linearin reserves the right to make any change in circuit design, specification or other related things if necessary without notice at any time. Please contact Linearin's sales office to get the latest data sheets.

Output Capacitor

Symbol	Parameter	Test Conditions	V_{CC} ± 10% (V)	T_A = 25°C			Unit
				Min	Typ	Max	
V_{IH}	High-Level Input Voltage, Select Inputs		1.65 ~ 5.5	0.4V_{CC}			V
V_{IL}	Low-Level Input Voltage, Select Inputs		1.65 ~ 5.5			0.5	V
I_{IN}	Maximum Input Leakage Current, Select Inputs	V_{IN} = V_{CC} or GND	5			±0.3	µA
I_{off}	Power Off Leakage Current	V_{IN} = 4.3 V	0			±0.5	µA
I_{CO}	Maximum Quiescent Supply Current (Note 2)	Select, V_{IS} = V_{CC} or GND	3.6			1.0	µA
I_{CCT}	Increase in I_{CC} per input	IN1 = 2.6 V, IN2 = 0 V or IN2 = 2.6 V, IN1 = 0 V	4.3		1.5		µA
		IN1 = 1.8 V, IN2 = 0 V or IN2 = 1.8 V, IN1 = 0 V			4.5		µA
$I_{COM\ (ON)}$	COM ON Leakage Current (Note 3)	V_{IN} = V_{IL} or V_{IH}, V_{NO} = 0.3 V OR 4.7 V V_{NC} Floating V_{NO} = 0.3 V OR 4.7 V V_{NO} Floating V_{COM} = 0.3 V OR 4.7 V	5.0	-20		20	nA
Ron	On-Resistance (Note 2) (Note 3)	V_{IS} = 0.7 V, 3.6 V, 4.3 V I_{IN} = 100 mA	4.3		0.3		Ω
		V_{IS} = 0.7 V, 2.3 V, 3.0 V I_{IN} = 100 mA	3.0		0.4	0.8	
Rflat	On-Resistance Flatness (Note 2) (Note 3) (Note 5)	I_{COM} = 100 mA V_{IS} = GND to Vcc	5.0			0.3	Q
△Ron	On-Resistance Match Between Channels (Note 2) (Note 3) (Note 4)	I_{COM} = 100 mA, V_{IS} = 1.5 V	5.0		0.25		Q

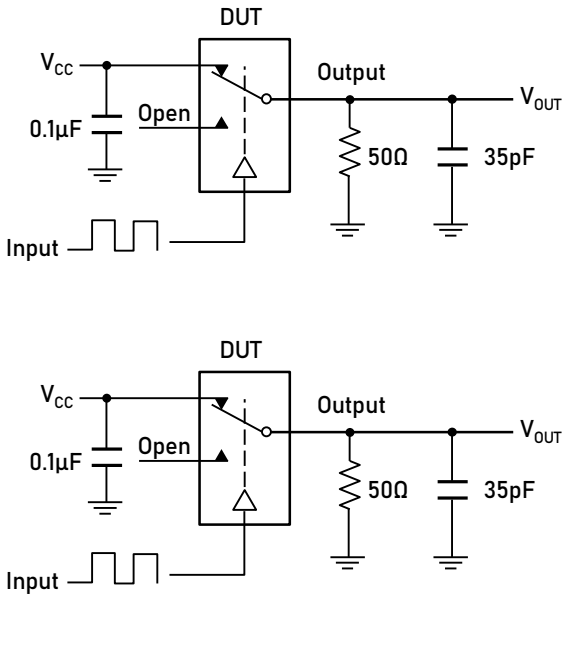
Electrical Characteristics

Symbol	Parameter	Test Conditions	V_{CC} ± 10% (V)	T_A = 25C			Unit
				Min	Typ	Max	
t_{ON}	Turn-On Time (Figure 1)	V_{IS} = 1.5 V	2.5 ~ 3.3		35	45	ns
			3.3 ~ 5.5		25	30	
t_{OFF}	Turn-Off Time (Figure 1)	V_{IS} = 1.5 V	2.5 ~ 3.3		17	20	ns
			3.6 ~ 5.5		15	20	
t_{BBM}	Break-Before-MakeTime (Note6)(Figure 2)	C_L= 35 pF R_{IS} = 50 Ω V_{IS} = 1.5 V	2.5 ~ 3.3	7	9		ns
			3.6 ~ 5.5	4	6		
BW	On-Channel, -3 dB Bandwidth Frequency Response (Figure 4)				55		MHz
	R_{IS} = 50 Ω						
O_{ISO}	Off-Channel Isolation (Figure 5)				-70		dB
	F_{IS} = 100 kHz, V_{IN} = GND to V_{CC}, C_L = 5 pF, R_L = 50 Ω, V_{IS} = IV_{RMS}						
Q	Charge Injection Select Input to Common I/O (Figure 3)				25		pC
	V_{IN} = 0 or V_{CC}, R_{IS} = 0 Ω, C_L = 100 pF, R_L = 1 mΩ, Q = C_L x ΔV_{OUT}						
THD	Total Harmonic Distortion THD +Noise		3.6		0.06		%
	F_{IS} = 20 Hz to 20 kHz, R_L = 600Ω, C_L = 50 pF, V_{IS} = 2 V_{RMS}						
X_{TALK}	Channel-to-Channel Crosstalk (Figure 6)		3.6 ~ 5.0		-72		dB
	F_{IS} = 100 KHZ, V_{IN} = GND TO V_{CC}, R_L = 50 Ω, C_L = 5 PF, V_{IS} = 1 V_{RMS}						
C_{IN}	Control Pin Input Capacitance		3.6		3.5		pF
C_{CN}/C_{NO}	NC/NO Port Capacitance		3.6		50		pF
C_{COM}	COM Port Capacitance When Switch is Enabled		3.6		120		pF

Note:

2. Guaranteed by design.
3. Guaranteed by design. Resistance measurements do not include test circuit or package resistance.
4. ΔR_{ON} = $R_{ON\ (MAX)}$ - $R_{ON\ (MIN)}$ between NC1 and NC2 or between NO1 and NO2.
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal ranges.
6. Guaranteed by design in -40°C.

TEST CIRCUITS



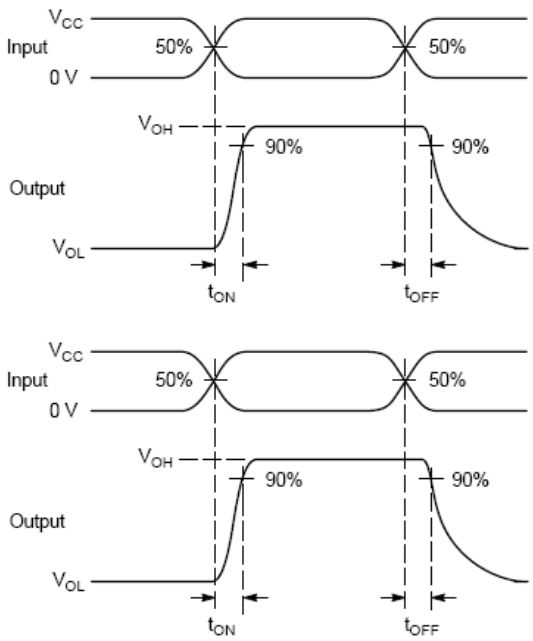
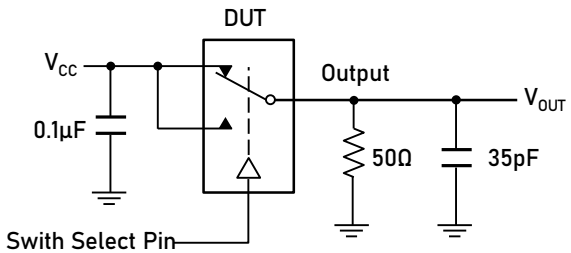


Figure 1. t_{ON}/t_{OFF}



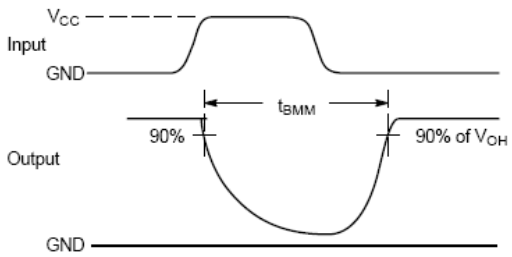
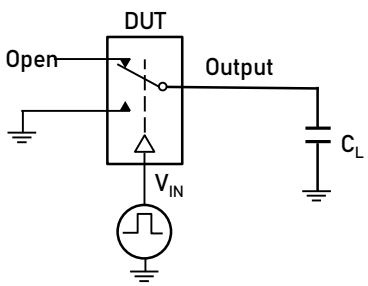


Figure 2. t_{BBM}



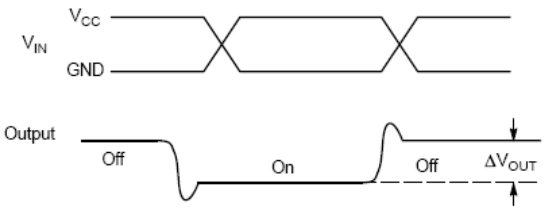


Figure3: Charge Injection

TEST CIRCUITS (Cont.)

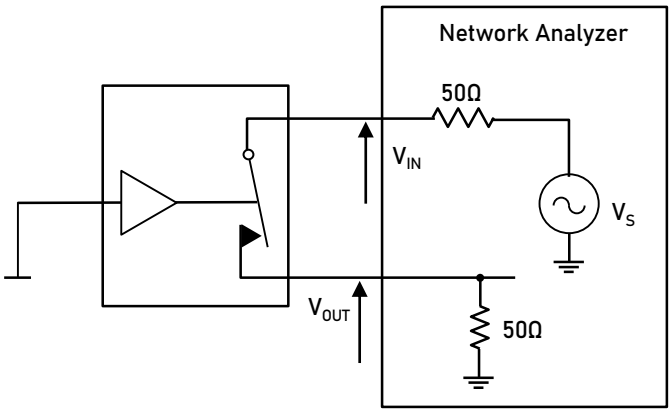
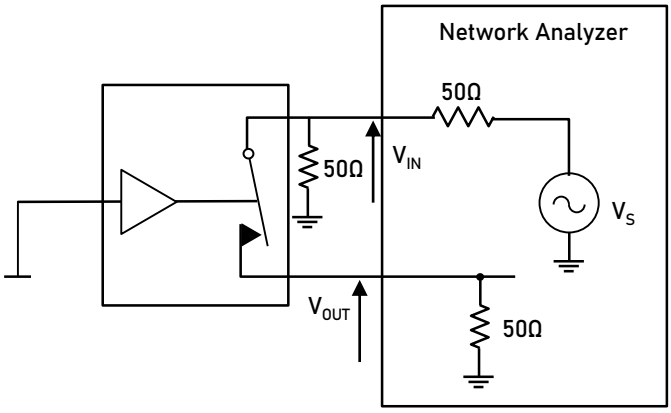
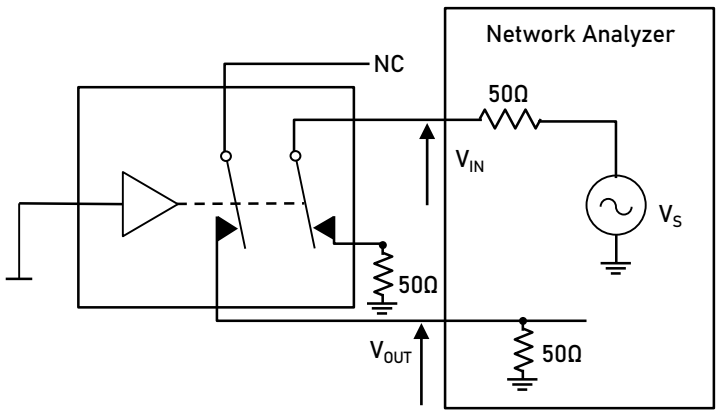


Figure4: Bandwidth



Off -Isolation = 20 Log (V_{OUT}/ V_{IN})

Figure5: Channel Off Isolation

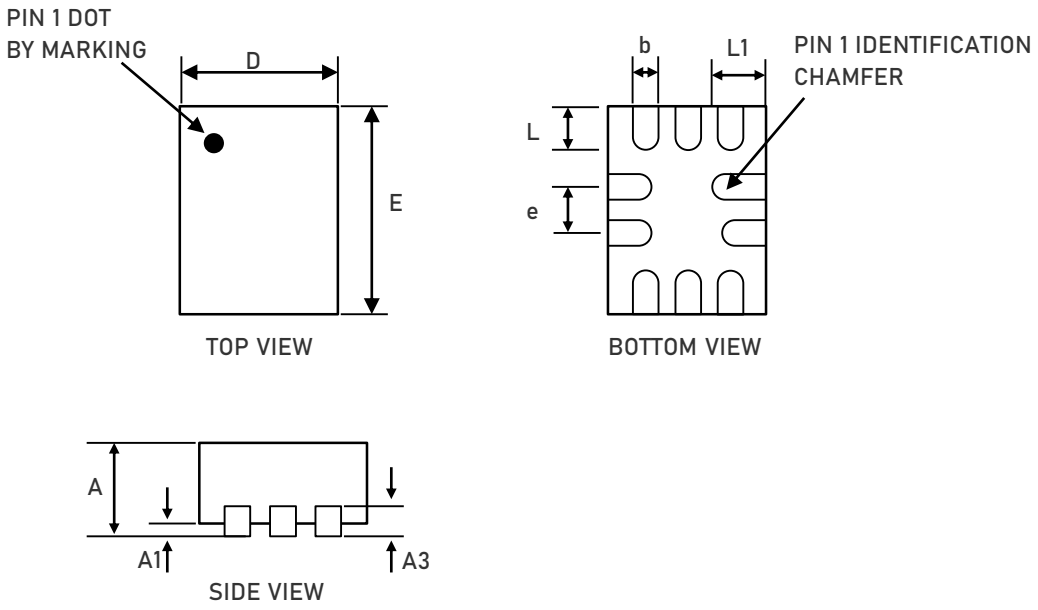


CROSSTALK = 20 Log (V_{OUT}/ V_{IN})

Figure6: Non-Adjacent Channel-to-Channel Crosstalk

PACKAGE OUTLINE

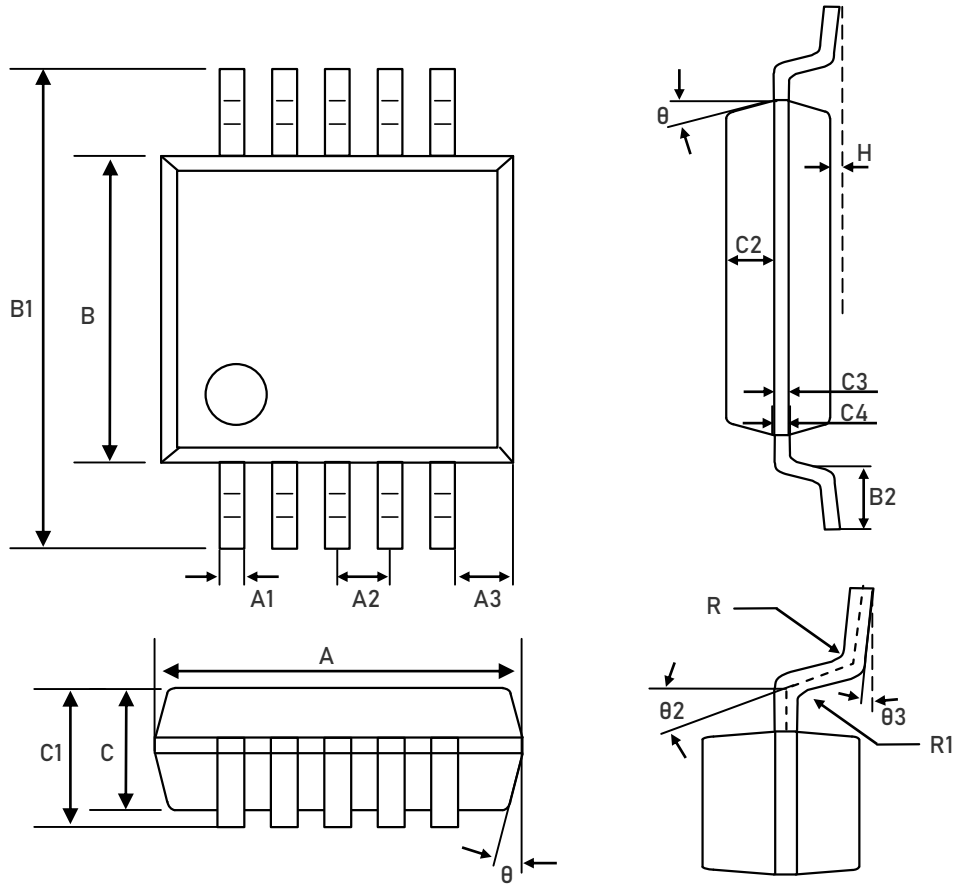
QFN1.8×1.4-10L



Dimensions In Millimeters (mm)			
Symbol	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.000		0.050
A3	0.15 REF		
D	1.350	1.400	1.450
E	1.750	1.800	1.850
b	0.150	0.200	0.250
L	0.300	0.400	0.500
L1	0.400	0.500	0.600
e	0.40 BSC		

PACKAGE OUTLINE

MSOP-10L



Symbol	Dimensions In Millimeters (mm)		Symbol	Dimensions In Millimeters (mm)	
	Min.	Max.		Min.	Max.
A	2.90	3.10	C3	0.152	
A1	0.18	0.25	C4	0.15	0.23
A2	0.50 TYP		H	0.00	0.09
A3	0.40 TYP		θ	15°TYP4	
B	2.90	3.10	θ1	12°TYP4	
B1	4.70	5.10	θ2	14°TYP	
B2	0.45	0.75	θ3	0° ~ 6°	
C	0.75	0.95	R	0.15TYP	
C1	-	1.100	R1	0.15TYP	
C2	0.328 TYP				