

Features

- ESD Protect for 1 Line with Bi-directional
- Provide ESD protection for the protected line to IEC 61000-4-2 (ESD) ±15kV (air/contact)
 IEC 61000-4-4 (EFT) 50A (5/50ns)
 Cable Discharge Event (CDE)
- 0402 small DFN package saves board space
- Protect one I/O line or one power line
- Fast turn-on and Low clamping voltage
- For low operating voltage applications: 5V maximum
- Solid-state silicon-avalanche and active circuit triggering technology
- Green Part

Applications

- Mobile Phones
- Hand Held Portable Applications
- Computer Interfaces Protection
- Microprocessors Protection
- Serial and Parallel Ports Protection
- Control Signal Lines Protection
- Power lines on PCB Protection
- Latchup Protection

Description

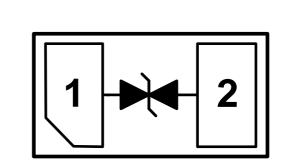
AZ5725-01F is a design which includes one Bi-directional ESD rated clamping cell to protect one power line, or one control line, or one low speed data line in an electronic systems. The AZ5725-01F has been specifically designed to protect sensitive components which are connected to power and control lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD), Electrical Fast Transients (EFT), and Cable Discharge Event (CDE).

AZ5725-01F is a unique design which includes

proprietary clamping cell in a single package. During transient conditions, the proprietary clamping cell prevents over-voltage on the power line or control/data lines, protecting any downstream components.

AZ5725-01F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge)

Circuit Diagram / Pin Configuration



DFN1006P2X (Bottom View) (1.0mm x 0.6mm x 0.45mm)

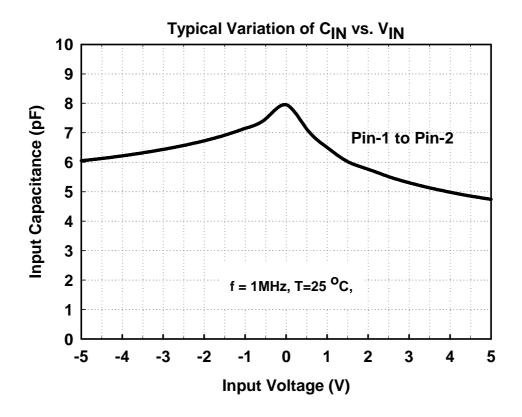
SPECIFICATIONS

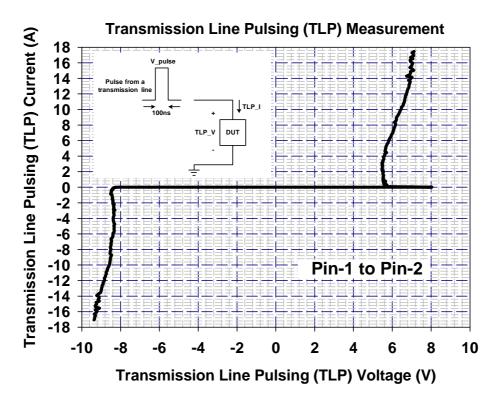
| ABSOLUTE MAXIMUM RATINGS | | | |
|---------------------------------|------------------|---------------|-------|
| PARAMETER | SYMBOL | RATING | UNITS |
| Operating Supply Voltage | V _{DC} | ±5.5 | V |
| ESD per IEC 61000-4-2 (Air) | V _{ESD} | ±15 | kV |
| ESD per IEC 61000-4-2 (Contact) | | ±15 | |
| Lead Soldering Temperature | T _{SOL} | 260 (10 sec.) | °C |
| Operating Temperature | T _{OP} | -55 to +85 | °C |
| Storage Temperature | T _{STO} | -55 to +150 | ℃ |

| ELECTRICAL CHARACTERISTICS | | | | | | |
|------------------------------|---------------------|--|-----|-----|-----|-------|
| PARAMETER | SYMBOL | CONDITIONS | | TYP | MAX | UNITS |
| Stand-Off Voltage | V _{RWM} | T=25 °C. | -5 | | 5 | V |
| Leakage Current | l _{Leak} | V _{RWM} =±5V, T=25 °C. | | | 1 | μΑ |
| Breakdown Voltage | V_{BV} | I _{BV} = 1mA, T=25 °C. | 5.8 | | 9.0 | V |
| ESD Clamping Voltage | V _{ESD_CL} | IEC 61000-4-2 +6kV, T=25 °C, Contact mode. | | 10 | | V |
| Channel Input Capacitance | C _{IN} | V_R = 0V, f = 1MHz, T=25 °C. | | 8 | 10 | pF |



Typical Characteristics







Applications Information

The AZ5725-01F is designed to protect one line against System ESD/EFT/Cable-Discharge pulses by clamping it to an acceptable reference. It provides bi-directional protection.

The usage of the AZ5725-01F is shown in Fig. 1. Protected line, such as data line, control line, or power line, is connected at pin 1. The pin 2 is connected to a ground plane on the board. Since AZ5725-01F is b-directional, these connections can be reversed (protected line to pin 2, ground to pin 1). In order to minimize parasitic inductance in the board traces, all path lengths connected to the pins of AZ5725-01F should be kept as short as possible.

In order to obtain enough suppression of ESD induced transient, good circuit board is critical. Thus, the following guidelines are recommended:

- Minimize the path length between the protected lines and the AZ5725-01F.
- Place the AZ5725-01F near the input terminals or connectors to restrict transient coupling.
- The ESD current return path to ground should be kept as short as possible.
- Use ground planes whenever possible.
- NEVER route critical signals near board edges and near the lines which the ESD transient easily injects to.

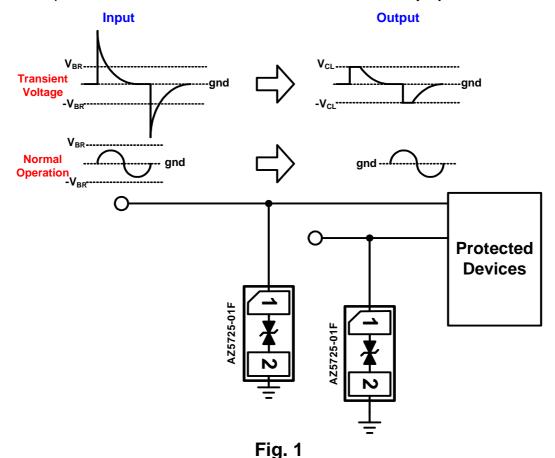


Fig. 2 shows another simplified example of using AZ5725-01F to protect the control line, low speed

data line, and power line from ESD transient stress.

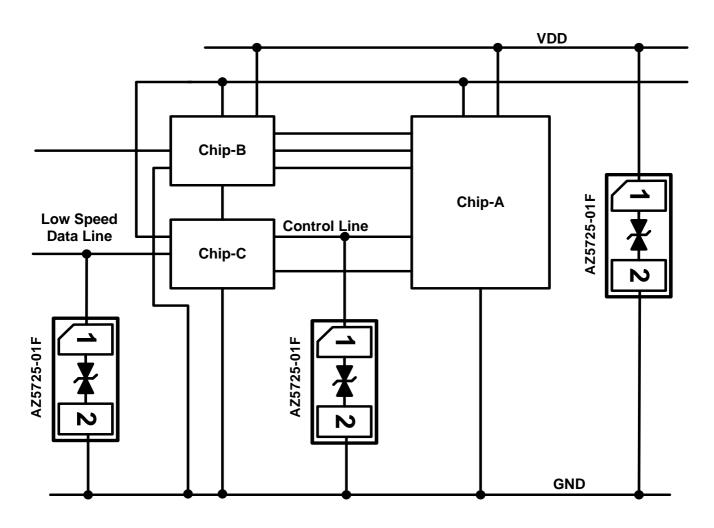
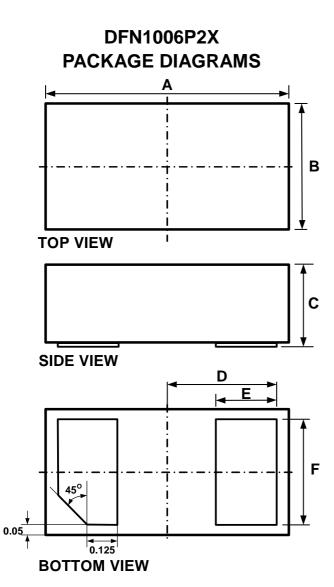


Fig. 2

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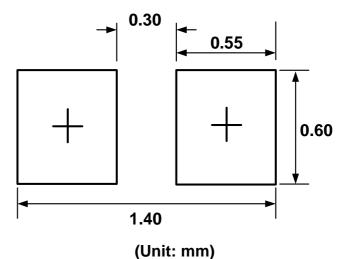


Mechanical Details



| Symbol | Millim | neters | Inches | | |
|--------|--------|--------|--------|-------|--|
| Symbol | min | max | min | max | |
| Α | 0.95 | 1.05 | 0.037 | 0.041 | |
| В | 0.55 | 0.65 | 0.022 | 0.026 | |
| С | 0.41 | 0.50 | 0.016 | 0.020 | |
| D | 0.45 | | 0.018 | | |
| E | 0.20 | 0.30 | 0.008 | 0.012 | |
| F | 0.45 | 0.55 | 0.018 | 0.022 | |

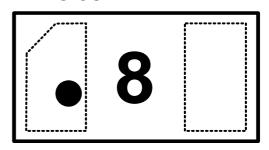
LAND LAYOUT



Notes:

This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



Top View

| Part Number | Marking Code |
|--------------|--------------|
| AZ5725-01F | 0 |
| (Green Part) | 0 |

Note: Green means Pb-free, RoHS, and Halogen free compliant.



Ordering Information

| PN# | Material | Type | Reel size | MOQ | MOQ/internal box | MOQ/carton |
|-----------------|----------|------|-----------|-------------|-------------------|----------------------|
| AZ5725-01F.R7GR | Green | T/R | 7 inch | 12,000/reel | 4 reel=48,000/box | 6 box=288,000/carton |

Revision History

| Revision | Modification Description | | |
|---------------------|----------------------------------|--|--|
| Revision 2011/10/27 | Formal Release. | | |
| Revision 2012/01/18 | Add the Ordering Information. | | |
| Revision 2015/01/29 | Update the Ordering Information. | | |
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