160A-M

4/3-Type, 16.78-mega pixel CMOS Image Sensor

The specifications are subject to change without notice.

General Description

The 160A-M is a 4/3-type 16.78-megapixel high resolution CMOS image sensor, the frame rate is up to 46.8fps at full resolution of 4096 (H) x 4096 (V). Sensors is featured with global shutter pixels, high-resolution ADC and high-speed readout. The sensors meet the high-performance and high-resolution requirements in applications such as intelligent traffic system, machine vision and high-resolution industrial inspection, etc.

Features

- Active pixel array
  160A-M 4112 (H) × 4112 (V)
  14.34mm (H) × 14.34 mm (V), 20.27mm

- Global shutter pixel
- Programmable analog gain and digital gain
- 14-bit ADC
- Master mode, Slave mode and TRIGEXP mode
- External electronic shutter control (only in TRIGEXP mode)
- Other functions
  Multi-ROI (V-direction only)
  Vertical/Horizontal binning
  Vertical/Horizontal sub-sampling
  Vertical/Horizontal normal and inverted readout mode

Specifications

Table 1. Sensor specifications

Parameters	Specifications
Image Format	160A-M: 4/3-Type, diagonal 20.27mm
Number of Total Pixels	160A-M: 4336 (H) x 4184 (V)
Number of Active Pixels	160A-M: 4112 (H) x 4112 (V)
Pixel Size	3.5µm x 3.5µm
Pixel Type	Global shutter pixel
Sensitivity	T.B.D. (> 2V/lux·s)
Saturation (Linear)	T.B.D. (> 0.9V)
Dynamic Range	T.B.D.
Read noise (with Pixel)	T.B.D.
Windowing (ROI)	V-direction only with multi-ROI
ADC Resolution	14bit
Frame Rate	Maximum frame rate at full resolution 160A-M: 46.8fps
LVDS Outputs	16 LVDS pairs
Data Rate	Max. 800 Mbps/pair
Power Supply	1.2V/1.8V/3.3V
Power Consumption	T.B.D
Chroma	Mono and Color
Type of Package	230 pin LGA

Applications

- Intelligent traffic system
- Machine vision
- High resolution industrial inspection

Contents

Block Diagram

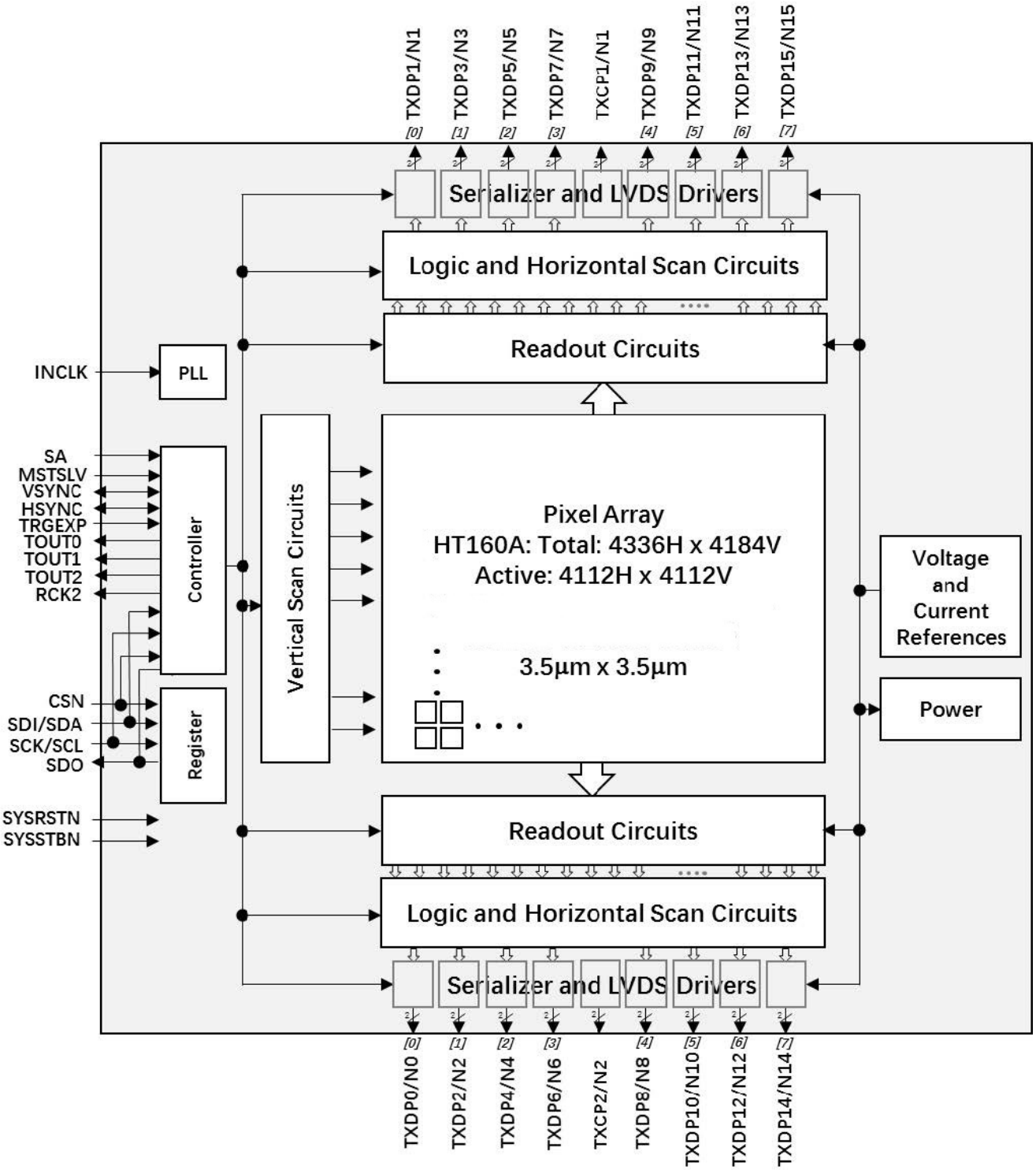


Figure 1. Block Diagram

Pixel Array

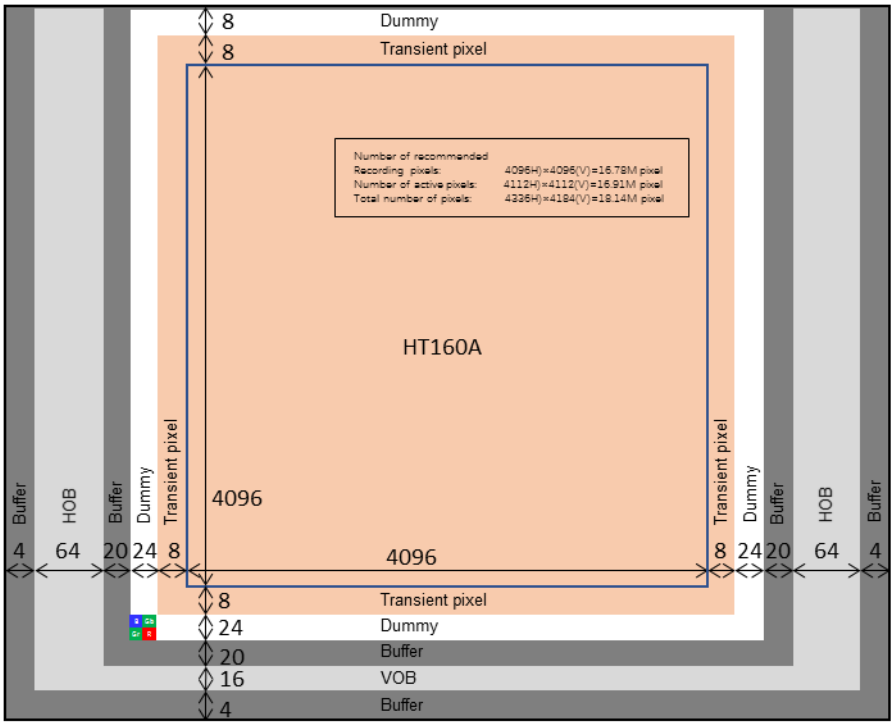


Figure 2. 160A-M Pixel Array

Pixel arrangement at corners

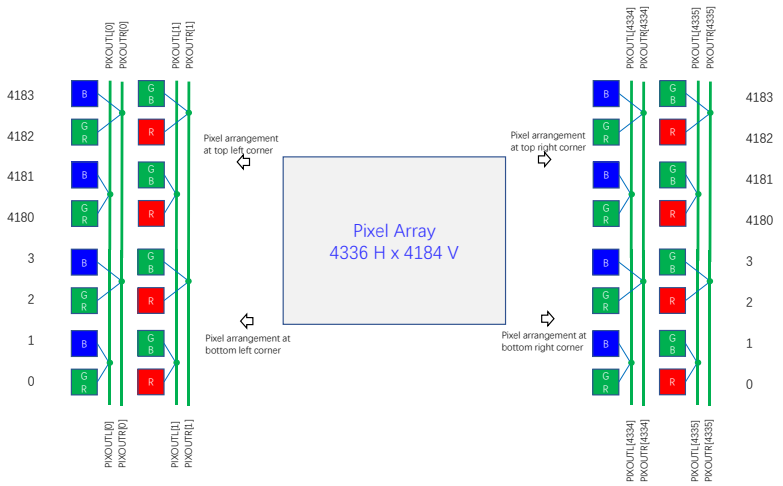


Figure 4. Pixel arrangement at corner

Pixel arrangement at center

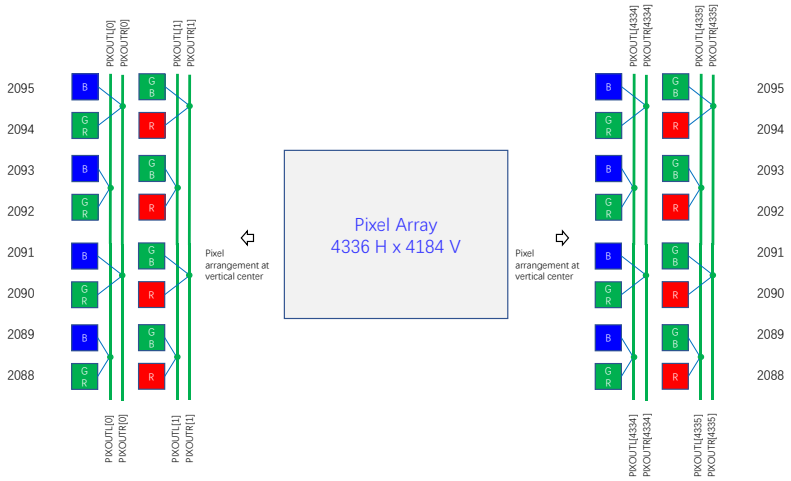


Figure 5. Pixel arrangement at vertical center

Pin Arrangement

	U	T	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A
1	NC	U1	NC	DTSTL0	VSYNC	VDD12T	SDO	SA	VDD12T	VSS12T	VDD12T	TOUT0	DTSTR0	NC6	NC	NC	A1
2			NC	DTSTL1	HSYNC	VSS12T	CSN	NC	VSS12T	VSS12T	VSS12T	TOUT2	DTSTR1	VDD12T	VNSUB		
3	NC	TXDN6	TXDP6	NC	TRGEXP	SDI	SCK	SYSRSTN	MSTSLV	SYSSTBN	TOUT1	NC	NC	VSSR	VSSR	NC	VRP_T
4	TXDN4	TXDP4	TXDN2	TXDP2	NC	VSSA1	VSSP	VSSA1	VSSA1	VSSP	VSSP	NC	VSSP	NC	VSSR	VDDR	VRA0_T
5	TXCN1	TXCP1	TXDN0	TXDP0	VSS18L	VDDA1	VDDP	NC	VDDA1	VDDP	VDDP	VDDCH	VSSP	NC	VSSR	VDDR	VRA1_T
6	TXDN1	TXDP1	TXDN3	TXDP3	VSS18L	VSS12L						TX2H	VSSP	RSL	VDDCL	NC	VRA2_T
7	TXDN5	TXDP5	TXDN7	TXDP7	VSS18L	VDD18						RSH	VSSP	VSSR	VIREF	TX1L	VSSR
8	VSS12L	ATST2	VSS18L	VSS18L	VDD18L	VSS12L			Top View			TX1H	VSSP	VSSR	VSSR	TX2L	GRSTL
9	INCLK	NC	VSS18L	VSS18L	VDD18L	VDD12L						GRSTH	VSSP	ATSTIN	VSSR	VDDR	VSSR
10	TXDN12	TXDP12	TXDN14	TXDP14	VSS18L	VDD12D						NC	VSSP	VSSCP	VCP1	ATST1	VRA2_B
11	TXDN8	TXDP8	TXDN10	TXDP10	VSS18L	VSS12D						VDDP	VSSP	VSSCP	VCP1IN	ATST0	VRA1_B
12	TXCN2	TXCP2	TXDN9	TXDP9	VSS18L	VDDA2	NC	VDDP	VDDA2	NC	NC	VR_EXTS	VR_EXTR	VCP2	VSSCP	VDDCP	VRA0_B
13	TXDN13	TXDP13	TXDN11	TXDP11	NC	VSSA2	NC	VSSP	VSSA2	VSSA2	NC	NC	NC	VCP2IN	NC	NC	VRP_B
14	NC	TXDN15	TXDP15	NC2	NC3	NC	NC	NC	NC	NC	NC	NC	VDD12CP	VSSCP	VSSCP	NC	NC
15	U16		NC1	DTSTL4	NC4	VSS12B	NC	VSS12B	NC	VSS12B	NC	VSS12B	DTSTR4	VDD12CP	VDDCP	A16	
16	NC		RCK2	DTSTL3	NC5	VDD12B	NC	VDD12B	NC	VDD12B	NC	VDD12B	DTSTR3	NC	NC	NC	

Figure 6. Package pin arrangement (Top View)

Pin Descriptions

#	PIN#	I/O	A/D	PIN Function	Description
1	A1	-	-	NC	-
2	A3	I	A	VRP_T	Voltage reference input for read-out circuits
3	A4	I	A	VRA0_T	Voltage reference input for read-out circuits
4	A5	I	A	VRA1_T	Voltage reference input for read-out circuits
5	A6	I	A	VRA2_T	Voltage reference input for read-out circuits
6	A7	GND	A	VSSR	3.3V analog ground
7	A8	I	A	GRSTL	Pixel driving signal low level voltage power supply
8	A9	GND	A	VSSR	3.3V analog ground
9	A10	I	A	VRA2_B	Voltage reference input for read-out circuits
10	A11	I	A	VRA1_B	Voltage reference input for read-out circuits
11	A12	I	A	VRA0_B	Voltage reference input for read-out circuits
12	A13	I	A	VRP_B	Voltage reference input for read-out circuits
13	A14	-	-	NC	-
14	A16	-	-	NC	-
15	B3	-	-	NC	-
16	B4	PWR	A	VDDR	3.3V analog power supply
17	B5	PWR	A	VDDR	3.3V analog power supply
18	B6	-	-	NC	-
19	B7	I/O	A	TX1L	Pixel driving signal low level voltage power supply, connect to 10uF+0.1uF to GND
20	B8	I/O	A	TX2L	Pixel driving signal low level voltage power supply, connect to 10uF+0.1uF to GND
21	B9	PWR	A	VDDR	3.3V analog power supply
22	B10	O	A	ATST1	analog test output
23	B11	O	A	ATST0	analog test output
24	B12	PWR	A	VDDCP	3.3V analog power supply
25	B13	-	-	NC	-
26	B14	-	-	NC	-
27	C1	-	-	NC	-
28	C2	PWR	A	VNSUB	Chip substrate potential, 3.3V.
29	C3	GND	A	VSSR	3.3V analog ground
30	C4	GND	A	VSSR	3.3V analog ground
31	C5	GND	A	VSSR	3.3V analog ground
32	C6	GND	A	VDDCL	Pixel driving signal low level voltage power supply, connect to 2.2uF+0.1uF to GND
33	C7	O	A	VIREF	Connect to analog ground through a 62k resistance.
34	C8	GND	A	VSSR	3.3V analog ground
35	C9	GND	A	VSSR	3.3V analog ground
36	C10	O	A	VCP1	charge pump output，connect to VCP1IN and 22uF+0.1uF to GND
37	C11	I	A	VCP1IN	LDO power supply, connect to VCP1
38	C12	GND	A	VSSCP	3.3V analog ground
39	C13	-	-	NC	-
40	C14	GND	A	VSSCP	3.3V analog ground
41	C15	PWR	A	VDDCP	3.3V analog power supply
42	C16	-	-	NC	-
43	D1	-	-	NC	-
44	D2	PWR	D	VDD12T	Digital power supply, 1.2V
45	D3	GND	A	VSSR	3.3V analog ground

46	D4	-	-	NC	-
47	D5	-	-	NC	-
48	D6			RSL	Pixel driving signal low level voltage power supply
49	D7	GND	A	VSSR	3.3V analog ground
50	D8	GND	A	VSSR	3.3V analog ground
51	D9	I	A	ATSTIN	Test pin. Leave this pin open
52	D10	GND	D	VSSCP	Digital ground
53	D11	GND	D	VSSCP	Digital ground
54	D12	O	A	VCP2	charge pump output，connect to VCP2IN and 22uF+0.1uF to GND
55	D13	I	A	VCP2IN	LDO power supply, connect to VCP2
56	D14	GND	D	VSSCP	Digital ground
57	D15	PWR	D	VDD12CP	Digital power supply, 1.2V
58	D16	-	-	NC	-
59	E1	O	D	DTSTR0	Digital test output
60	E2	O	D	DTSTR1	Digital test output
61	E3	-	-	NC	-
62	E4	GND	A	VSSP	3.3V analog ground
63	E5	GND	A	VSSP	3.3V analog ground
64	E6	GND	A	VSSP	3.3V analog ground
65	E7	GND	A	VSSP	3.3V analog ground
66	E8	GND	A	VSSP	3.3V analog ground
67	E9	GND	A	VSSP	3.3V analog ground
68	E10	GND	A	VSSP	3.3V analog ground
69	E11	GND	A	VSSP	3.3V analog ground
70	E12	I	A	VR_EXTR	Test pin. Leave this pin open.
71	E13	-	-	NC	-
72	E14	PWR	D	VDD12CP	Digital power supply, 1.2V
73	E15	O	D	DTSTR4	Digital test output
74	E16	O	D	DTSTR3	Digital test output
75	F1	O	D	TOUT0	Pulse output. High during pixel exposure period.
76	F2	O	D	TOUT2	Leave this pin open if not use.
77	F3	-	-	NC	-
78	F4	-	-	NC	-
79	F5	PWR	A	VDDCH	Pixel driving signal high level voltage power supply
80	F6	PWR	A	TX2H	Pixel driving signal high level voltage power supply, connect to 2.2uF+0.1uF to GND
81	F7	PWR	A	RSH	Pixel driving signal high level voltage power supply, connect to 2.2uF+0.1uF to GND
82	F8	PWR	A	TX1H	Pixel driving signal high level voltage power supply, connect to 4.7uF+0.1uF to GND
83	F9	PWR	A	GRSTH	Pixel driving signal high level voltage power supply, connect to 2.2uF+0.1uF to GND
84	F10	-	-	NC	-
85	F11	PWR	A	VDDP	3.3V analog power supply
86	F12	I	A	VR_EXTS	Test pin. Leave this pin open.
87	F13	-	-	NC	-
88	F14	-	-	NC	-
89	F15	GND	D	VSS12B	Digital ground
90	F16	PWR	D	VDD12B	Digital power supply, 1.2V
91	G1	PWR	D	VDD12T	Digital power supply, 1.2V
92	G2	GND	D	VSS12T	Digital ground
93	G3	O	D	TOUT1	Leave this pin open if not use.

94	G4	GND	A	VSSP	3.3V analog ground
95	G5	PWR	A	VDDP	3.3V analog power supply
96	G12	-	-	NC	-
97	G13	-	-	NC	-
98	G14	-	-	NC	-
99	G15	-	-	NC	-
100	G16	-	-	NC	-
101	H1	GND	D	VSS12T	Digital ground
102	H2	GND	D	VSS12T	Digital ground
103	H3	I	D	SYSSTBN	System standby signal, low active
104	H4	GND	A	VSSP	3.3V analog ground
105	H5	PWR	A	VDDP	3.3V analog power supply
106	H12	-	-	NC	-
107	H13	GND	A	VSSA2	3.3V analog ground
108	H14	-	-	NC	-
109	H15	GND	D	VSS12B	Digital ground
110	H16	PWR	D	VDD12B	Digital power supply, 1.2V
111	J1	PWR	D	VDD12T	Digital power supply, 1.2V
112	J2	GND	D	VSS12T	Digital ground
113	J3	I	D	MSTSLV	Master/Slave selection input. Low: Master, High: Slave.
114	J4	GND	A	VSSA1	3.3V analog ground
115	J5	PWR	A	VDDA1	3.3V analog power supply
116	J12	PWR	A	VDDA2	3.3V analog power supply
117	J13	GND	A	VSSA2	3.3V analog ground
118	J14	-	-	NC	-
119	J15	-	-	NC	-
120	J16	-	-	NC	-
121	K1	I	D	SA	change slave address for 2-wire serial communication interface
122	K2	-	-	NC	-
123	K3	I	D	SYSRSTN	System reset signal. Low active.
124	K4	GND	A	VSSA1	3.3V analog ground
125	K5	-	-	NC	-
126	K12	PWR	A	VDDP	3.3V analog power supply
127	K13	GND	A	VSSP	3.3V analog ground
128	K14	-	-	NC	-
129	K15	GND	D	VSS12B	Digital ground
130	K16	PWR	D	VDD12B	Digital power supply, 1.2V
131	L1	O	D	SDO	Serial interface data output.
132	L2	I	D	CSN	Serial interface control signal. Pull low to enable the 4-wire serial communication.
133	L3	I	D	SCK	Serial interface clock input
134	L4	GND	A	VSSP	3.3V analog ground
135	L5	PWR	A	VDDP	3.3V analog power supply
136	L12	-	-	NC	-
137	L13	-	-	NC	-
138	L14	-	-	NC	-
139	L15	-	-	NC	-
140	L16	-	-	NC	-
141	M1	PWR	D	VDD12T	Digital power supply, 1.2V
142	M2	GND	D	VSS12T	Digital ground
143	M3	I	D	SDI	Serial interface data input

144	M4	GND	A	VSSA1	3.3V analog ground
145	M5	PWR	A	VDDA1	3.3V analog power supply
146	M6	GND	D	VSS12L	Digital ground
147	M7	PWR	D	VDD18	I/O power supply,1.8V
148	M8	GND	D	VSS12L	Digital ground
149	M9	PWR	D	VDD12L	Digital power supply, 1.2V
150	M10	PWR	D	VDD12D	Digital power supply, 1.2V
151	M11	GND	D	VSS12D	Digital ground
152	M12	PWR	A	VDDA2	3.3V analog power supply
153	M13	GND	A	VSSA2	3.3V analog ground
154	M14	-	-	NC	-
155	M15	GND	D	VSS12B	Digital ground
156	M16	PWR	D	VDD12B	Digital power supply, 1.2V
157	N1	I/O	D	VSYNC	Vertical sync signal input
158	N2	I/O	D	HSYNC	Horizontal sync signal input
159	N3	I	D	TRGEXP	Trigger input
160	N4	-	-	NC	-
161	N5	GND	D	VSS18L	1.8V LVDS Digital ground
162	N6	GND	D	VSS18L	1.8V LVDS Digital ground
163	N7	GND	D	VSS18L	1.8V LVDS Digital ground
164	N8	PWR	D	VDD18L	Digital power supply, 1.8V
165	N9	PWR	D	VDD18L	Digital power supply, 1.8V
166	N10	GND	D	VSS18L	1.8V LVDS Digital ground
167	N11	GND	D	VSS18L	1.8V LVDS Digital ground
168	N12	GND	D	VSS18L	1.8V LVDS Digital ground
169	N13	-	-	NC	-
170	N14	-	-	NC	-
171	N15	-	-	NC	-
172	N16	-	-	NC	-
173	P1	O	D	DTSTL0	Digital test output
174	P2	O	D	DTSTL1	Digital test output
175	P3	-	-	NC	-
176	P4	O	D	TXDP2	LVDS data output
177	P5	O	D	TXDP0	LVDS data output
178	P6	O	D	TXDP3	LVDS data output
179	P7	O	D	TXDP7	LVDS data output
180	P8	GND	D	VSS18L	1.8V LVDS Digital ground
181	P9	GND	D	VSS18L	1.8V LVDS Digital ground
182	P10	O	D	TXDP14	LVDS data output
183	P11	O	D	TXDP10	LVDS data output
184	P12	O	D	TXDP9	LVDS data output
185	P13	O	D	TXDP11	LVDS data output
186	P14	-	-	NC	-
187	P15	O	D	DTSTL4	Digital test output
188	P16	O	D	DTSTL3	Digital test output
189	R1	-	-	NC	-
190	R2	-	-	NC	-
191	R3	O	D	TXDP6	LVDS data output
192	R4	O	D	TXDN2	LVDS data output
193	R5	O	D	TXDN0	LVDS data output
194	R6	O	D	TXDN3	LVDS data output

195	R7	O	D	TXDN7	LVDS data output
196	R8	GND	D	VSS18L	1.8V LVDS Digital ground
197	R9	GND	D	VSS18L	1.8V LVDS Digital ground
198	R10	O	D	TXDN14	LVDS data output
199	R11	O	D	TXDN10	LVDS data output
200	R12	O	D	TXDN9	LVDS data output
201	R13	O	D	TXDN11	LVDS data output
202	R14	O	D	TXDP15	LVDS data output
203	R15	-	-	NC	-
204	R16	O	D	RCK2	Internal clock output. Half of the internal reference clock.
205	T3	O	D	TXDN6	LVDS data output
206	T4	O	D	TXDP4	LVDS data output
207	T5	O	D	TXCP1	LVDS clock output
208	T6	O	D	TXDP1	LVDS data output
209	T7	O	D	TXDP5	LVDS data output
210	T8	O	A	ATST2	Analog test output
211	T9	-	-	NC	-
212	T10	O	D	TXDP12	LVDS data output
213	T11	O	D	TXDP8	LVDS data output
214	T12	O	D	TXCP2	LVDS clock output
215	T13	O	D	TXDP13	LVDS data output
216	T14	O	D	TXDN15	LVDS data output
217	U1	-	-	NC	-
218	U3	-	-	NC	-
219	U4	O	D	TXDN4	LVDS data output
220	U5	O	D	TXCN1	LVDS clock output
221	U6	O	D	TXDN1	LVDS data output
222	U7	O	D	TXDN5	LVDS data output
223	U8	GND	D	VSS12L	Digital ground, 1.2V
224	U9	I	D	INCLK	Input reference clock
225	U10	O	D	TXDN12	LVDS data output
226	U11	O	D	TXDN8	LVDS data output
227	U12	O	D	TXCN2	LVDS clock output
228	U13	O	D	TXDN13	LVDS data output
229	U14	-	-	NC	-
230	U16	-	-	NC	-

Peripheral Connections

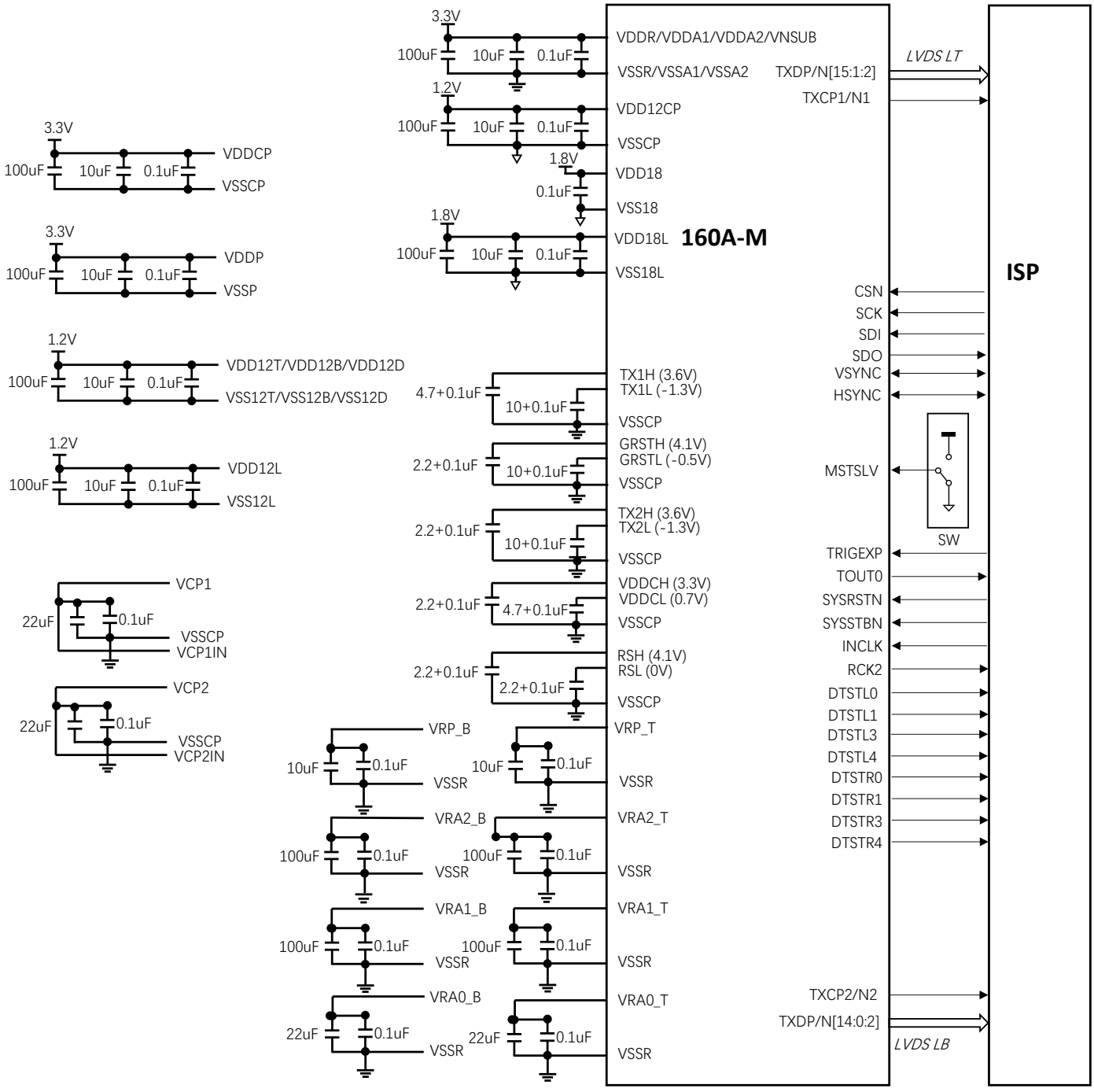


Figure 7. Peripheral connections

Absolute Maximum Ratings

Table 2. Absolute maximum ratings

Operation ambient temperature (T_A)		T.B.D (-10 ~ 60 ℃)
Storage ambient temperature (T_{STOR})		T.B.D (-40 ~ 85 ℃)
Supply voltage (with respect to ground)	VDD33, VDDP33, VDDCP33	-0.3V ~ 4.6V
	VDD18, DVDD18L	-0.3V ~ 3.3V
	VDD12, VDD12L, VDD12CP	-0.3V ~ 1.7V
Digital I/O (DIO/DI/DO. With respect to ground.)		-0.3V ~ VDD18 + 0.3V but <3.3V
Analog I/O (AIO. With respect to ground.)		-0.3V ~ VDD33 + 0.3V but <4.6V

Note: Exceeding the absolute maximum ratings listed above will affect all AC and DC electrical characteristics and may result in permanent damage to the device.

DC Electrical characteristics

Table 3. DC electrical characteristic

Parameter Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Power Supplies						
3.3V analog/digital power supply	VDDR VDDA1 VDDA2 VNSUB		3.3		V	
3.3V analog power supply	VDDP		3.3		V	PLL/PIX/CSL/PGA
3.3V analog power supply	VDDCP		3.3		V	POWER
1.8V I/O power supply	VDD18		1.8		V	I/O
1.8V I/O (LVDS) power supply	VDD18L		1.8		V	LVDS (DVDDL_T/B)
1.2V digital power supply	VDD12T VDD12B VDD12L VDD12CP		1.2		V	Digital core power supply
3.3V operation current	IAV33		*420.2*		mA	Design estimation value
1.8V I/O operation current	IVDD18		*1*		mA	Design estimation value
1.8V LVDS operation current	IDVDDL		*43.2*	*50*	mA	Design estimation value
1.2V operation current	IDV12		*252*		mA	Design estimation value
Pixel power supply Note 1						
Pixel power supply	TX1H TX1L		3.6 -1.3		V V	
Pixel power supply	GRSTH GRSTL		4.1 -0.5		V V	
Pixel power supply	TX2H TX2L		3.6 -1.3		V V	
Pixel power supply	VDDCH VDDCL		3.3 0.7		V V	
Pixel power supply	RSH RSL		4.1 0		V V	
Pixel power supply	AV33_PIX		3.3		V	
Pixel power supply	AG33_PIX		0		V	
Read-out Circuits Reference Voltage Note 2						
PGA voltage reference	VRP		1.25		V	
ADC voltage reference	VRA2		2.2		V	
	VRA1		1.2		V	
	VRA0		1.2		V	
Digital I/O						
Output High Voltage	VOH	VDD18-0.4			V	IOH=2mA
Output Low Voltage	VOL			0.4	V	IOL=2mA
Input High Voltage	VIH	VDD18x0.8			V	
Input Low Voltage	VIL			VDD18x0.2	V	
Low Level Output Current	IOL		T.B.D		mA	VOL=0.4 V

High Level Output Current	IOH		T.B.D		mA	VOH=VDD18-0.4 V
LVDS I/O						
Output Common Voltage	VOCOM		0.9		V	
Output Differential Voltage	|VOD|	200	300	400	mV	Depending on the board design

Note 1: Pixel power supply is generated on-chip, the output symbols are TX1H, TX1L, TX2H, TX2L, GRSTH, GRSTL, VDDCH, VDDCL, RSH, RSL. For details about connection, please refer to **Peripheral Connections**. These reference voltages can be generated by off-chip circuits. When use the off-chip voltage generator, the reference voltages pins should disconnect from the internal reference voltages output pins.

Note 2: These reference voltages are generated on-chip, the output symbols are VRP_T/B, VRA2_T/B, VRA1_T/B and VRA0_T/B. For details about connection, please refer to **Peripheral Connections**. These reference voltages can be generated by off-chip circuits. When use the off-chip voltage generator, the reference voltages pins should disconnect from the internal reference voltages output pins.

AC Electrical characteristics

Reference clock (INCLK) input waveform diagram

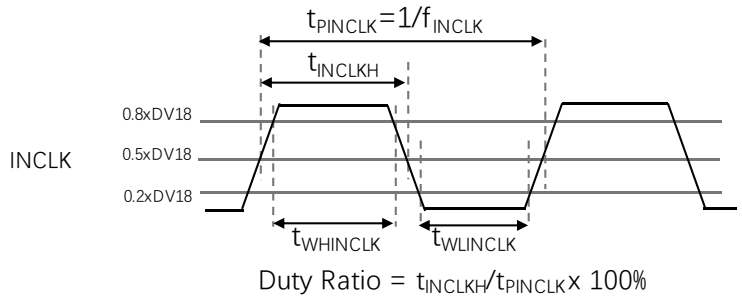


Figure 8. INCLK input waveform diagram

Table 4. INCLK AC electrical characteristics

Parameter Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency of INCLK	f_{INCLK}	12	37.125	62.5	MHz	
INCLK high level pulse width	$t_{WHINCLK}$	T.B.D			ns	
INCLK high level pulse width	$t_{WLINCLK}$	T.B.D			ns	
Duty Ratio	-	45	50	55	%	

Sync signal output waveform diagram (Master Mode)

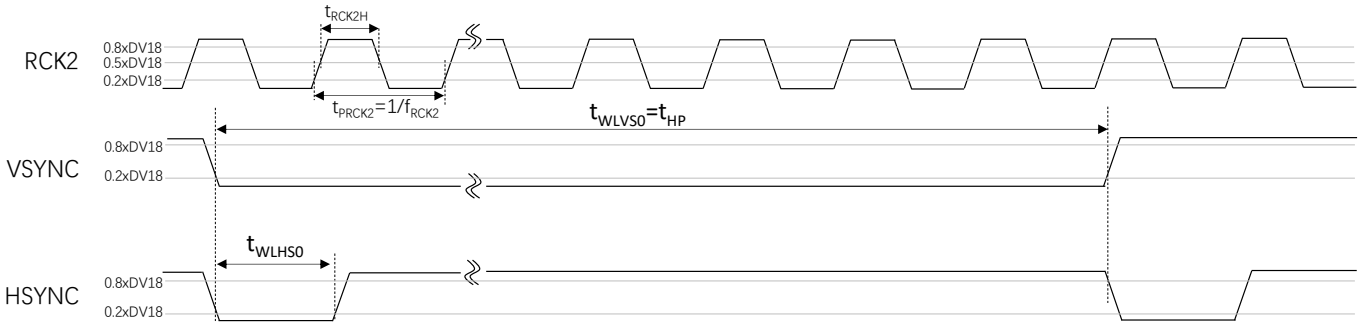


Figure 9. Sync signal output waveform diagram of master mode

Table 5. Sync signal output AC electrical characteristics of master mode

Parameter Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency of clock output RCK2	f_{RCK2}	-	55.7	-	MHz	t_{PRCK2} =1/f_{RCK2}. *Note1*
RCK2 Duty Ratio	-	T.B.D	50	T.B.D	%	t_{RCK2H}/t_{PRCK2} x 100%
Vertical sync signal output low level pulse width.	t_{WLVS0}	-	1x t_{HP}	-	us	*Note2*
Horizontal sync signal output low level pulse width.	t_{WLHS0}	2xt_{PRCK2}			us	

Note 1. Refer to **Input Reference Clock** for detail

Note 2. t_{HP} is the period of one horizontal scanning period. Refer to **Frame Rate and Output Data Rate** for details.

Sync signal input waveform diagram (Slave Mode)

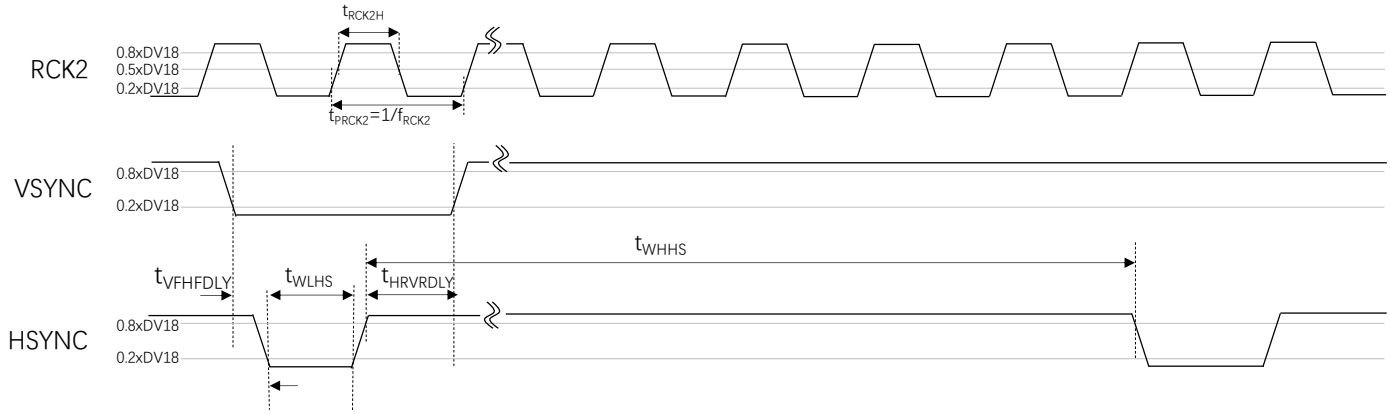


Figure 10. Sync signal input waveform diagram of slave mode

Table 6. Sync signal input AC electrical characteristics of slave mode

Parameter Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency of clock output RCK2	f_{RCK2}	-	55.7	-	MHz	$t_{PRCK2}=1/f_{RCK2}$
RCK2 Duty Ratio	-	T.B.D	50	T.B.D	%	t_{RCK2H}/t_{PRCK2} x 100%
Horizontal sync signal input low level pulse width.	t_{WLHS}	4 x t_{PRCK2}	-	-	us	
Horizontal sync signal input high level pulse width.	t_{WHHS}	4 x t_{PRCK2}	-	-	us	
VSYNC falling edge to HSYNC falling edge delay	$t_{VFHFDLY}$	2 x t_{PRCK2}	-	-	us	
HSYNC rising edge to VSYNC rising edge delay	$t_{HRVRDLY}$	2 x t_{PRCK2}	-	-	us	

Sync signal input waveform diagram (TRIGEXP Mode)

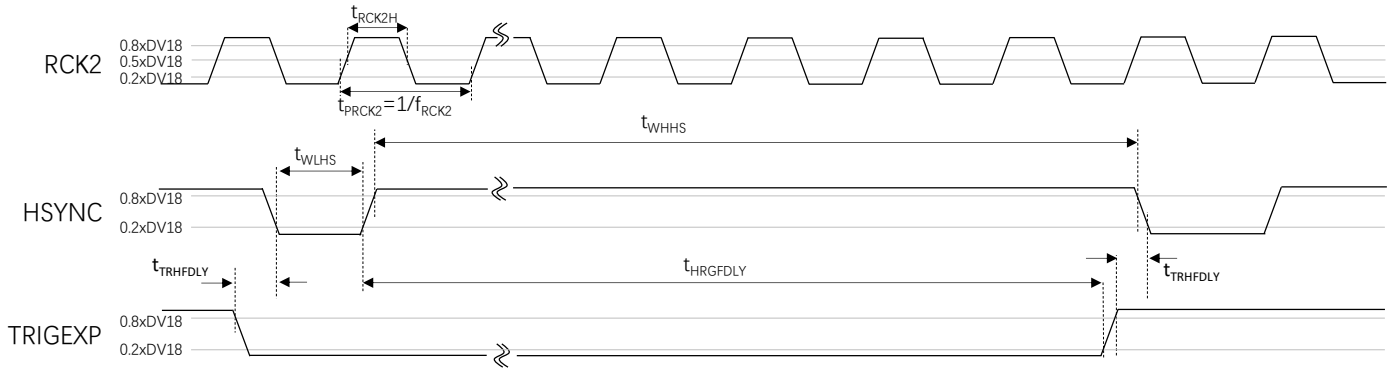
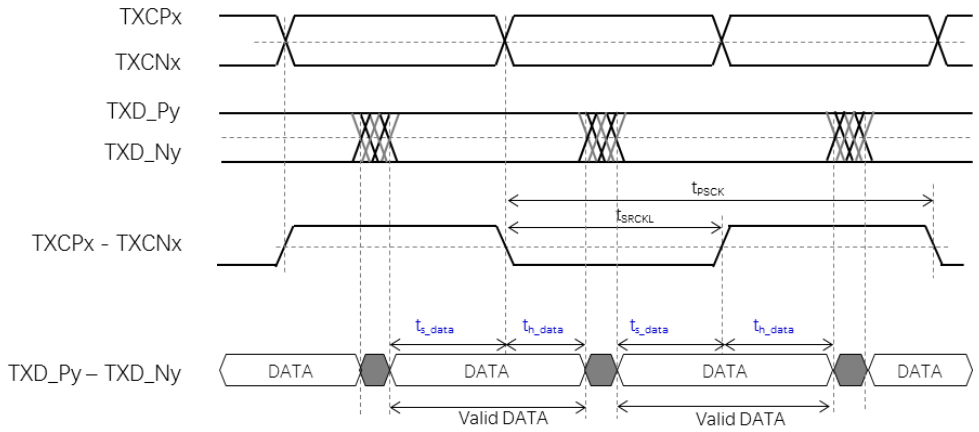


Figure 11. Sync signal input waveform diagram of TRIGEXP mode

Table 7. Sync signal input AC electrical characteristics of TRIGEXP mode

Parameter Item	Symbol	Min.	Typ.	Max.	Unit	Condition
Clock frequency of clock output RCK2	f_{RCK2}	-	55.7	-	MHz	$t_{PRCK2}=1/f_{RCK2}$
RCK2 Duty Ratio	-	T.B.D	50	T.B.D	%	t_{RCK2H}/t_{PRCK2} x 100%
Horizontal sync signal input low level pulse width.	t_{WLHS}	4 x t_{PRCK2}	-	-	us	
Horizontal sync signal input high level pulse width.	t_{WHHS}	4 x t_{PRCK2}	-	-	us	
TRIGEXP rising edge to HSYNC falling edge delay	$T_{TRHFDLY}$	2 x t_{PRCK2}	-	-	us	
TRIGEXP falling edge to HSYNC falling edge delay	$T_{TFHFDLY}$	2 x t_{PRCK2}	-	-	us	

LVDS Outputs



TXCPx/TXCNx , where x: 1,2
TXD_Py/TXD_Ny, where y: 0,1,2···15

Figure 12. LVDS signal waveform diagram

Table 8. LVDS signals AC characteristics

Parameter Item	Symbol	Min.	Typ.	Max.	Unit	Condition
LVDS strobe clock frequency	f_{SRCK}			779.625	MHz	f_{SRCK} =1/t_{PSRCK}
LVDS strobe clock duty ratio	-		50		%	t_{SRCKH}/t_{PSRCK} x 100%
LVDS data setup time	t_{s_data}		T.B.D. (0.35)		UI	UI = 1/(2 x f_{SRCK})
LVDS data hold time	t_{h_data}		T.B.D. (0.35)		UI	UI = 1/(2 x f_{SRCK})

4-wire SPI-like serial communication interface timing diagram

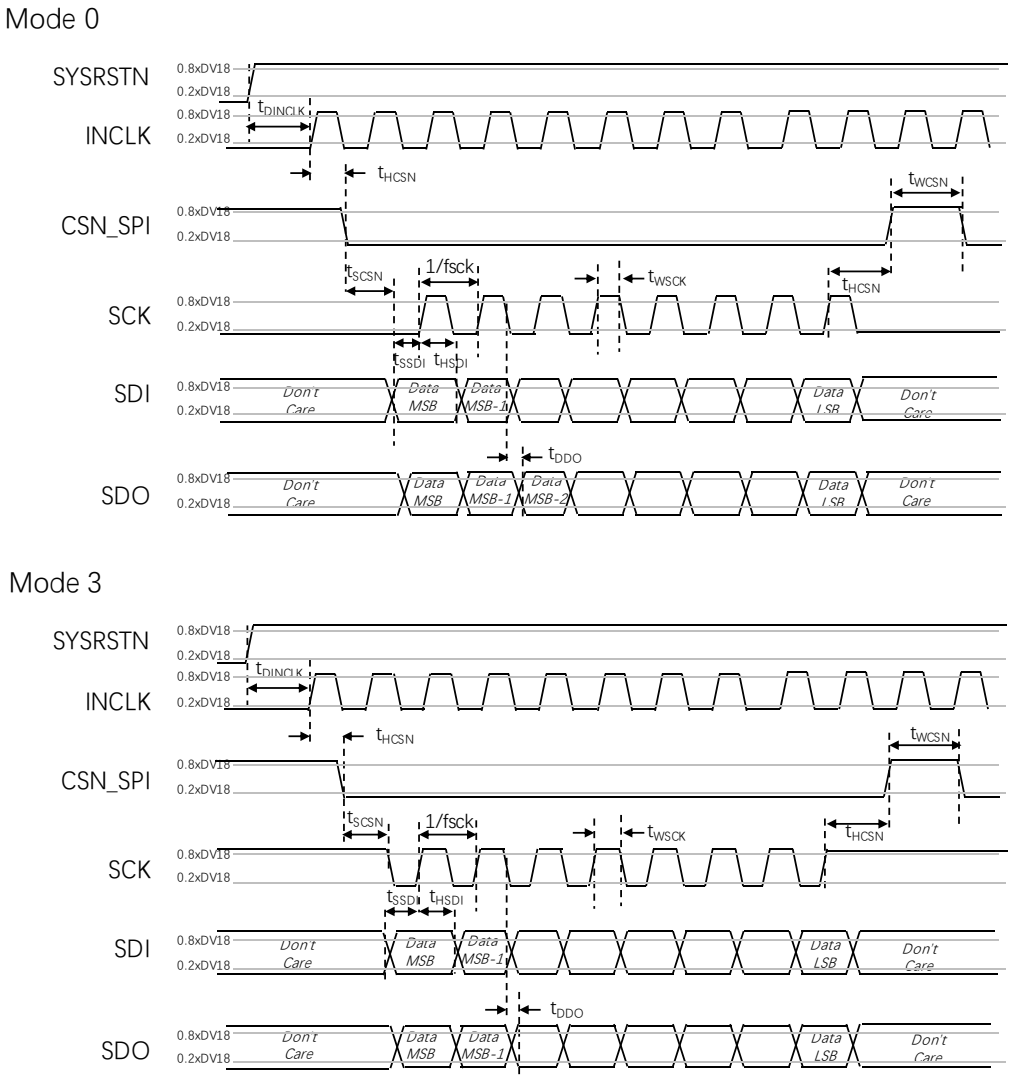


Figure 13. 4-wire serial interface timing diagram

Table 9. 4-wire serial interface AC electrical characteristics

Parameter Item	Symbol	Specs				Note
		Min.	Typ.	Max.	unit	
SCK input frequency	f_{SCK}			$f_{INCLK}/5$	MHz	
CSN input high level pulse width	t_{WCSN}	2 x t_{PINCLK}			us	t_{PINCLK} =1/f_{INCLK}
Clock input delay	t_{DINCLK}	1.5 x t_{PINCLK}			us	
SCK input high level pulse width	t_{WSCK}	2 x t_{PINCLK}			us	
CSN input setup time	t_{SCSN}	2 x t_{PINCLK}			us	
CSN input hold time	t_{HCSN}	2.5 x t_{PINCLK}			us	
SDI input setup time	t_{SSDI}	t_{PINCLK}+0.005			us	
SDI input hold time	t_{HSDI}	t_{PINCLK}+0.005			us	
SDO data output delay	t_{DDO}	t_{PINCLK}+0.005			us	

2-wire serial communication interface timing diagram.

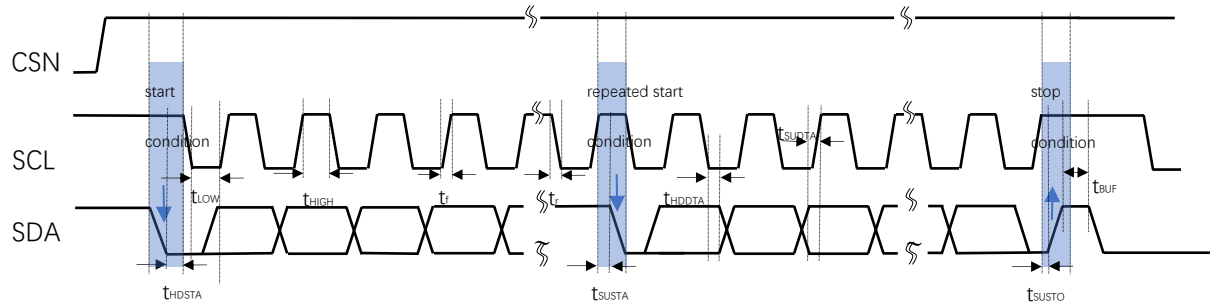


Figure 14. I2C serial interface timing diagram

Table 10. I2C serial interface AC electrical characteristics

Parameter Item	Symbol	Specs				Note
		Min.	Typ.	Max.	unit	
SCL *Note1* input frequency	f_{SCL}	-	-	1	MHz	
Setup time (Start condition)	t_{HDSTA}	0.26			us	
Hold time (Repeated start condition)	t_{SUSTA}	0.26			us	
SCL input low level pulse width	t_{LOW}	0.50			us	
SCL input high level pulse width	t_{HIGH}	0.26			us	
Data setup time	t_{HDDAT}	0		0.45	us	
Data hold time	t_{SUDAT}	0.05			us	
Setup time (Stop condition)	t_{SUSTO}	0.26			us	
Bus free time between a Stop and a Start condition	t_{BUF}	0.50			us	
SDA *Note 2* SCL rising time	t_R			0.12	us	
SDA, SCL falling time	t_F			0.12	us	

Note 1. Share the same package pin with SCK.
Note 2. Share the same package pin with SDI.

Internal Register Access

This part describes the register access through 4-wire SPI-like and 2-wire serial communication interface.

Internal Register Access

Please refer to AC Electrical characteristics for detailed waveform diagram.

4-wire SPI-like serial communication interface

1. Command packet, address packet and data packet
   The first 8-bit is command packet. The first bit is command-bit, “0” for write mode and “1” for read mode, and followed by four “0”s. the last three bits “S2,S1,S0” are used to select register block .
   The second 8-bit packet is address packet that specifies the address to write or read.
   Starting from the third packet, all packets are data packet, which in write mode are the data to write (input through SDI) and in read mode are the read out data from the corresponding address (output through SDO)

2. Random access to any address is possible.

3. It is also possible to access multi continuous addresses starting from a random address.
   In this mode, after the access to the address specified by address packet is completed, the target address will automatically point to the next address.

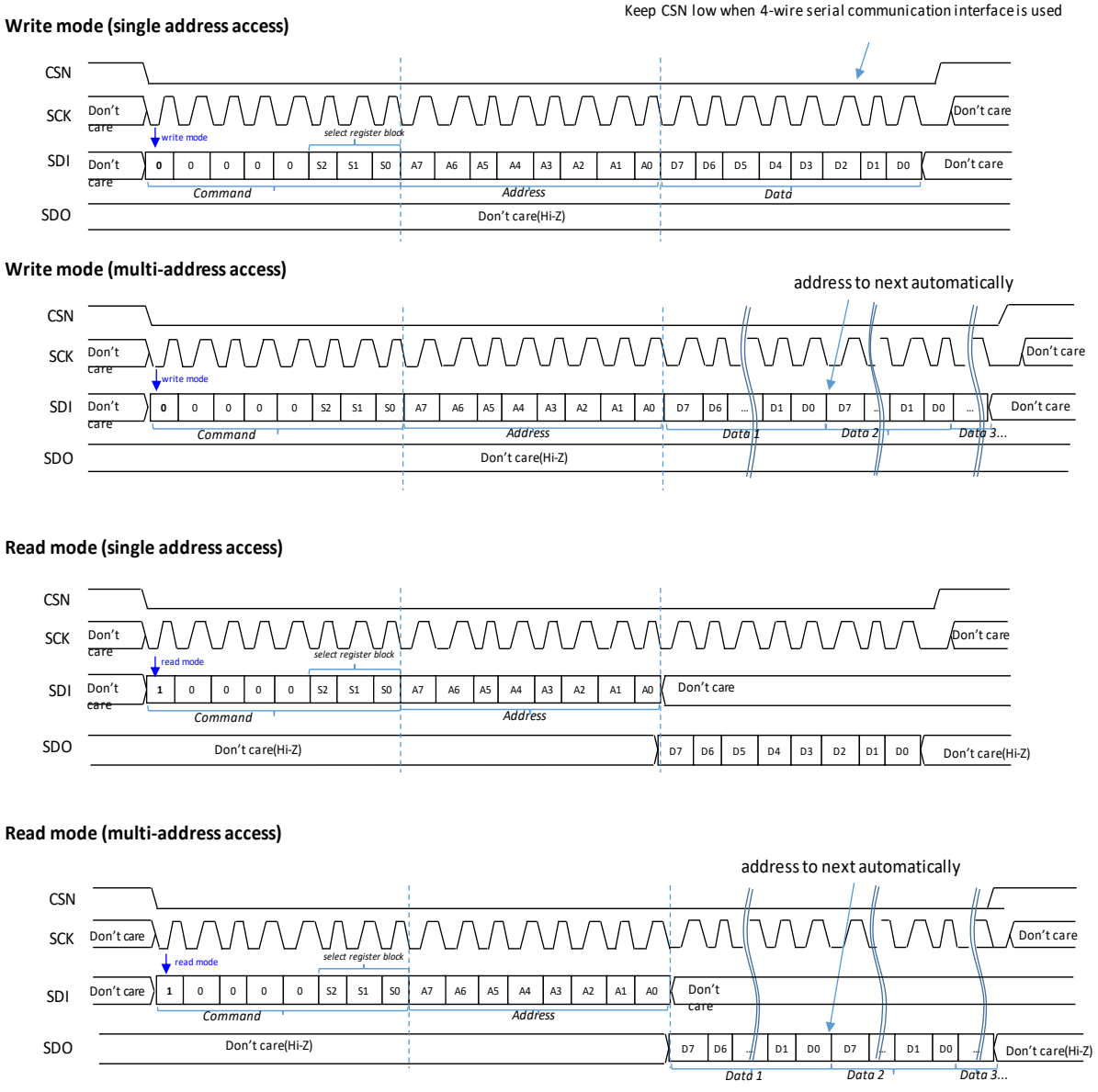


Figure 15. 4-wire serial communication interface timing diagram

2-wire serial communication interface

1. Start and stop condition (refer to *Figure 16* for detail)

SDA can change only while SCL is low, so the start condition is that when SDA goes from high to low while SCL is high, and stop condition is that when SDA goes from low to high while SCL is high. When the stop condition is not generated in the previous communication phase and start condition is generated for the next communication, that start condition is recognised as a repeated start condition.

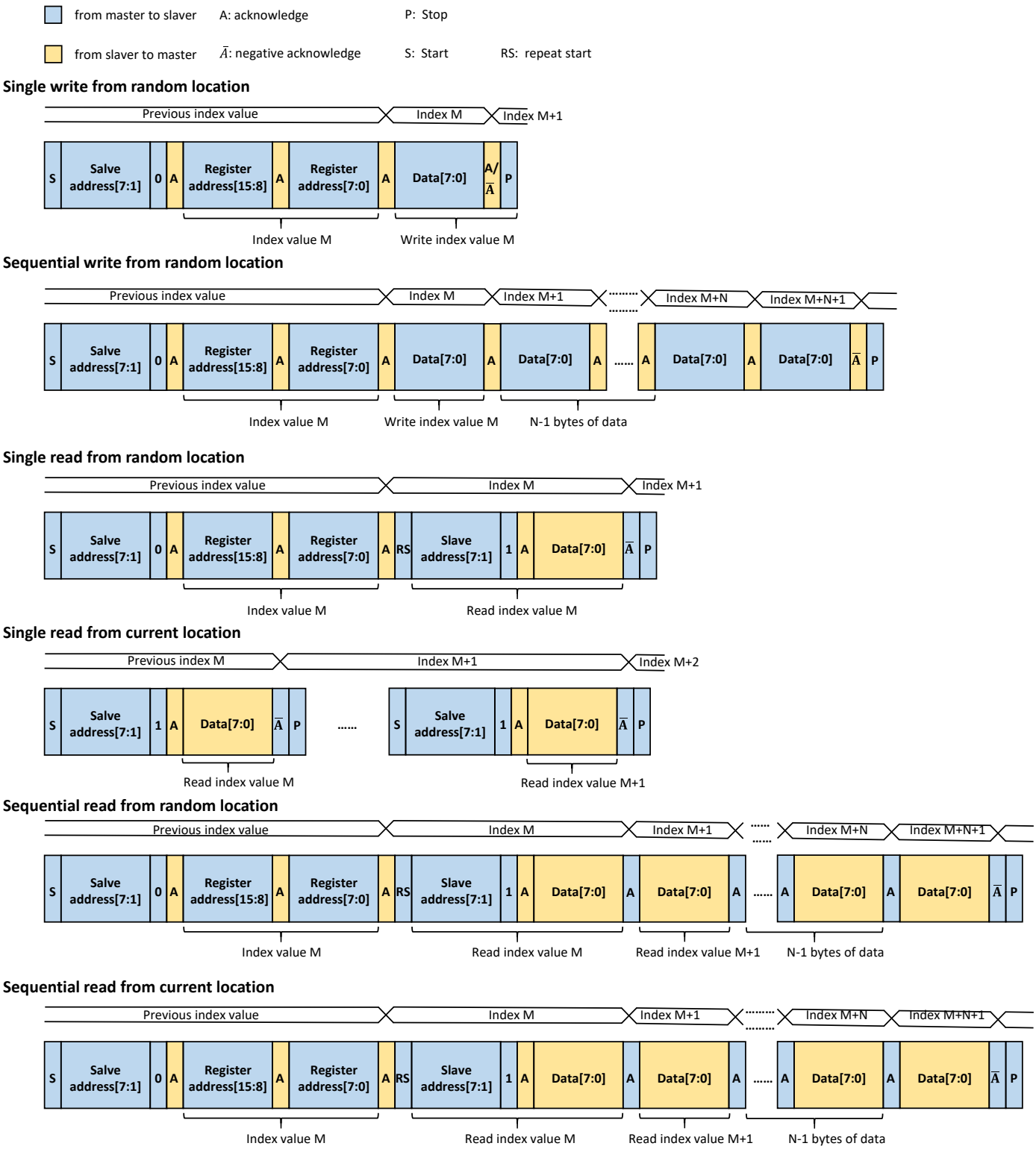


Figure 16. 2-wire serial communication interface timing diagram

2. Acknowledgment

When master transferred a data byte to slaver, a bit of acknowledgment(A) or negative acknowledgment($\bar{A}$) is transferred from slaver to master, means the data byte to slaver is valid or invalid. And after slaver transferred a data

byte to master, a bit of acknowledgment(A) or negative acknowledgment($\bar{A}$) is transferred from master to slaver, means the data byte to master is valid or invalid.

3. Command packet, address packet and data packet
The first 8-bit is command packet, in which the first 7 bits are slave address, and the last bit is command bit,"0" for write mode and "1" for read mode. Slave address is set to "0010000" or "0011010" when the pin SA set to "0"or "1" . The second and third 8-bit packets are register address packets that specifies the address to write or read. Starting from the fourth packet, all packets are data packet, which in write mode are the data to write and in read mode are the read out data from the corresponding address. Data are transfered serially in 8 bits unit with MSB first.

4. Random access to any address is possible.

5. It is also possible to access multi continuous addresses starting from a random address.
In this mode, after the access to the address specified by address packet is completed, the target address will automatically point to the next address.

Register Reflection Timing

There are two types of register reflection timing, immediately and sync to vertical period. Sync to vertical period is controlled by register REGHOLD, sync to vertical period is valid when REGHOLD=0. In **Register Map**, the column "reflection timing" marks each register's reflection timing, "I" for immediately and "V" for sync to vertical period.

Immediately reflection timing

The registers will take into effect immediately after the input of 8-bit data packet.

Sync to vertical period

The registers will take into effect after the next VSYNC pulse when REGHOLD=0.

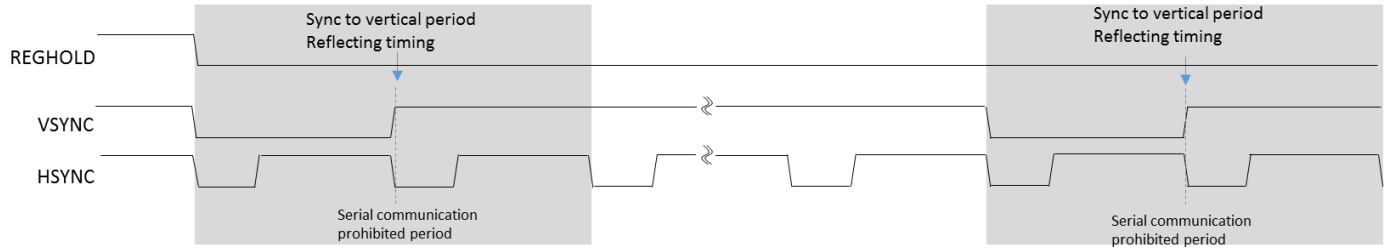


Figure 17. Register reflection timing diagram

Register Map

Please refer to other document for details.

Input Signals

Master Mode and Salve Mode

The sensors can operate at master mode and slave mode. The operation mode is selected by pin input and register setting. By default, since the register Addr.0x4C[6] is set to "0" and Addr.0x4E[7] is set to "0" ,operation mode can be switched by pin MSTSLV.

Table 11. Register setting of master mode and slave mode

Operation Mode	pin input	Register setting	
	MSTSLV	Addr.0x4C[6]	Addr.0x4E[7]
Master mode	0	x	0(default)
	x	0(default)	1
Slave mode	1	x	0
	x	1	1

Note: TRIGEXP mode is same as slave mode

Input Signals

The sensors need input signals to operate properly.

Table 12. Input signals

	Master mode	Slave mode	TRIGEXP mode
Input Signals			
Reference clock input (pin INCLK)	Yes	Yes	Yes
Synchronization signal input (VSYNC/HSYNC)	No (pin VSYNC, HSYNC are outputs)	Yes (pin VSYNC, HSYNC are inputs)	Yes (pin HSYNC is input)
Trigger signal input (TRIGEXP)	No (do not care the input of pin TRIGEXP)	No (do not care the input of pin TRIGEXP)	Yes (pin TRIGEXP is input)
Power supply and reference voltage input	Yes Note 1.	Yes The same as Master mode	Yes The same as Master mode

Note 1: Please refer to *DC Electrical characteristics* for details

Input Reference Clock and Clock System

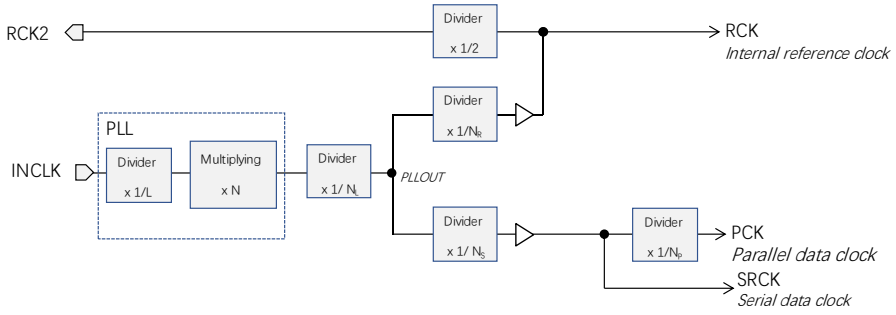


Figure 18. Clock system diagram

Input reference clock is input through pin INCLK and multiplied by PLL. From the PLL output clock, dividers generate internal reference clock (RCK), the parallel data clock (PCK) and the serial data clock (SRCK, it is also the LVDS strobe clock.).

The frequency of internal clock respect to the input reference clock are as shown below.

$f_{PLLOUT} = f_{INCLK} * N / L / N_L$

$f_{RCK} = f_{PLLOUT} / N_R$

$f_{SRCK} = f_{PLLOUT} / N_S$

$f_{PCK} = f_{SRCK} / N_P$

f_{PCK} and f_{SRCK} must be set that, $f_{SRCK} = DBW * f_{PCK}$ or $DBW = N_P$, where DBW is the output data bit-width and can be set to 14,12 ,10 or 8. DBW is set by register 194[1:0], 00b: 8bit, 01b: 10bit, 10b:12bit,11b:14bit, default value is 11b.

N, L, N_L, N_R, N_S and N_P are set by the following register respectively.
(By default,
L = 2, N = 42, N_L = 1, N_R = 7, N_S = 1, N_P = 14, DBW = 14
f_{INCLK} = 37.125 MHz
f_{PLLOUT} = f_{INCLK} * N/ L / N_L = 37.125MHz * 42 / 2 / 1 = 779.625 MHz
f_{RCK} = f_{PLLOUT} / N_R = 779.625MHz / 7 = 111.375 MHz
f_{SRCK} = f_{PLLOUT} / N_S = 779.625 MHz
f_{PCK} = f_{SRCK} / N_P = 779.625MHz / 14 = 55.6875 MHz)

N (Register Index:98, bit6~0, PLL_DIV_N[6:0], default value: 0x2A):

Table 13. Register setting of DIV_N[6:0]

Feedback Divider Setting DIV_N[6:0]	Feedback Divider Ratio(N)
7'b0000000～7'b0001011	Not defined
7'b0001100	12
7'b0001101	13
7'b0001110	14
…	…
7'b1111110	126
7'b1111111	127

L (Register Index:97, bit3~0, PLL_DIV_L[3:0], default value: 0x1):

Table 14. Register setting of DIV_L[3:0]

Input Divider Setting DIV_L[3:0]	Input Divider Ratio(L)
4'b0000	1
4'b0001	2
4b'0010	3
…	
4'b1110	15
4'b1111	16

N_L (Register Index:101, bit7~6, PLL_DIV1[1:0], default value: 0x0):
Note: N_L = PLL_DIV1 + 1, where PLL_DIV1 is the register value in decimal.

Table 15. Register setting of DIV_NL[1:0]

Post Divider Setting DIV_NL[1:0]	Post divider Ratio(N_L)
2'b00	1
2'b01	2
2'b10	3
2'b11	4

N_R (Register Index:77, bit4~0, CKGEN_RCKDIV[4:0], default value: 0x7):
Note: N_R = CKGEN_RCKDIV , where CKGEN_RCKDIV is the register value in decimal.

Table 16. Register setting of DIV_NR[4:0]

RCK Divider Setting DIV_NR[4:0]	RCK divider Ratio(N_R)
5b'00001	1
5b'00010	2
5b'00011	3
……	……
5b'11110	30
5b'11111	31

N_S (Register Index:76, bit4~0, CKGEN_SCKDIV[4:0], default value: 0x1)

Note: N_S = CKGEN_SCKDIV , where CKGEN_SCKDIV is the register value in decimal.

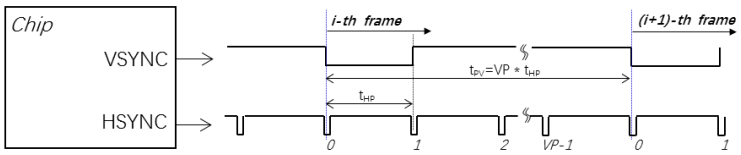
Table 17. Register setting of DIV_NS[4:0]

SCK Divider Setting DIV_NS[4:0]	SCK divider Ratio(N_S)
5b'00000	0
5b'00001	1
5b'00010	2
5b'00011	3
……	……
5b'11110	30
5b'11111	31

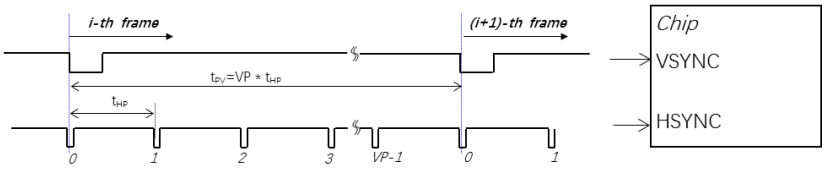
Synchronize Signal

In master mode, the sensors will internally generate a vertical sync signal (VSYNC) and a horizontal sync signal (HSYNC). These two sync signals are output through pin VSYNC and HSYNC, respectively. The waveforms are as shown in *Figure 19*. where, t_{HP} is the time of one horizontal period, VP is the number of horizontal periods in one vertical period.

Master Mode



Slave Mode



TRIGEXP Mode

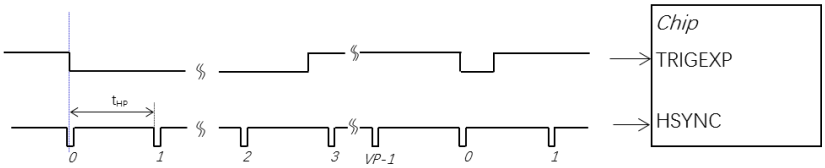


Figure 19. Timing diagram of synchronize signal

In master mode, the vertical period and horizontal period are set by the following registers.

Vertical period:
VP[23:0]: Register 16[7:0], 15[7:0], 14[7:0], default value: 0x001021 (4129d)
unit: one horizontal period
The vertical period VP is VP[23:0] + 1, by 160A-M default, VP is 4130;

Horizontal period:
HP[15:8]: Register 17[7:0], 18[7:0]. Default value: 0x023F (575d)
unit: one RCK period, when RCK is the internal reference clock.
The horizontal period HP is HP[15:0] + 1, by default, HP is 576.

In slave mode, the vertical sync signal and horizontal sync signal must be input from pin VSYNC and HSYNC respectively. Refer to **AC Electrical characteristics** for electrical requirements. As shown in the following figure, the vertical period and horizontal period are determined by the time between two adjacent pulses of VSYNC and HSYNC, respectively. The vertical period and horizontal period must be set carefully for proper operation, please refer to Frame Rate and Output Data Rate for details.

Frame Rate and Output Data Rate

The following table lists the default settings of internal reference clock frequency, vertical and horizontal period and data rate. When it is necessary to adjust frame rate according to the requirement of a specific application, instead of horizontal period, it is recommended to adjust the vertical period or internal reference clock frequency.

Table 18. Frame rate and output data rate

INCLK [MHz]	-	Frame Rate [fps]	f_{RCK} [MHz]	V period VP [t_{HP}]	H period HP [t_{PRCK}]	f_{PCK} [MHz]	f_{SRCK} [MHz]	The number of LVDS lane	LVDS data rate [Mbps]
37.125	160A-M	46.8183	111.375	4130	576	55.6875	779.625	16	779.625

Note: t_{PRCK} is one period of RCK. $t_{PRCK}=1/f_{RCK,}$ where f_{RCK} is the frequency of RCK.

Image Data Output Format

Pixel Read Out Order

As shown in the following figure, in default mode, the vertical scanning direction is from down to up, the horizontal scanning direction is from left to right.

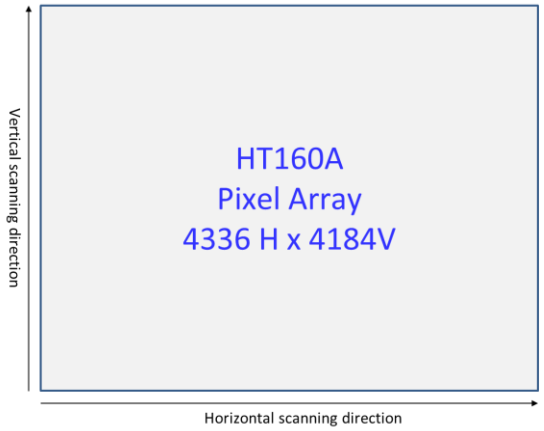


Figure 20. Pixel read out order in default mode

Image Output Data Format

Image output data from each LVDS pair includes sync codes, pixel data, VBLANK, HBLANK and invalid data. The following figure is an image drawing of the image output data format. The data need to capture start with a sync code. There are four types of sync code,

SOF, start of frame
SOL, start of line
EOL, end of line
EOF, end of frame

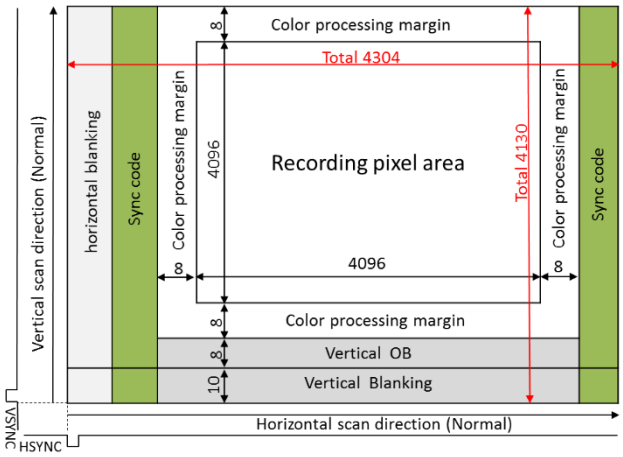


Figure 21. Image of output data

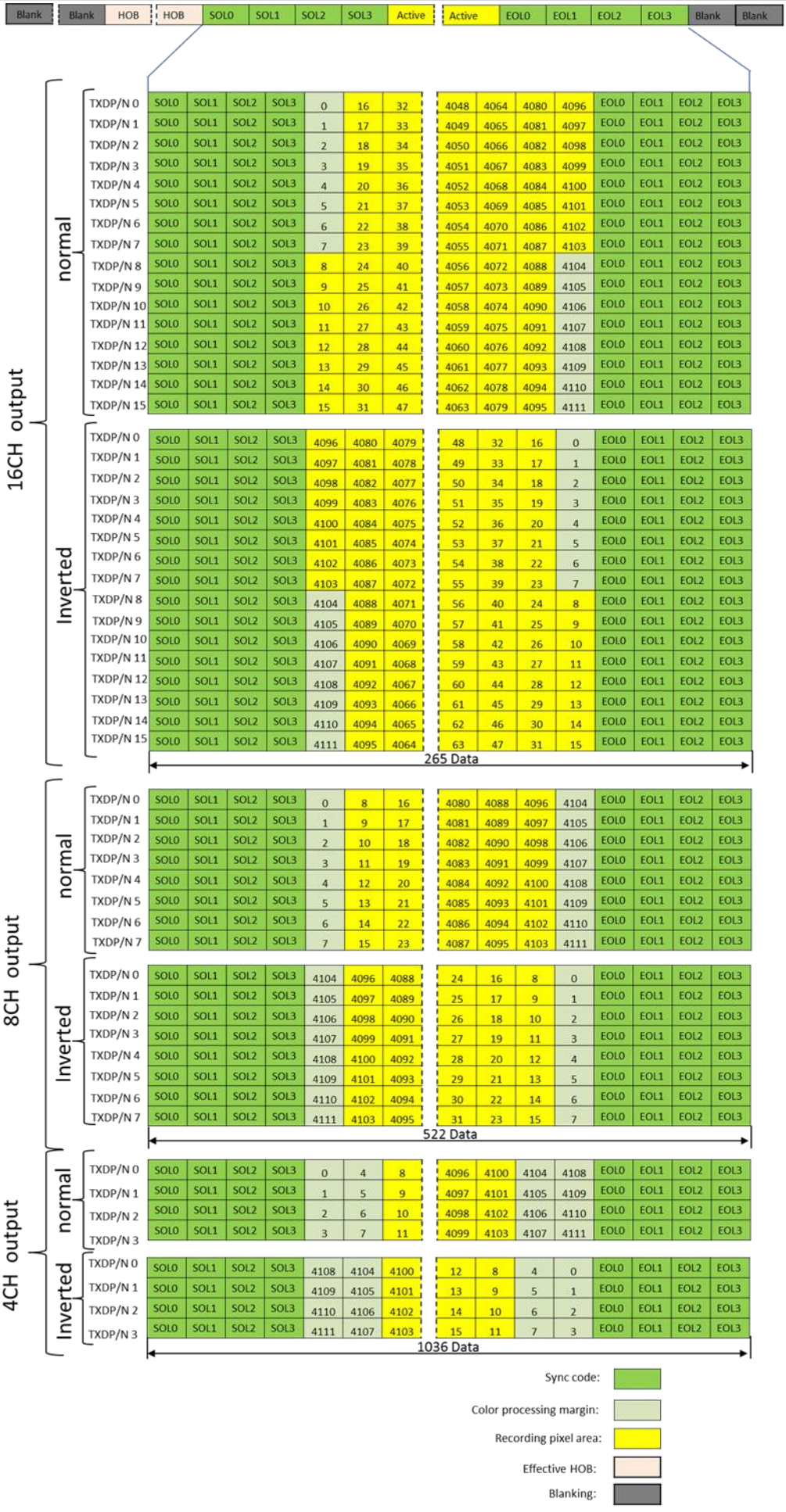


Figure 22. Image drawing of the image output data in normal mode

Sync Code

Each sync code has 4 words (1 word has same data width of a pixel data) as list in the following table (in kinds of modes). Only the 3rd word is designated to be different.

The sensors support multi-frame WDR (wide dynamic range) mode. By default, WDR mode is disabled and WDR mode can be enabled by setting RLI_WDR_EN to high. In WDR mode, sync code of N consecutive frames automatically switch between N sync codes. N=2 when RLI_WDR_MODE=00, N=3 when RLI_WDR_MODE=01 and N=4 when RLI_WDR_MODE=10/11.

Table 19. Sync code of Sync.Code0

Symbol	Output Bit-Width	Sync.Code0					
		SOL	EOL	SOF	EOF	SSOE	ESOE
S0	8	FFh	FFh	FFh	FFh	FFh	FFh
	10	3FFh	3FFh	3FFh	3FFh	3FFh	3FFh
	12	FFFh	FFFh	FFFh	FFFh	FFFh	FFFh
	14	3FFFh	3FFFh	3FFFh	3FFFh	3FFFh	3FFFh
S1	8	00h	00h	00h	00h	00h	00h
	10	000h	000h	000h	000h	000h	000h
	12	000h	000h	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h	0000h	0000h
S2	8	00h	00h	00h	00h	00h	00h
	10	000h	000h	000h	000h	000h	000h
	12	000h	000h	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h	0000h	0000h
S3	8	80h	9Dh	ABh	B6h	90h	98h
	10	200h	274h	2ACh	2D8h	240h	260h
	12	800h	9D0h	AB0h	B60h	900h	980h
	14	2000h	2740h	2AC0h	2D80h	2400h	2600h

*Note: S0: the 1st word, S1: the 2nd word, S2: the 3rd word, S3: the 4th word.

Table 20. Sync code of Sync.Code1

Symbol	Output Bit-Width	Sync.Code1					
		SOL	EOL	SOF	EOF	SSOE	ESOE
S0	8	FFh	FFh	FFh	FFh	FFh	FFh
	10	3FFh	3FFh	3FFh	3FFh	3FFh	3FFh
	12	FFFh	FFFh	FFFh	FFFh	FFFh	FFFh
	14	3FFFh	3FFFh	3FFFh	3FFFh	3FFFh	3FFFh
S1	8	00h	00h	00h	00h	00h	00h
	10	000h	000h	000h	000h	000h	000h
	12	000h	000h	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h	0000h	0000h
S2	8	00h	00h	00h	00h	00h	00h
	10	000h	000h	000h	000h	000h	000h
	12	000h	000h	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h	0000h	0000h
S3	8	81h	A1h	AFh	B9h	91h	99h
	10	204h	284h	2BCh	2E4h	244h	264h
	12	810h	A10h	AF0h	B90h	910h	990h
	14	2040h	2840h	2BC0h	2E40h	2440h	2640h

Table 21. Sync code of Sync.Code2

Symbol	Output Bit-Width	Sync.Code2					
		SOL	EOL	SOF	EOF	SSOE	ESOE
S0	8	FFh	FFh	FFh	FFh	FFh	FFh
	10	3FFh	3FFh	3FFh	3FFh	3FFh	3FFh
	12	FFFh	FFFh	FFFh	FFFh	FFFh	FFFh
	14	3FFFh	3FFFh	3FFFh	3FFFh	3FFFh	3FFFh
S1	8	00h	00h	00h	00h	00h	00h
	10	000h	000h	000h	000h	000h	000h
	12	000h	000h	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h	0000h	0000h

S2	8	00h	00h	00h	00h	00h	00h
	10	000h	000h	000h	000h	000h	000h
	12	000h	000h	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h	0000h	0000h
S3	8	82h	A2h	AEh	BAh	92h	9Ah
	10	208h	288h	2B8h	2E8h	248h	268h
	12	820h	A20h	AE0h	BA0h	920h	9A0h
	14	2080h	2880h	2B80h	2E80h	2480h	2680h

Table 22. Sync code of Sync.Code3

Symbol	Output Bit-Width	Sync.Code3					
		SOL	EOL	SOF	EOF	SSOE	ESOE
S0	8	FFh	FFh	FFh	FFh	FFh	FFh
	10	3FFh	3FFh	3FFh	3FFh	3FFh	3FFh
	12	FFFh	FFFh	FFFh	FFFh	FFFh	FFFh
	14	3FFFh	3FFFh	3FFFh	3FFFh	3FFFh	3FFFh
S1	8	00h	00h	00h	00h	00h	00h
	10	000h	000h	000h	000h	000h	000h
	12	000h	000h	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h	0000h	0000h
S2	8	00h	00h	00h	00h	00h	00h
	10	000h	000h	000h	000h	000h	000h
	12	000h	000h	000h	000h	000h	000h
	14	0000h	0000h	0000h	0000h	0000h	0000h
S3	8	83h	A3h	AFh	BBh	93h	9Bh
	10	20Ch	28Ch	2BCh	2ECh	24Ch	26Ch
	12	830h	A30h	AF0h	BB0h	930h	9B0h
	14	20C0h	28C0h	2BC0h	2EC0h	24C0h	26C0h

*Note:

WDR mode 00, sync code switch between **Sync.Code0** and **Sync.Code1;**
WDR mode 01, sync code switch between **Sync.Code0** and **Sync.Code1, Sync.Code2;**
WDR mode 10/11, sync code switch between **Sync.Code0** and **Sync.Code1, Sync.Code2, Sync.Code3.**

Example Data Output of One LVDS Pair

The following figure shows an example of 160A-M 16-channel data output from channel x (x=0~15, Normal mode).

160A-M Channelx DATA. Note: P[column, row], N=PCK-25, M=HP-18, x=0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15

HP# ↓ PCK #→	0	1~13	14	15	16~19	20	21	22	23	24	25	26	27~149	150	151	152	153	154~278	279	280	281	282	283	284	285	286	287	Type of Pix.	# of row
4128	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	Active Pixel	
4129	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	EOF0	EOF1	EOF2	EOF3	Invalid data	Invalid data		
0	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
1~8	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	VBLANK	10
9	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
10	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOF0	SOF1	SOF2	SOF3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
11~16	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	VOB	8
17	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
18	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
19	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
20-1999	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	...	...	...	...	...	...	...	...	...	...	...	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2000	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2001	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	Active Pixel	4112
2002	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2003	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2004-4127	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	...	...	...	...	...	...	...	...	...	...	...	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
4128	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
4129	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	...	P[16N+x,M]	P[16N+x,M]	P[16N+x,M]	EOF0	EOF1	EOF2	EOF3	Invalid data	Invalid data		
0	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
1~8	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	VBLANK	10
9	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
10	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	VOB	8
Type of Data.	HBLANK			HOB			SYNC_CODE				Active Pixel											SYNC_CODE				HBLANK			
# of col	15			6			4				257											4				2			

Figure 23. 160A-M 16-channel data output from channel x

The following figure shows an example of 160A-M 8-channel data output from channel x (x=0~7, Normal mode).

160A-M Channelx DATA. Note: P[column, row], N=PCK-50, M=HP-18, x=0, 1, 2, 3, 4, 5, 6, 7

HP# ↓ PCK #→	0	1–28	29	30	31–44	45	46	47	48	49	50	51	52–299	300	301	302	303	304–560	561	562	563	564	565	566	567	568–574	575	Type of Pix.	# of row
4128	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	Active Pixel	
4129	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	EOF0	EOF1	EOF2	EOF3	Invalid data	Invalid data		
0	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
1–8	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	VBLANK	10
9	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
10	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOF0	SOF1	SOF2	SOF3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
11–16	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	VOB	8
17	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
18	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	Active Pixel	4112
19	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
20-1999	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	...	...	...	...	...	...	...	...	...	...	...	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2000	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2001	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2002	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2003	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2004-4127	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	...	...	...	...	...	...	...	...	...	...	...	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
4128	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
4129	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	...	P[8N+x,M]	P[8N+x,M]	P[8N+x,M]	EOF0	EOF1	EOF2	EOF3	Invalid data	Invalid data		
0	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
1–8	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	VBLANK	10
9	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
10	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	VOB	8
Type of Data.	HBLANK			HOB			SYNC_CODE				Active Pixel											SYNC_CODE				HBLANK			
# of col	30			16			4				514											4				8			

Figure 25. 160A-M 8-channel data output from channel x

The following figure shows an example of 160A-M 4-channel data output from channel x (x=0~3, Normal mode).

160A-M Channelx DATA. Note: P[column, row], N=PCK-100, M=HP-18, x=0, 1, 2, 3

HP# ↓ PCK #→	0	1~58	59	60	61~94	95	96	97	98	99	100	101	102~599	600	601	602	603	604~1123	1124	1125	1126	1127	1128	1129	1130	1131~1150	1151	Type of Pix.	# of row
4128	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	Active Pixel	
4129	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	EOF0	EOF1	EOF2	EOF3	Invalid data	Invalid data		
0	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
1~8	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	VBLANK	10
9	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
10	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOF0	SOF1	SOF2	SOF3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
11~16	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	VOB	8
17	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
18	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	Active Pixel	4112
19	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
20-1999	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	...	...	...	...	...	...	...	...	...	...	...	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2000	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2001	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2002	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2003	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
2004-4127	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	...	...	...	...	...	...	...	...	...	...	...	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
4128	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
4129	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	...	P[4N+x,M]	P[4N+x,M]	P[4N+x,M]	EOF0	EOF1	EOF2	EOF3	Invalid data	Invalid data		
0	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
1~8	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	VBLANK	10
9	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data		
10	Invalid data	...	Invalid data	Invalid data	...	Invalid data	SOL0	SOL1	SOL2	SOL3	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	Invalid data	...	Invalid data	Invalid data	Invalid data	EOL0	EOL1	EOL2	EOL3	Invalid data	Invalid data	VOB	8
Type of Data.	HBLANK			HOB			SYNC_CODE				Active Pixel											SYNC_CODE				HBLANK			
# of col	60			36			4				1028											4				20			

Figure 27. 160A-M-M 4-channel data output from channel x

LVDS Data Bit Output Order

The output DBW width can be selected from 14-bit, 12-bit, 10-bit or 8-bit output using register RLI_LVS_BS. Sync code is output according to bit width setting of these register.

Table 23. Register list of bit width selection

Register name	Address and bit	Default value	Setting value
RLI_LVS_BS[1:0]	194[1:0]	11b	00b: 8-bit; 01b: 10-bit; 10b: 12-bit; 11b: 14-bit;

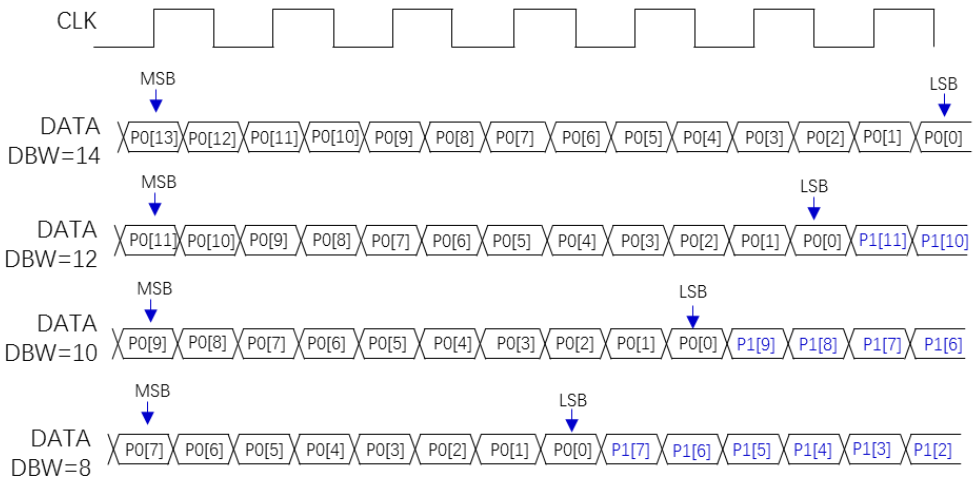


Figure 29. Output Data Bit Output Order

Exposure time Adjustment

The sensors have a charge-domain global shutter. Each pixel has a memory node for charge storage during read-out period. During the global charge transfer period, all pixels move the charges in the photo diode to its own memory node. Then the charge will be stored in the memory node until be read out row by row.

Internal Expsoure Time Control Mode

At internal exposure time control mode, the exposure time is determined by registers. This mode is available for both master mode and slave mode.

The charge transfer period, read out period and exposure time etc. are shown in the following figure.

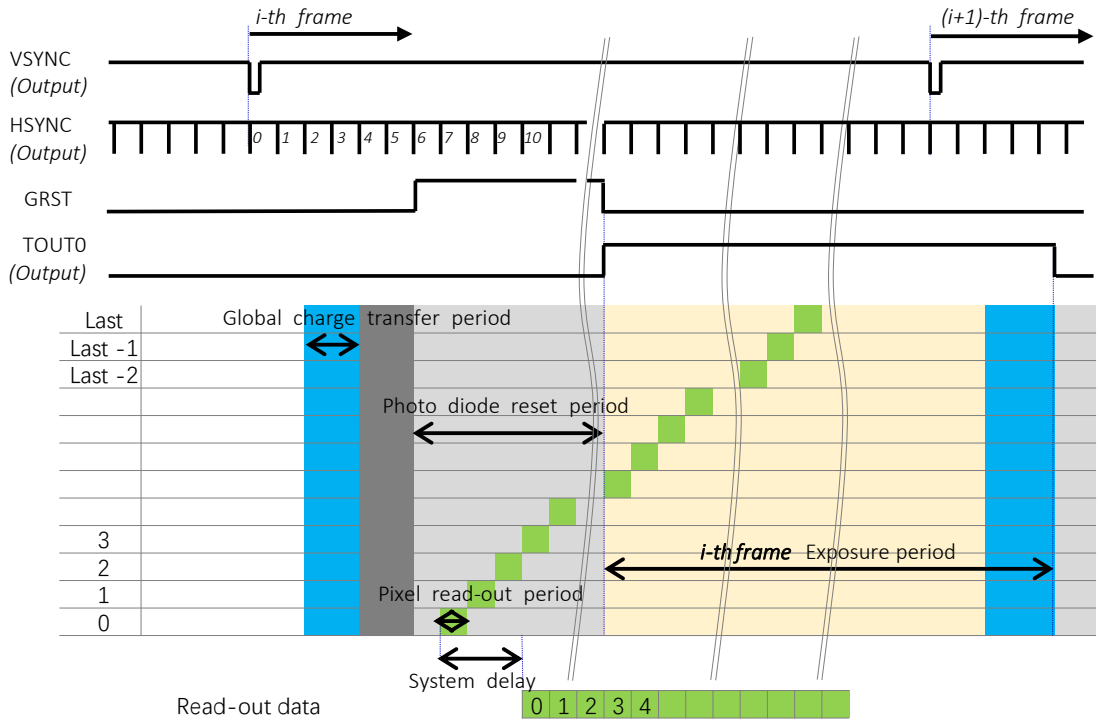


Figure 30.Timing diagram of internal expsoure time control

The exposure time is determined by the position of the falling edge of GRST (respect to pulse of VSYNC). The register settings and exposure time calculation is explained as following.

GRST falling edge:

The position of the falling edge is determined by the position of rising edge and the pulse width.

The position of rising edge respect to VSYNC pulse:

GRSTR[7:0], register 19[7:0], default value: 0x06(6d)

unit: one horizontal period

The width:

GRSTW[23:0], register 22[7:0], 23[7:0], 24[7:0], default value: 0x000001(1d)

unit: one horizontal period

Exposure time calculation:

The exposure time is the vertical period minus the width of GRST pulse. It is can be calculated by the following equation.

Exposure time = VP – GRSTW

unit: one horizontal period

*Please note, this is a rough calculation, if more precious calculation is preferred, please ask for technical support. As shown in the figure, the output pin TOUT0 is high during exposure period roughly indicates the start and end position of the exposure period.

External Exposure Time Control Mode

The exposure time can be also controlled by input pulse from pin TRIGEXP. This mode is only available at TRIGEXP mode. The charge transfer period, read out period and exposure time etc. are shown in the following figure.

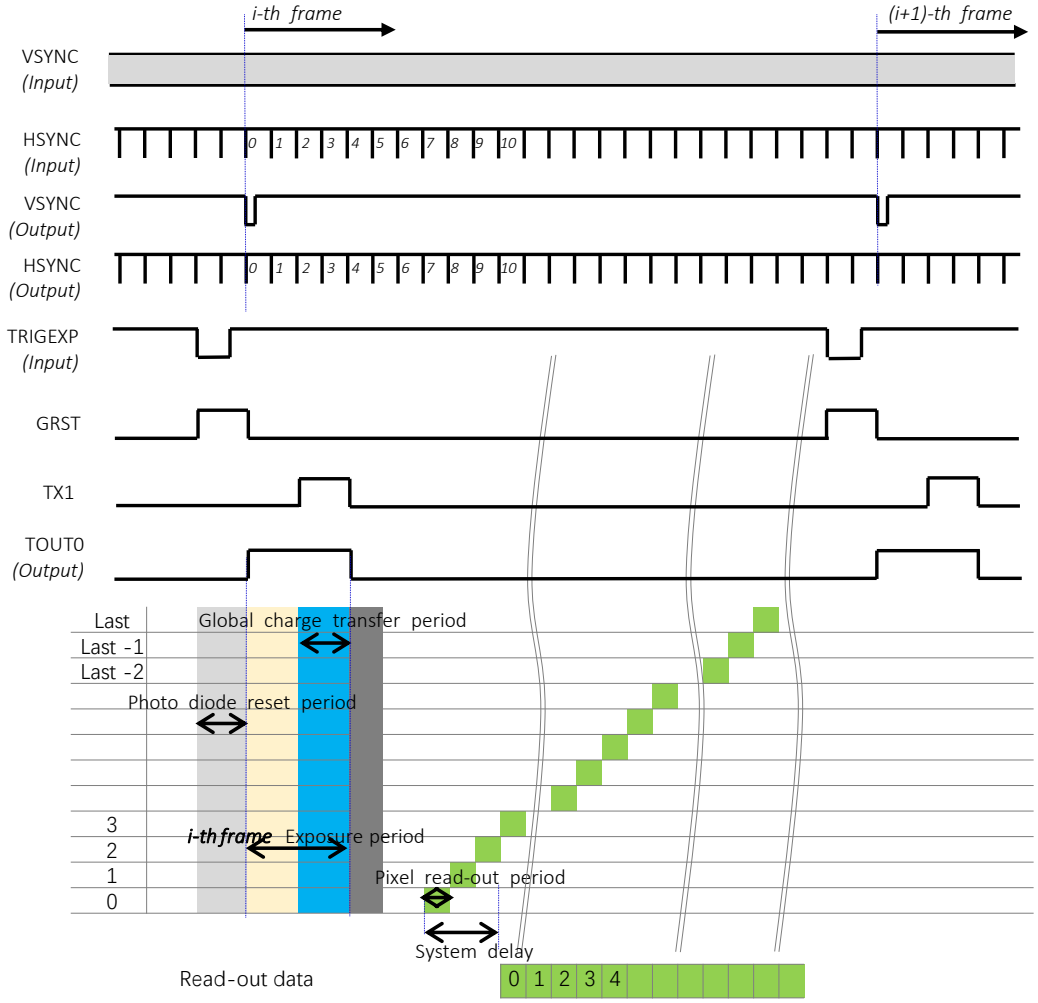


Figure 31.Timing diagram of external exposure time control

The exposure period, not same with the internal control mode, is determined by the low-level pulse width of TRIGEXP, the position of the falling edge of TX1 (respect to pulse of VSYNC) and the width of GRST. The register settings and exposure time calculation is explained as following.

TX1 falling edge:

The position of the falling edge is determined by the position of rising edge and the pulse width.

The position of rising edge respect to VSYNC pulse:

TX1R[7:0], register 25[7:0], default value: 0x01(1d)

unit: one horizontal period

The width:

TX1W[3:0], register 28[3:0], default value: 0x2(2d)

unit: one horizontal period

GRST width:

GRSTW1[3:0], register 46[7:4], default value: 0x2(2d), not same with the internal control mode

unit: one horizontal period

Exposure time calculation:

The exposure time is the low-level pulse width of TRIGEXP add the position of rising edge respect to VSYNC pulse and the width of TX1 pulse, then minus the width of GRST pulse. It is can be calculated by the following equation.

Exposure time = TRIGEXPW (low level pulse) + TX1R + TX1W – GRSTW1

unit: one horizontal period

*Please note, this is a rough calculation, if more precious calculation is preferred, please ask for technical support. As shown in the figure, the output pin TOUT0 is high during exposure period roughly indicates the start and end position of the exposure period.

Various Function Description

Windowing

The sensors support vertical multi-ROI windows, but does not support overlap windows. Since a smaller number of rows need to read out, vertical windowing can achieve higher frame rate. The pixel array supports vertical 9 ROI windows maximum in all, the VOB (Vertical Optical Black) pixel region supports vertical 1 ROI window, the active pixel region supports 8 vertical ROI windows maximum, the VOB pixel region and the active pixel region are independent.

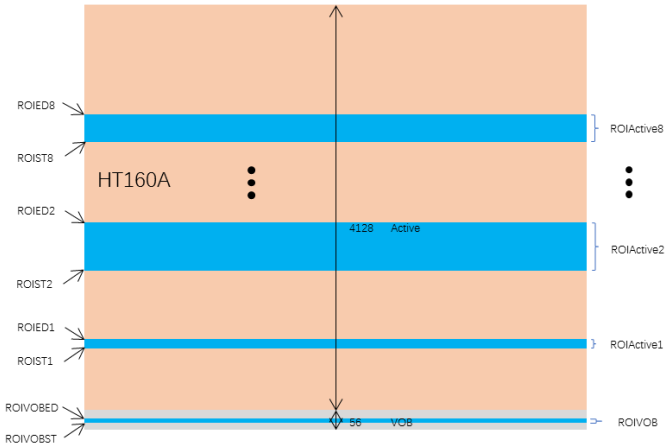


Figure 32.Multi-ROI of 160A-M

Start row and end row of every ROI window controlled by different registers, the detail requirements of the registers are shown in the following table.

Table 24. Register description of multi-ROI

Symbol	Registers set start row of the window *Note 1*	Registers set the end row of the window	Description	Note
ROIVOB	ROIVOBST	ROIVOBED	VOB pixel window	The number of rows in the window must be in multiple of 2 and not larger than 56.
ROIActive1~8	ROIST1~8	ROIED1~8	Active pixel window	The number of rows in the window must be in multiple of 2 and not larger than 4128 by 160A-M.

Note 1: The start row must be set smaller than or equal to the end row. If the start row is equal to the end row, this region does not support ROI windowing.
160A-M registers settings are shown in the following table.

Table 25. Register setting of multi-ROI of 160A-M

Register symbol	Register address	Range	Default value	Description
ROIVOBST[4:0]	104 [4:0]	≤27d	04h	Start row number: 2*ROIVOBST *Note 1 Note 2*
ROIVOBED[4:0]	105 [4:0]	≤28d	08h	End row number: 2*ROIVOBED-1 *Note 2*
ROIST1[11:0]	107[3:0], 106[7:0]	≤2063d	0004h	Start row number: 56+(2*ROIST1) *Note 2*
ROIED1[11:0]	109[3:0], 108[7:0]	≤2064d	080Ch	End row number: 56+(2*ROIED1-1) *Note 2*
ROIST2[11:0]	111[3:0], 110[7:0]	≤2063d	080Eh	Start row number: 56+(2*ROIST2) *Note 2*
ROIED2[11:0]	113[3:0], 112[7:0]	≤2064d	080Eh	End row number: 56+(2*ROIED2-1) *Note 2*
ROIST3[11:0]	115[3:0], 114[7:0]	≤2063d	080Eh	Start row number: 56+(2*ROIST3) *Note 2*
ROIED3[11:0]	117[3:0], 116[7:0]	≤2064d	080Eh	End row number: 56+(2*ROIED3-1) *Note 2*
ROIST4[11:0]	119[3:0], 118[7:0]	≤2063d	080Eh	Start row number: 56+(2*ROIST4) *Note 2*
ROIED4[11:0]	121[3:0], 120[7:0]	≤2064d	080Eh	End row number: 56+(2*ROIED4-1) *Note 2*
ROIST5[11:0]	123[3:0], 122[7:0]	≤2063d	080Eh	Start row number: 56+(2*ROIST5) *Note 2*
ROIED5[11:0]	125[3:0], 124[7:0]	≤2064d	080Eh	End row number: 56+(2*ROIED5-1) *Note 2*
ROIST6[11:0]	127[3:0], 126[7:0]	≤2063d	080Eh	Start row number: 56+(2*ROIST6) *Note 2*
ROIED6[11:0]	129[3:0], 128[7:0]	≤2064d	080Eh	End row number: 56+(2*ROIED6-1) *Note 2*
ROIST7[11:0]	131[3:0], 130[7:0]	≤2063d	080Eh	Start row number: 56+(2*ROIST7) *Note 2*
ROIED7[11:0]	133[3:0], 132[7:0]	≤2064d	080Eh	End row number: 56+(2*ROIED7-1) *Note 2*
ROIST8[11:0]	135[3:0], 134[7:0]	≤2063d	080Eh	Start row number: 56+(2*ROIST8) *Note 2*
ROIED8[11:0]	137[3:0], 136[7:0]	≤2064d	080Eh	End row number: 56+(2*ROIED8-1) *Note 2*

Note 1: The ROIVOBST here stands for the value of the register in decimal, the same for the other equations in this column.
Note 2: ROIVOBST, ROIVOBED, ROIST1~8 and ROIED1~8 must be set that their values are both odd or both even.

Gain

Programmable gain control consists of analog gain and digital gain control, the total of analog gain and digital gain can be set up to 48dB by register setting.

Analog Gain

The pixel signal is amplified by a programmable gain amplifier before input to ADC (Analog-to-Digital Converter). The gain of 1(0dB), 2(6dB) ,4(12dB) ,8(18dB) and 16(24dB) are available.

Table 27. Register setting of analog gain

Register name	Address and bit	Default value	Setting value and gain
PGAGAIN_T[5:0]	148[5:0]	2Fh	Analog gain of TOP region 2Fh: 1x 37h: 2x 3Bh: 4x 3Dh: 8x 3Eh: 16x
PGAGAIN_B[5:0]	147[5:0]	2Fh	Analog gain of BOTTOM region 2Fh: 1x 37h: 2x 3Bh: 4x 3Dh: 8x 3Eh: 16x

Digital Gain

The digital signal that shows the value of pixel signal is amplified in digital region before serializer and LVDS. The range of gain is 0~24dB by step of 0.1dB are available.

Table 28. Register setting of digital gain

Register name	Address and bit	Default value	Setting value	Gain
OUTDGAIN[7:0]	183[7:0]	00h	00h~F0h (0d~240d)	Gain(dB)=Setting value(d)/10

Test Pattern

The sensors can output a gray scale test pattern when set the register address 160[2:0] to25h. Its image draw is as shown below.

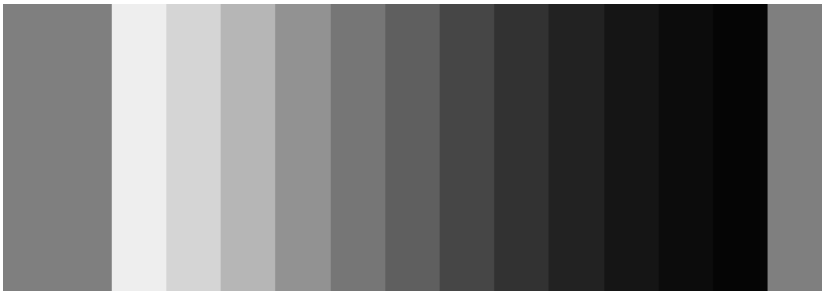


Figure 33.Gray scale chart

The pixel array is horizontally divided into 15 blocks, each block has different output as listed in the following table. Please note, when DWB is 10b, the upper 10 bits will be output.

Table 29. Pixel array output of gray scale chart

Block	1	2	3	4	5	6	7	8
Output (decimal)	2949	2949	15237	13599	11633	9339	7537	6062
Output (Hex)	B85	B85	3B85	351F	2D71	247B	1D71	17AE
Block	9	10	11	12	13	14	15	
Output (decimal)	4424	3113	2130	1311	655	328	2949	
Output (Hex)	1148	C29	852	51F	28F	148	B85	

LVDS Receiver Training Code Output

The sensors can send fixed code for the purpose of LVDS receiver training. The register settings are shown as below.

Table 30. Register setting of LVDS receiver training

Register name	Address and bit	Default value	Setting value
OUTTRNEN	191[6]	0b	0b: Training code output disable 1b: Training code output enable
OUTTRN[13:0]	191[5:0], 192[7:0]	70Fh	Change the default value if needed.
OUTSYNC_EN	191[7]	1b	0b: Sync code output disable 1b: Sync code output enable If sync code is not necessary, set to 0b.

Vertical/Horizontal Binning

The sensors support vertical 2-pixel FD binning mode and horizontal binning mode.

As vertical 2-pixel FD binning mode, because half rows to read out, it results in almost double frame rate. Please note, this mode will not increase the dynamic range.

As horizontal binning mode, because pixel architecture does not support 2×2 FD binning, horizontal binning mode cannot increase frame rate, only decrease LVDS outputs.

Vertical/Horizontal Sub-sampling

The sensors support vertical/horizontal 1/2 and 1/4 sub-sampling mode. This mode can achieve a higher frame rate without losing the basic information of the captured image.

As vertical 1/2 sub-sampling mode, because half rows to read out, it results in almost double frame rate.

As horizontal 1/2 sub-sampling mode cannot increase frame rate.

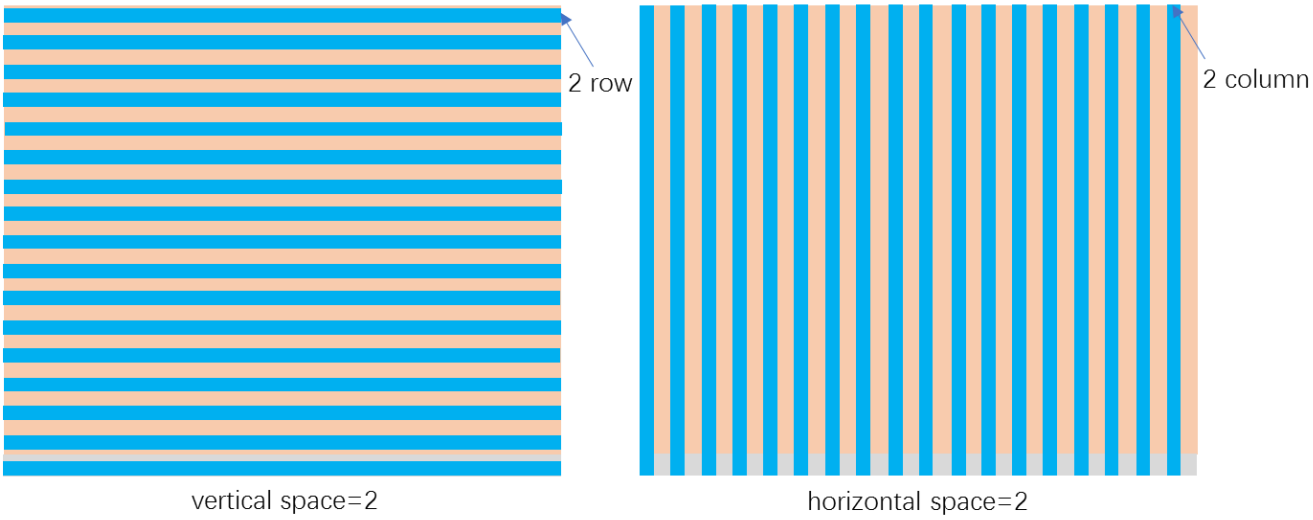


Figure 34. Vertical/Horizontal 1/2 sub-sampling mode

As vertical 1/4 sub-sampling mode, because 1/4 rows to read out, it results in almost fourfold frame rate.

As horizontal 1/4 sub-sampling mode cannot increase frame rate.

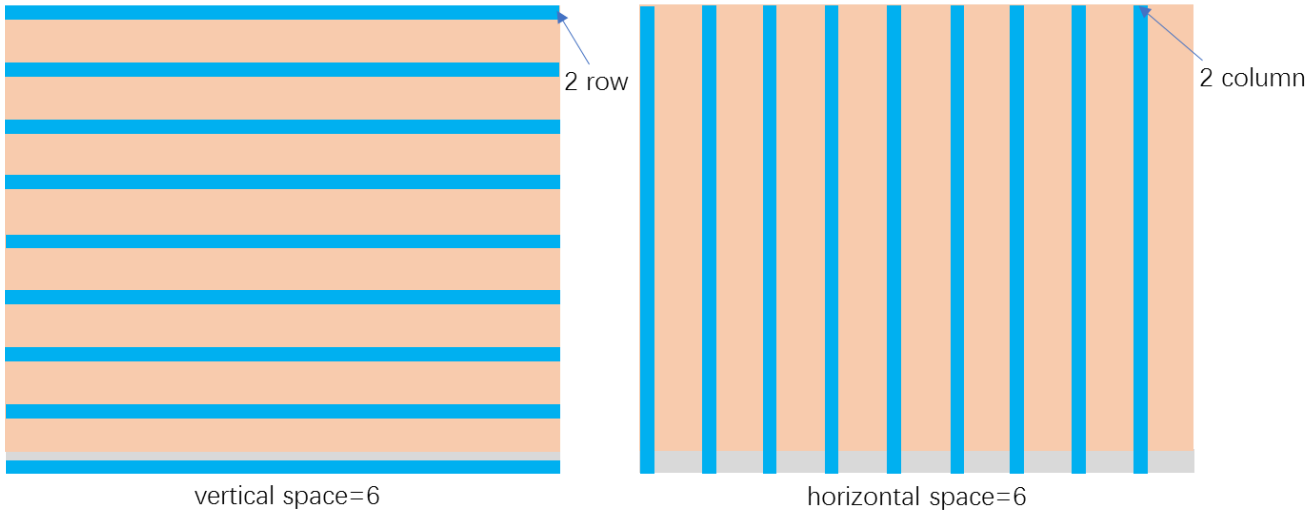


Figure 35. Vertical/Horizontal 1/4 sub-sampling mode

Vertical/Horizontal- Normal/Inverted readout

The sensors support vertical/horizontal- normal/inverted readout, details show in below.

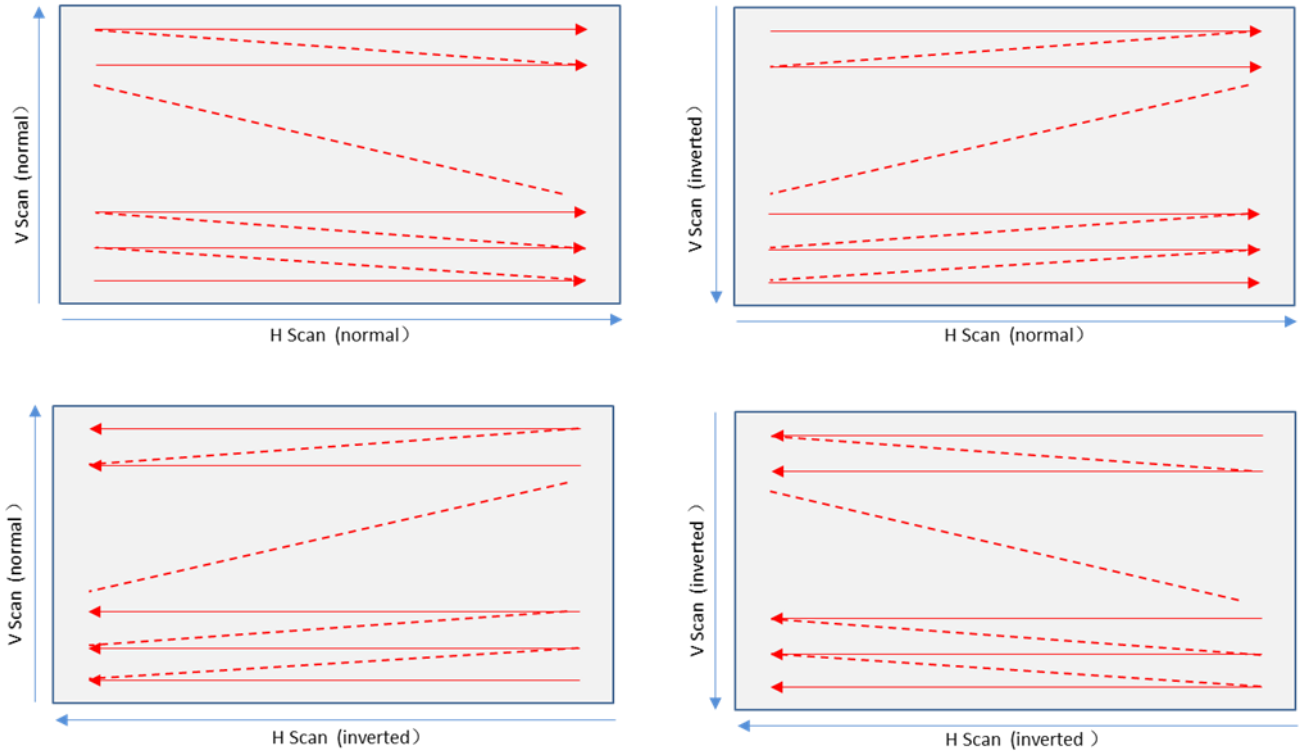


Figure 36. Detail of vertical/horizontal - normal/inverted readout

The sensors readout direction (normal/inverted) in vertical/horizontal can be switched by register setting.

Table 31. Register setting of vertical/horizontal - normal/inverted readout

Register name	Address and bit	Default value	Setting value
UPCTL	141[1]	1b	0b: Vertical inverted readout 1b: Vertical normal readout
HSCOP	162[2]	0b	0b: Horizontal normal readout 1b: Horizontal inverted readout

WDR mode

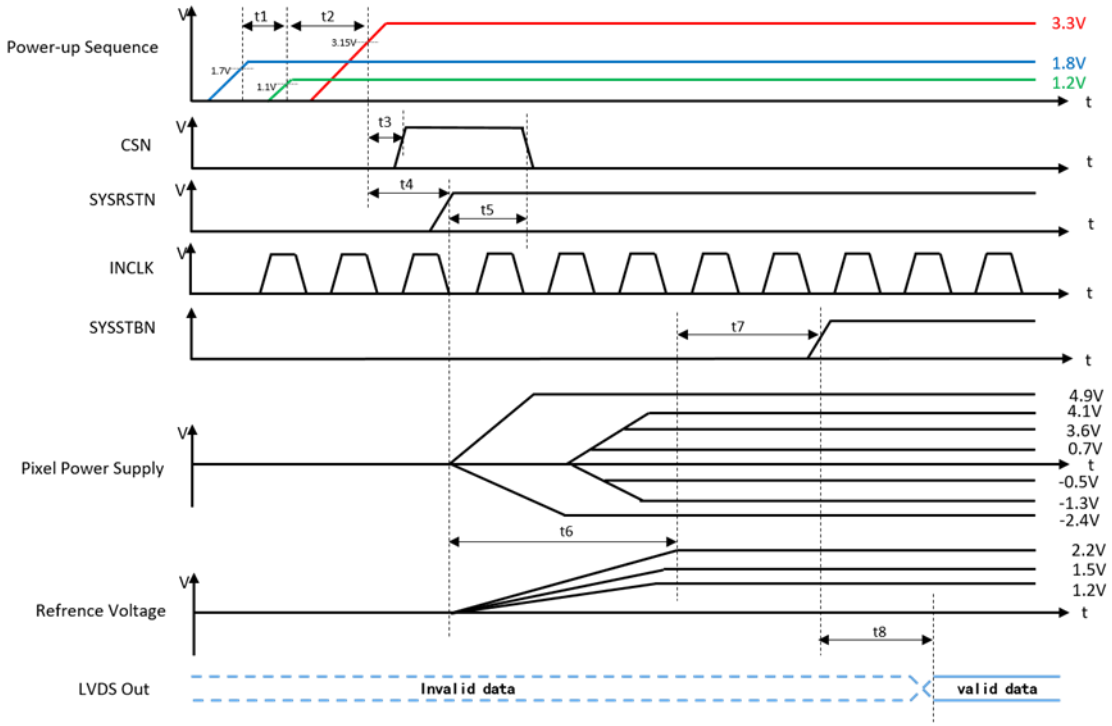
The sensors support three types of WDR (wide dynamic range) mode by allowing different exposure times for different frames. The surrounding system can combine different frames of different exposure times to generate a high dynamic range image.

Other Functions

Other functions listed below are also available, please ask for technical support or other document for details.
Digital offset
Digital saturation clip
Black sun clip

Power-On Sequence

It is recommended to turn on the power by the order of 1.8V(DV18 and DVDDL), 1.2V(DV12) and 3.3V(AV33).



#	min	unit	note
t1	0	ms	-
t2	0	ms	-
t3	0	us	-
t4	0.5	us	The time from external power-on to reset release
t5	20	us	Internal reset releasing time
t6	20	ms	Internal power on time
t7	0	us	Stand-by period before operation
t8	8	frame	The time from the stand-by release to valid data output.

Figure 37. Power-on sequence

Spectrum Response

T.B.D.

Package

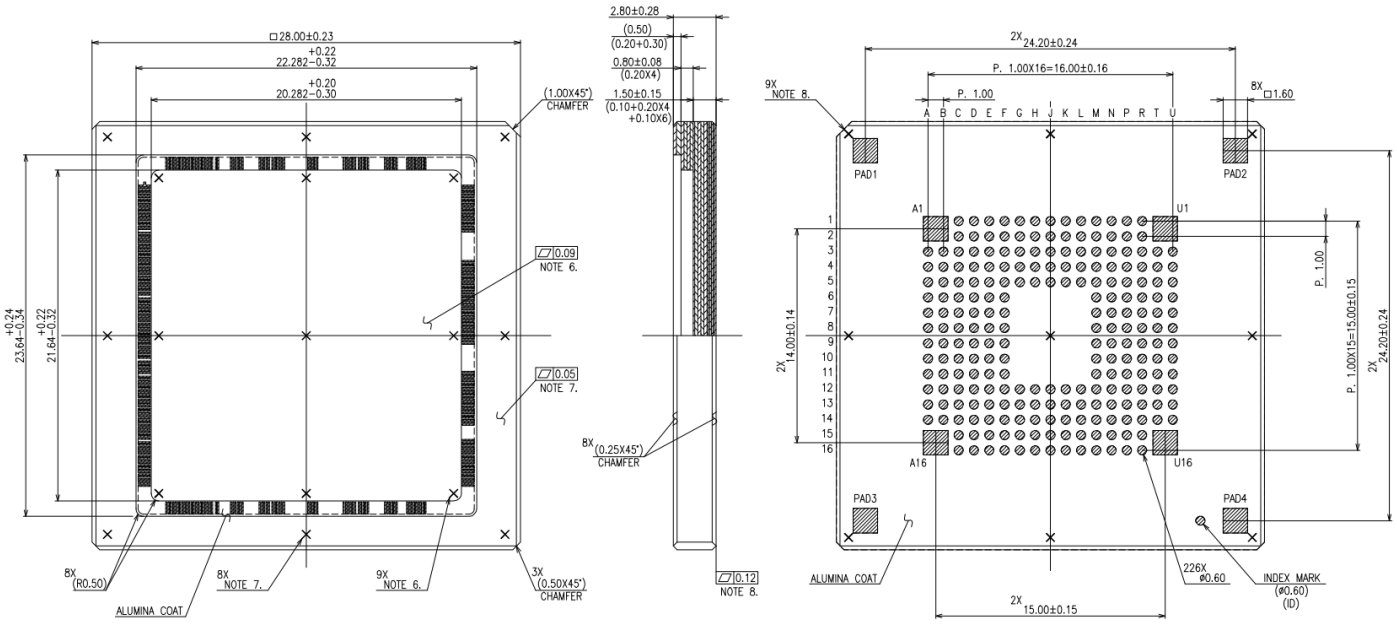


Figure 38. Detail of package

Note: Optical center is not the same with package center.

Document History

Version	Date	Description	Author
0.1	2020/08/19	New release	
1.5	2020/10/19	Update	
2.0	2020/12/18	Modify Input Reference Clock and Clock System and Image Output Data Format	