



# P-Channel 30-V (D-S) MOSFET

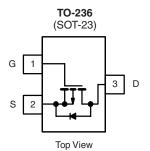
PRODUCT SUMMARY					
V <sub>DS</sub> (V)	$R_{DS(on)}\left(\Omega\right)$	I <sub>D</sub> (A) <sup>b</sup>			
- 30	0.078 at V <sub>GS</sub> = - 10 V	- 3.2			
	0.130 at V <sub>GS</sub> = - 4.5 V	- 2.5			

#### **FEATURES**

- Halogen-free Option Available
- TrenchFET® Power MOSFET







# Si2307BDS (L7)\* \* Marking Code

Warking Code

Ordering Information: Si2307BDS-T1-E3 (Lead (Pb)-free)

Si2307BDS-T1-GE3 (Lead (Pb)-free and Halogen-free)

<b>ABSOLUTE MAXIMUM RATINGS</b>	T <sub>A</sub> = 25 °C, unles	ss otherwise r	noted		
Parameter		Symbol	5 s	Steady State	Unit
Drain-Source Voltage		V <sub>DS</sub>	- 30		
Gate-Source Voltage		V <sub>GS</sub>	± 20		V
Out in the Comment (T. 150 20)h	T <sub>A</sub> = 25 °C	- I <sub>D</sub>	- 3.2	- 2.5	
Continuous Drain Current (T <sub>J</sub> = 150 °C) <sup>b</sup>	T <sub>A</sub> = 70 °C		- 2.6	- 2.0	
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	- 12		Α
Continuous Source Current (Diode Conduction) <sup>b</sup>		I <sub>S</sub>	- 1.25	- 0.75	
D D' ' ' ' ' '	T <sub>A</sub> = 25 °C	P <sub>D</sub>	1.25	0.75	W
Power Dissipation <sup>b</sup>	T <sub>A</sub> = 70 °C		0.8	0.48	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	- 55 to 150		°C

THERMAL RESISTANCE RATINGS						
Parameter	Symbol	Typical	Maximum	Unit		
Maximum Junction-to-Ambient <sup>b</sup>	- R <sub>thJA</sub>	80	100	°C/W		
Maximum Junction-to-Ambient <sup>c</sup>	' 'thJA	130	166	C/VV		

#### Notes:

- a. Pulse width limited by maximum junction temperature.
- b. Surface Mounted on FR4 board,  $t \le 5$  s.
- c. Surface Mounted on FR4 board.

For SPICE model information via the Worldwide Web: http://www.vishay.com/www/product/spice.htm

## **Si2307BDS**

# Vishay Siliconix



<b>SPECIFICATIONS</b> $T_J = 25$			Limits				
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static	<u> </u>						
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0 \text{ V, } I_D = -10  \mu\text{A}$	- 30			V	
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = -250 \mu A$	- 1.0		- 3.0	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zana Oata Wallana Buais Oamant		$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$			- 1	T	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			- 10	μΑ	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \le -10 \text{ V}, V_{GS} = -10 \text{ V}$	- 6			Α	
	<u> </u>	$V_{GS} = -10 \text{ V}, I_D = -3.2 \text{ A}$		0.063	0.078	Ω	
Drain-Source On-Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = -4.5 \text{ V}, I_D = -2.5 \text{ A}$		0.105	0.130		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	$V_{DS} = -10 \text{ V}, I_D = -3.2 \text{ A}$		5.0		S	
Diode Forward Voltage	V <sub>SD</sub>	I <sub>S</sub> = - 0.75 A, V <sub>GS</sub> = 0 V		- 0.85	- 1.2	V	
Dynamic <sup>b</sup>	<u> </u>			1			
Total Gate Charge	Qg	V 45.V.V 46.V		9.0	15	nC	
Gate-Source Charge	Q <sub>gs</sub>	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}$ $I_{D} \cong -1.7 \text{ A}$		1.4			
Gate-Drain Charge	$Q_{gd}$	ID = - 1.7 A		2.4		1	
Gate Resistance	$R_{g}$	f = 1.0 MHz		8.0		Ω	
Input Capacitance	C <sub>iss</sub>			380			
Output Capacitance	C <sub>oss</sub>	$V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		100		pF	
Reverse Transfer Capacitance	C <sub>rss</sub>			75		1	
Switching <sup>c</sup>				1	L		
Turn-On Time	t <sub>d(on)</sub>			9	20		
	t <sub>r</sub>	$V_{DD} = -15 \text{ V}, R_L = 15 \Omega$		12	20	1	
Turn-Off Time	t <sub>d(off)</sub>	$I_D \cong$ - 1.0 A, $V_{GEN}$ = - 4.5 V $R_a$ = 6 $\Omega$		25	40	ns	
	t <sub>f</sub>	1 ig = 0 32		14	21	1	

#### Notes:

- a. Pulse test: pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %.
- b. For DESIGN AID ONLY, not subject to production testing.
- c. Switching time is essentially independent of operating temperature.

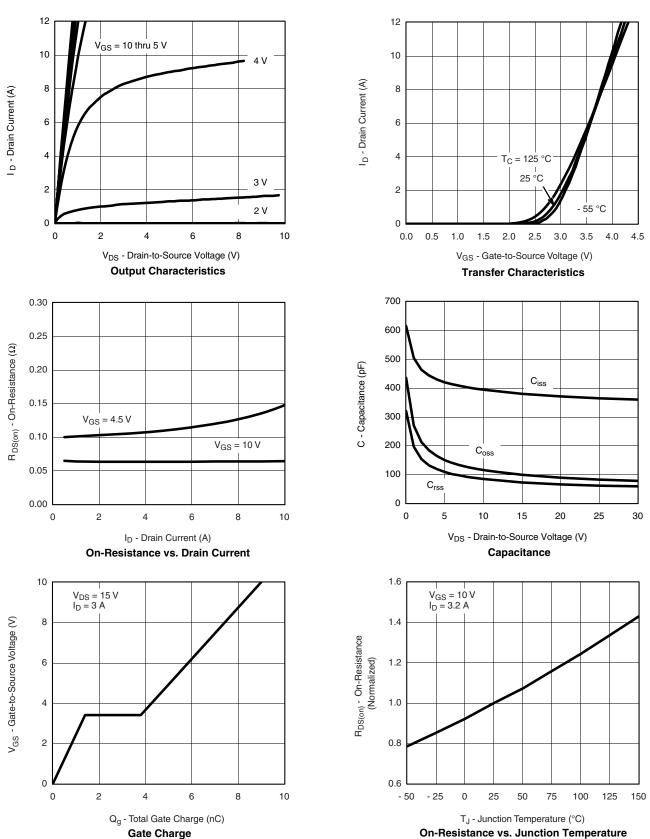
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.





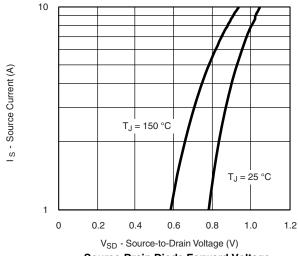


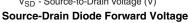
## TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

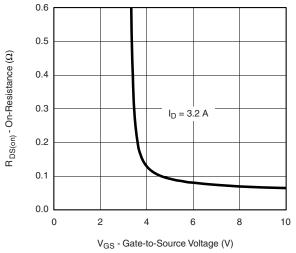


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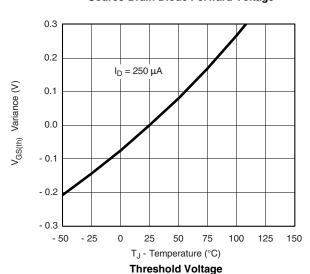
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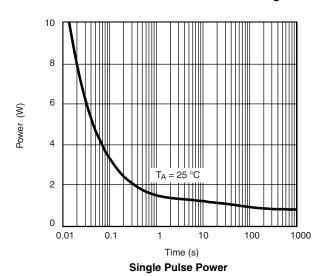


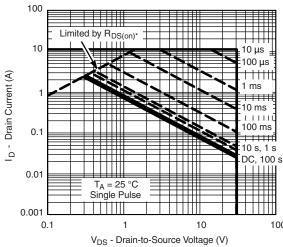




On-Resistance vs. Gate-to-Source Voltage





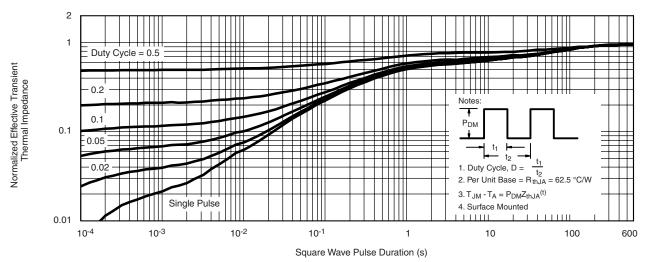


\*  $V_{GS}$  > minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified Square Wave Pulse Duration (s)

Safe Operating Area, Junction-to-Case



### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?72699">http://www.vishay.com/ppg?72699</a>.

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## SOT-23 (TO-236): 3-LEAD







Dim	MILLI	METERS	INCHES			
	Min	Max	Min	Max		
Α	0.89	1.12	0.035	0.044		
A <sub>1</sub>	0.01	0.10	0.0004	0.004		
A <sub>2</sub>	0.88	1.02	0.0346	0.040		
b	0.35	0.50	0.014	0.020		
С	0.085	0.18	0.003	0.007		
D	2.80	3.04	0.110	0.120		
E	2.10	2.64	0.083	0.104		
E <sub>1</sub>	1.20	1.40	0.047	0.055		
е	0.9	0.95 BSC		0.0374 Ref		
e <sub>1</sub>	1.90 BSC		0.0748 Ref			
L	0.40	0.60	0.016	0.024		
L <sub>1</sub>	0.64 Ref		0.025 Ref			
S	0.50 Ref		0.020 Ref			
q	3°	8°	3°	8°		
FCN: S-03946-Rev K 09-	lul-01	•				

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DWG: 5479

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### **RECOMMENDED MINIMUM PADS FOR SOT-23**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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