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Zhejiang University
Oct.1, 2017

IEEE ENERGY CONVERSION CONGRESS & EXPO
ECCE 2017 Cincinnati OHIO October 1–5

国产品牌碳化硅MOS单管选型目录，直销热线18928433735

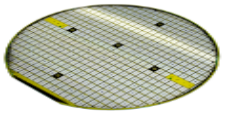
Product Type1	Model Name	Package	Voltage	R_{on}	Temperature Range	Status
SiC Chips	ASC8N650MT3	TO-247-3	650V	320mohm	-40~150°C	Development
	ASC12N650MT3	TO-247-3	650V	245mohm	-40~150°C	Development
	ASC20N650MT3	TO-247-3	650V	130mohm	-40~150°C	Development
	ASC60N650MT3	TO-247-3	650V	35mohm	-40~150°C	Product
	ASC60N650MT4	TO-247-4	650V	35mohm	-40~150°C	Product
	ASC60N650MD8	DFN8*8	650V	35mohm	-40~150°C	Product
	ASC100N650MT3	TO-247-3	650V	15mohm	-40~150°C	Product
	ASC100N650MT4	TO-247-4	650V	15mohm	-40~150°C	Product
	ASC60N900MT3	TO-247-3	900V	36mohm	-40~150°C	Product
	ASC60N900MT4	TO-247-4	900V	36mohm	-40~150°C	Product
	ASC100N900MT3	TO-247-3	900V	16mohm	-40~150°C	Product
	ASC100N900MT4	TO-247-4	900V	16mohm	-40~150°C	Product
	ASC5N1200MT3	TO-247-3	1200V	350mohm	-40~150°C	Development
	ASC10N1200MT3	TO-247-3	1200V	280mohm	-40~150°C	Development
	ASC18N1200MT3	TO-247-3	1200V	160mohm	-40~150°C	Development
	ASC30N1200MT3	TO-247-3	1200V	80mohm	-40~150°C	Product
	ASC30N1200MT4	TO-247-4	1200V	80mohm	-40~150°C	Product
	ASC60N1200MT3	TO-247-3	1200V	40mohm	-40~150°C	Product
	ASC60N1200MT4	TO-247-4	1200V	40mohm	-40~150°C	Product
	ASC60N1200MD8	DFN8*8	1200V	40mohm	-40~150°C	Product
	ASC100N1200MD10	DFN10*12	1200V	17mohm	-40~150°C	Product
	ASC100N1200MT3	TO-247-3	1200V	17mohm	-40~150°C	Product
	ASC100N1200MT4	TO-247-4	1200V	17mohm	-40~150°C	Product
	ASC5N1700MT3	TO-247-3	1700V	1000mohm	-40~150°C	Development
	ASC100N1700MT3	TO247	1700V	20mohm	-40~150°C	Product
	ASC20N3300MT4	TO247-4L	3300V	200mohm	-40~150°C	Product

SiC MOS芯片

芯片特性

全系列采用6英寸晶圆量产
最高耐压3300V
最低内阻15毫欧
高雪崩耐量，100% UIS测试
满足车规级要求：按照AEC-Q101标准测试

公 众 号



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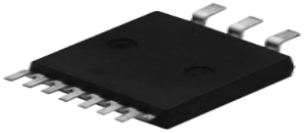
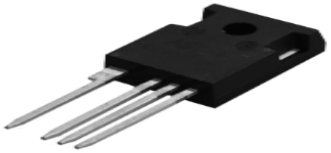


TO268
产品系列在开发中



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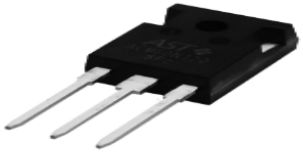

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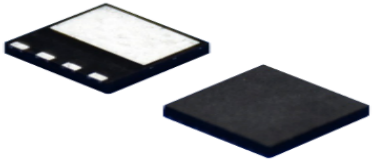


DFN8*8

碳化硅MOS管

Product Type	Model Name	Package	Voltage	R_{on}	Application	Status
SiC Chips	ASC8N650MT3	DFN5x6	650V	320mohm	PD快充	Product
	ASC12N650MT3	DFN5x6	650V	245mohm	PD快充	Development
	ASC20N650MT3	DFN8x8	650V	130mohm	PD快充	Development
	ASC40N650MT4	TO-247-4	650V	60mohm	OBC	Product
	ASC100N650MT3	TO-247-3	650V	15mohm	电源及快速充电桩	Product
	ASC100N650MT4	TO-247-4	650V	15mohm	电源及快速充电桩	Product
	ASC20N1200MT3	TO-247-3	1200V	150mohm	光伏逆变	Development
	ASC30N1200MT3	TO-247-3	1200V	80mohm	OBC	Product
	ASC30N1200MT4	TO-247-4	1200V	80mohm	OBC	Product
	ASC60N1200MT4	TO-247-4	1200V	40mohm	OBC及光伏逆变	Product
	ASC100N1200MD10	DFN10*12	1200V	17mohm	电源	Product
	ASC100N1200MT3	TO-247-3	1200V	17mohm	电源及快速充电桩	Product
	ASC100N1200MT4	TO-247-4	1200V	17mohm	电源及快速充电桩	Product
	ASC5N1700MT3	TO-247-3	1700V	1000mohm	光伏逆变	Product
	ASC100N1700MT4	TO247-4	1700V	20mohm	电源	Product
	ASC20N3300MT4	TO247-4L	3300V	200mohm	电源	Product

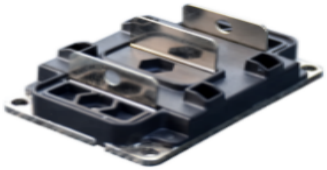
SiC 模块

Product Type	Model Name	Package	Voltage	R_{on}	Structure	Status
SiC Modules	ASC200N1200	Easypim	1200V	11mohm	半桥	Product
	ASC100N1200	Easypim	1200V	20mohm	三相全桥	Product
	ASC300N1200	HP1	1200V	6.7mohm	三相全桥	Product
	ASC600N1200	HP1/DWC3	1200V	3.3mohm	三相全桥	Product
	AC300N650	Econodual	650V	6.7mohm	半桥	Product
	ASC800N1200	Econodual	1200V	2.2mohm	半桥	Product
	ASC800N1200	HPD	1200V	2.2mohm	三相全桥	Product
	ASC600N1200	HPD	1200V	2.9mohm	三相全桥	Product

SiC MOS模块

模块特性

最高结温175℃
正温度系数
氮化铝绝缘基板
直接水冷散热
集成负温度系数传感器
2.5KV绝缘电压



XM3

EASYPIM

Econodual

HP1

HPD

DWC3

Outline

- Basics of Bidirectional DC/DC converters
- Modulation of DAB converter
- Synthesizing Phase-shift Bidirectional DC/DC converters
- Bidirectional DC/DC converter with PWM plus phase-shift control
- DAB Converter with resonant tank
- Summary

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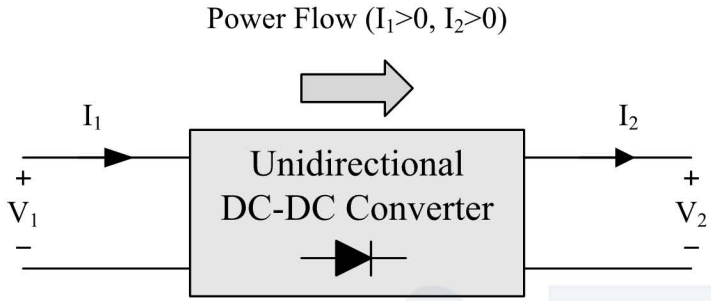
Chapter 1
Basics of Bidirectional DC/DC converters

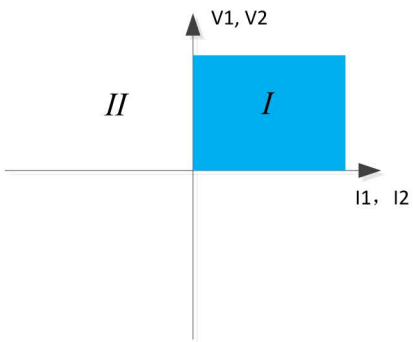
Outline

- Concept of bidirectional DC/DC conversion
- Classification of bidirectional DC/DC converters
- Requirement to bidirectional DC/DC converters

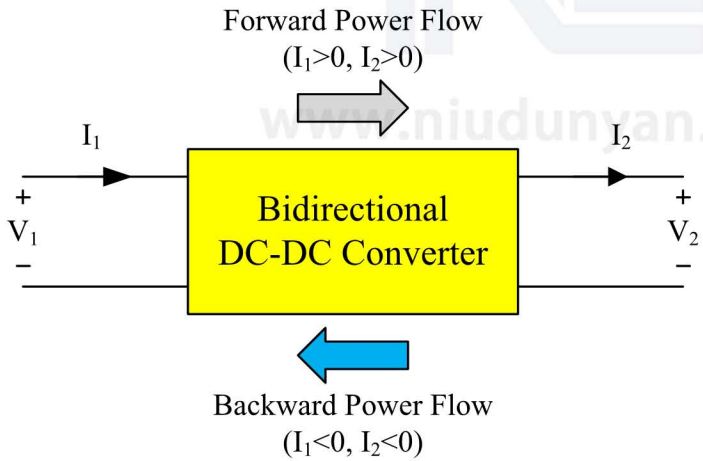
Concept of Bi-directional DC/DC Conversion

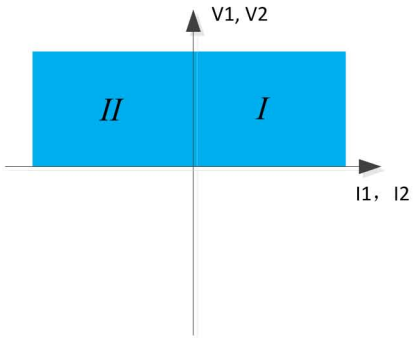
One directional conversion:





Bi-directional conversion:

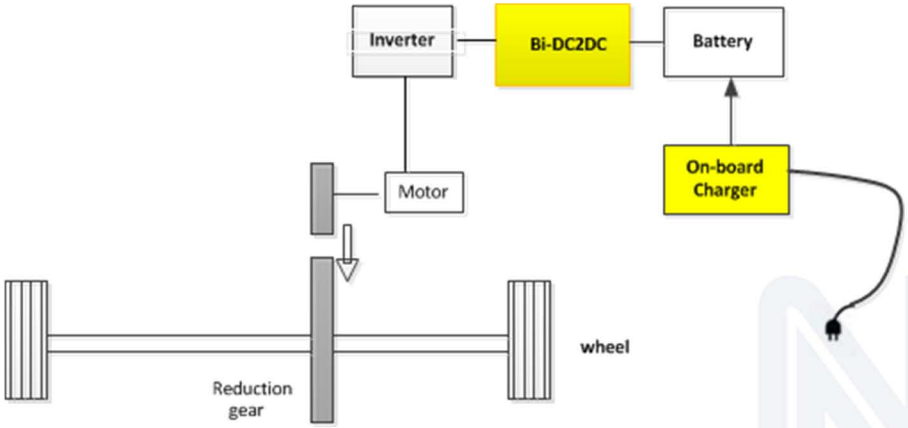




- Polarity of both input and output port voltages are always the same and fixed
- Port voltages are variable
- It operates at both the first quadrant and the second quadrant in V-I plane

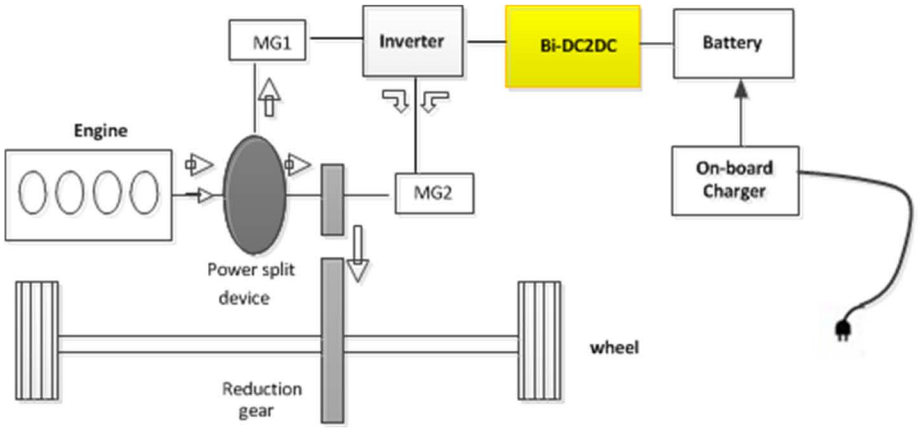
Electric Vehicle

Battery EV

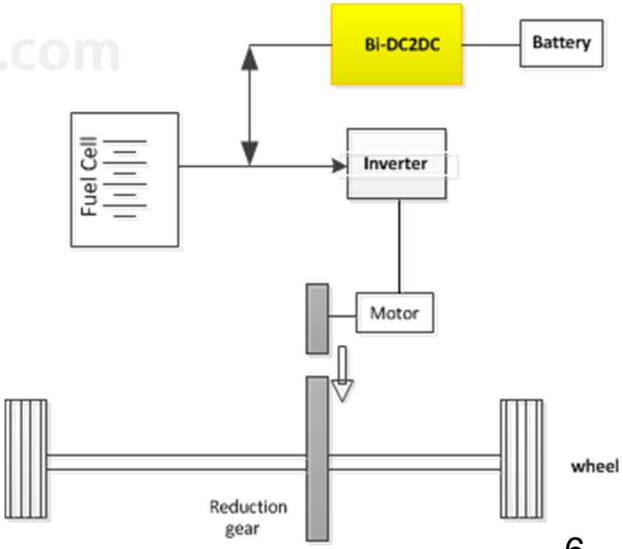


- Battery EV
- HEV or Plug-in HEV
- Fuel Cell Vehicle
- V2G charger

Plug-in HEV



Fuel Cell EV



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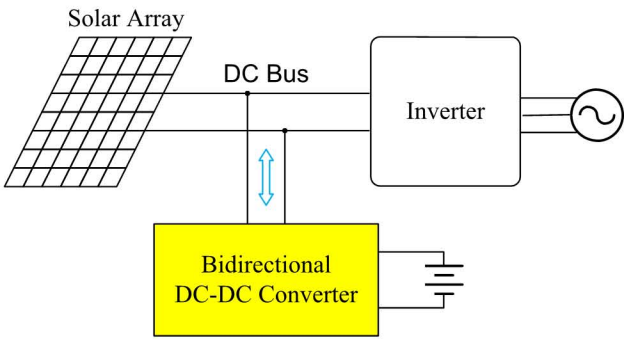
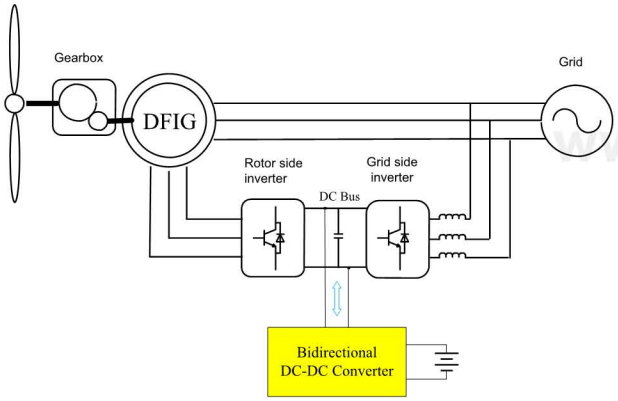
Distributed Power Generation

- Wind or Solar inverter with Battery
- BESS
- DC SST for DC grid or off Shore wind farm
- SST

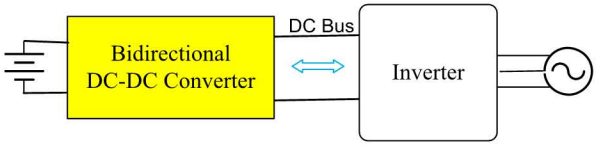
PV inverter w/ Battery storage



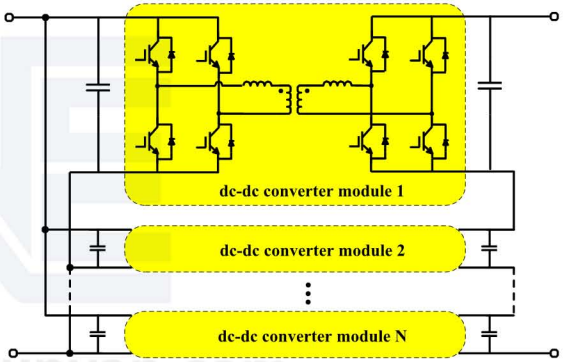
Wind turbine w/ battery storage



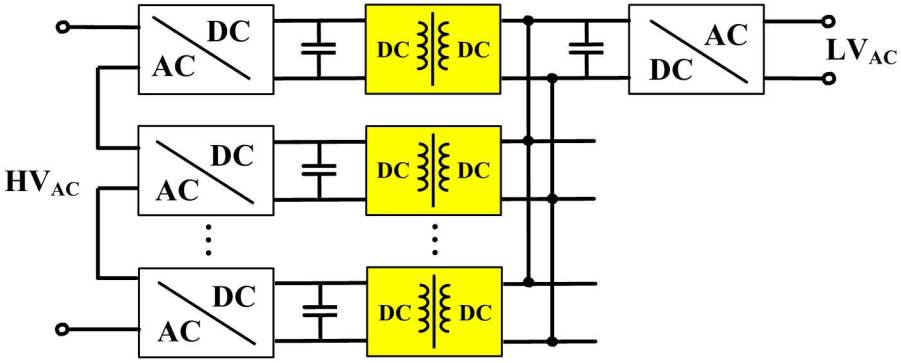
BESS



DC Solid State transformer



AC Solid State transformer



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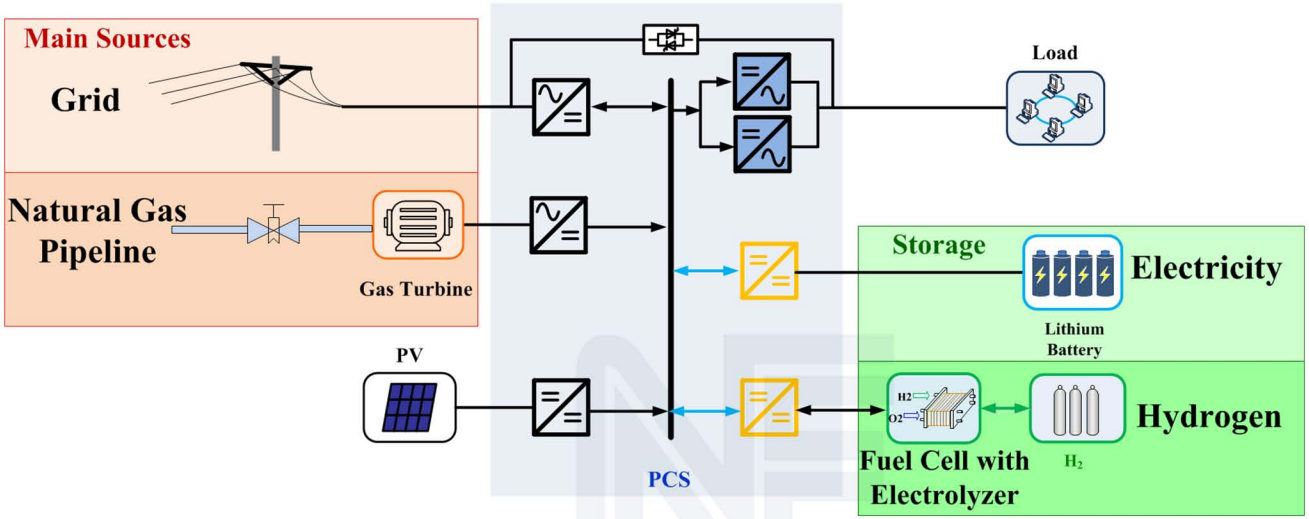
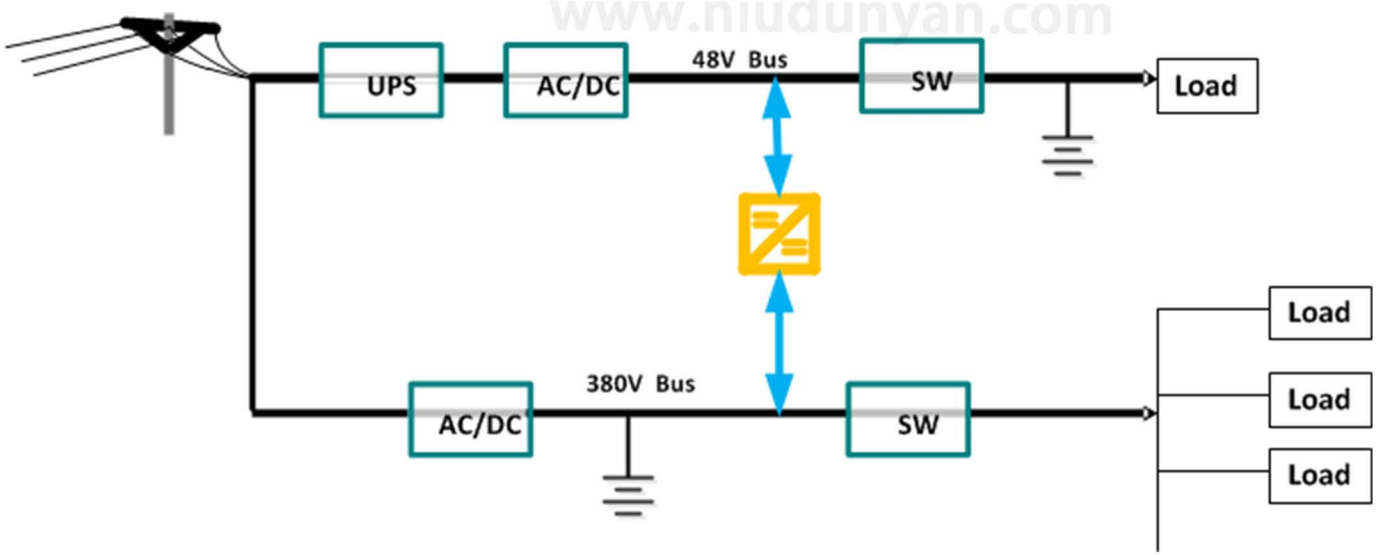
Data Center Power Supply



- HVDC
- UPS



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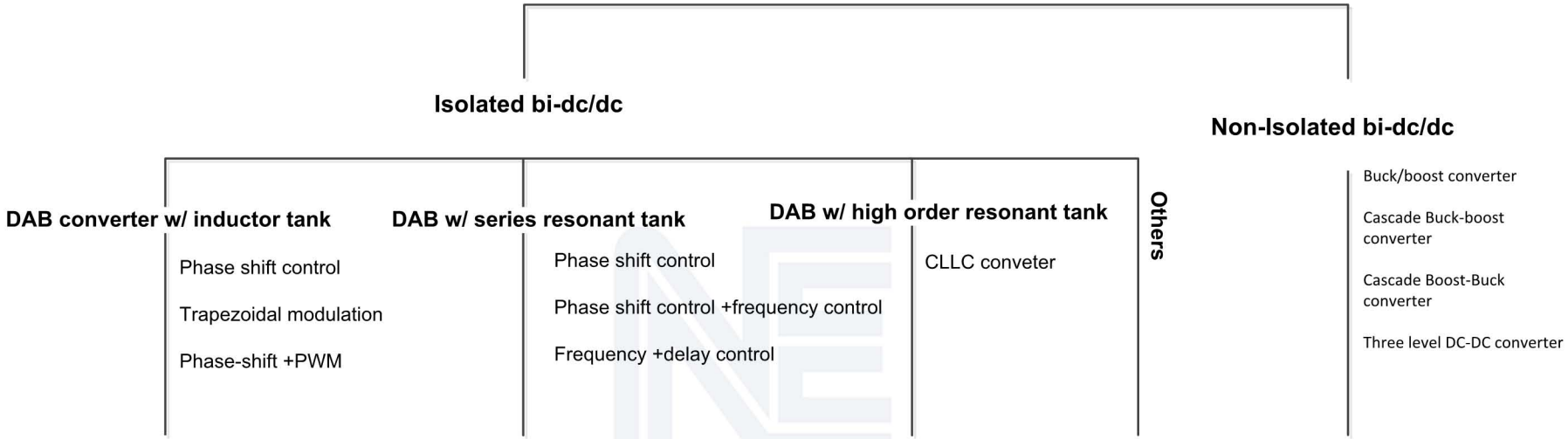
Classification of bidirectional DC/DC converters



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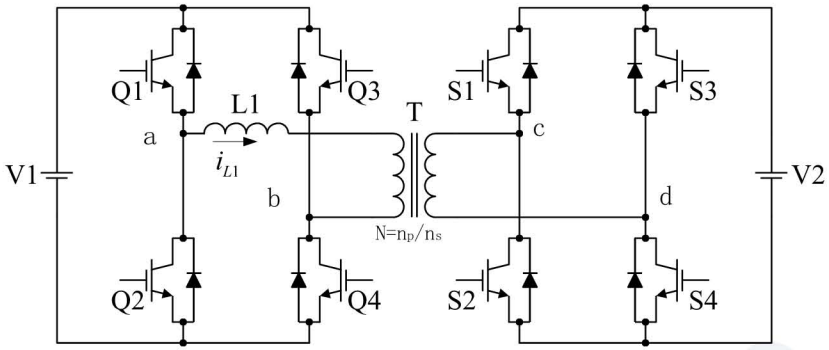
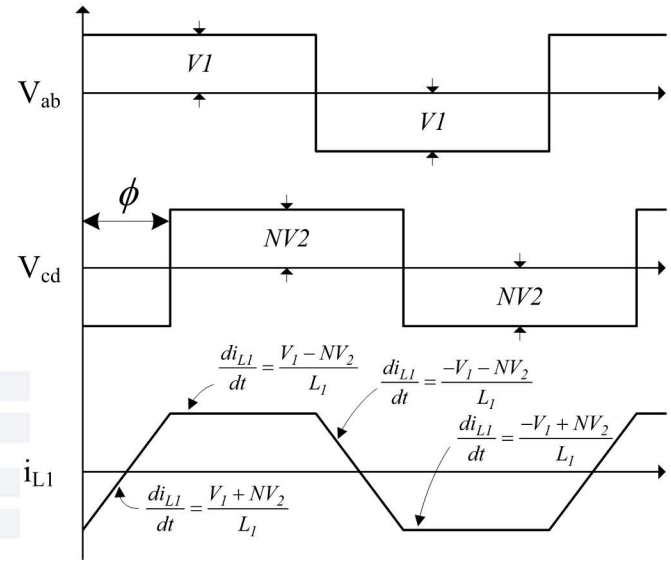
*DAB: Dual Active Bridge means that two full bridge converters are connected with back to back through passive tank.
*In this tutorial, Active Bridge of DAB means any circuits can generate square-wave or pseudo square-wave such as full bridge, 3 phase inverter, half bridge, current fed bridge etc.

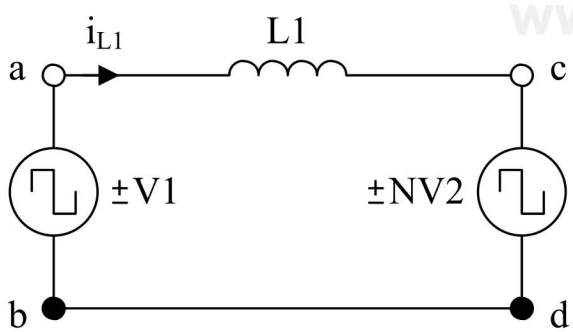
DAB converter with inductor tank

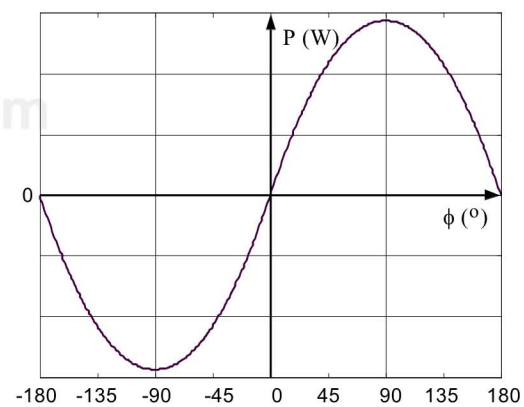




$$N=\frac{n_p}{n_s}$$ Transformer turn-ratio

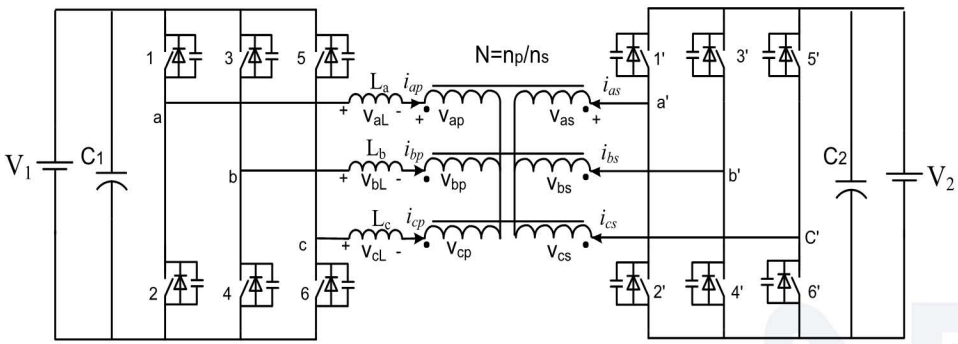
ϕ Phase shift between the primary and secondary

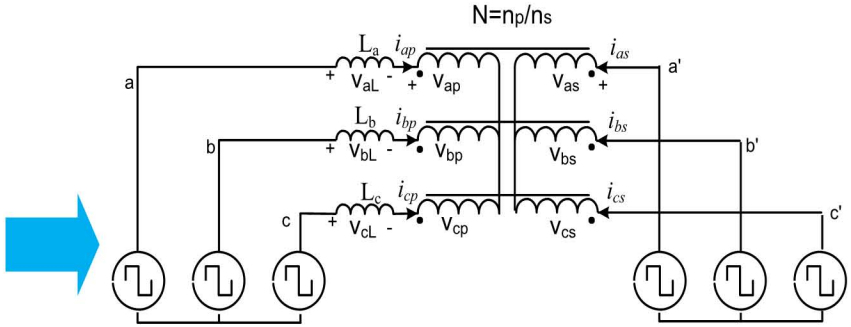




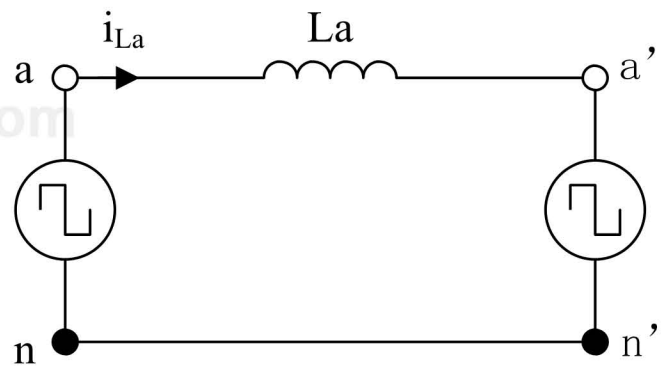
- Power flow can be adjusted with phase shift
- Bidirectional power flow with buck-boost capability
- fixed-frequency operation
- Zero voltage switching(ZVS) for all switches in ideal condition

Extension to three-phase DAB converter





- For primary side converter, Va, Vb, and Vc are all square waves with evenly phase angle shift degree
- If we ignore the coupling between phases, it can be simplified as three separate DAB converters

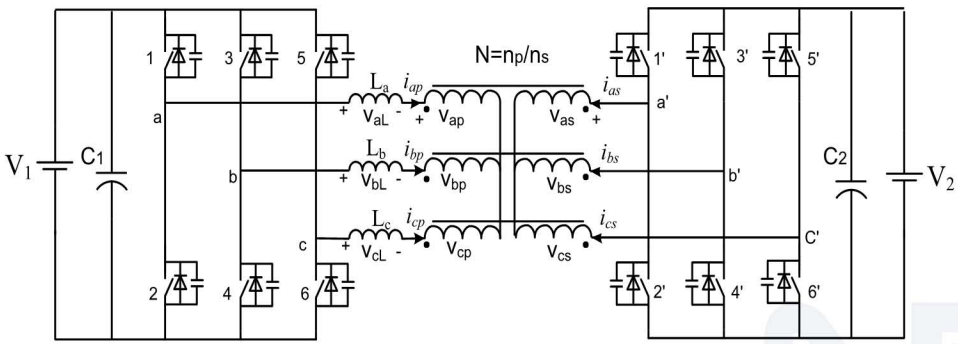


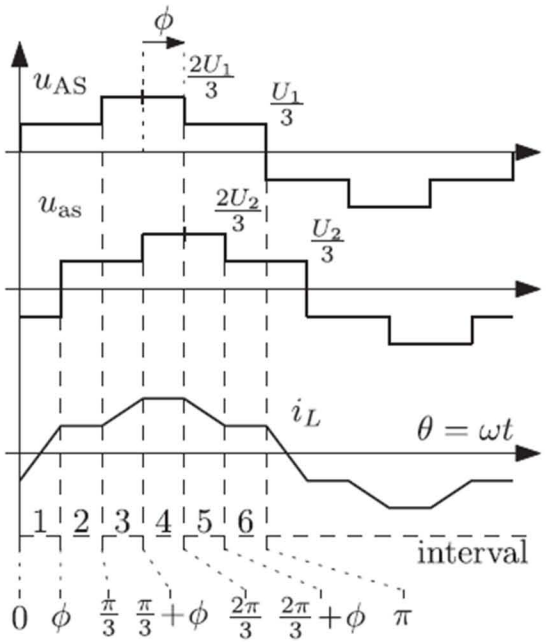
Advantages

- Triple switching frequency in DC filter capacitors ripple
- More sinusoidal ac-link current
- Lower rms and turn-off currents in the switch due to divided power over three phases
- Higher transformer utilization(single phase transformer has more magnetic core material and more hysteresis losses due to the absence of the flux canceling effect)

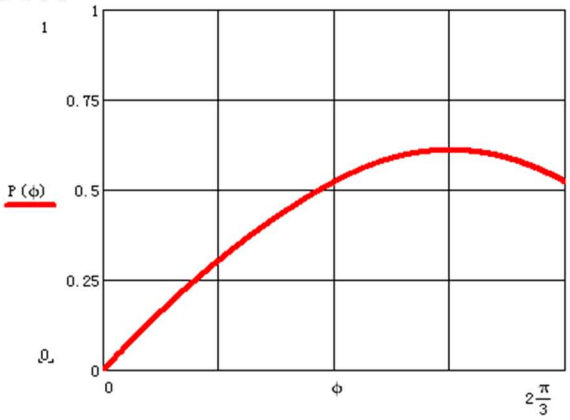
*Rik De Doncker, Deepakraj Divan, etal, Transaction IA, 1991

Power vs. Phase-shift





$$P(\phi) = \begin{cases} \dfrac{V_1 V_2^{'}}{\omega L}\phi\left(\dfrac{2}{3} - \dfrac{\phi}{2\pi}\right) & 0 \le \phi \le \dfrac{\pi}{3} \\ \dfrac{V_1 V_2^{'}}{\omega L}\left(\phi - \dfrac{\phi^2}{\pi} - \dfrac{\pi}{18}\right) & \dfrac{\pi}{3} \le \phi \le \dfrac{2\pi}{3} \end{cases}$$



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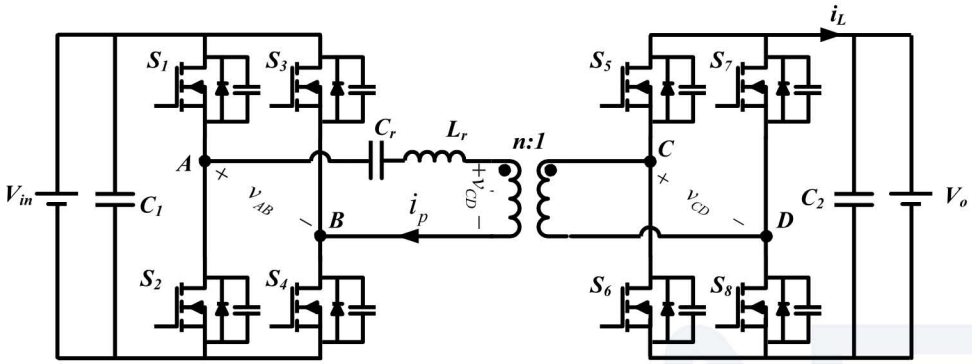
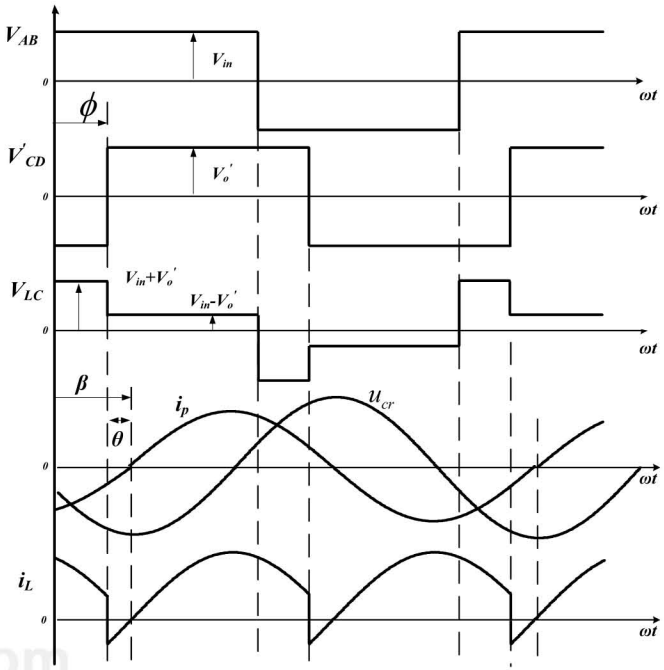
DAB with Series Resonant Tank(DABSRT)





- Shape the tank waveform into sinusoidal
- ZVS obtained with wide input/output voltage variation
- No transformer saturation due to series capacitor
- Combining phase-shift control with frequency control to minimize circulation current and extend the ZVS range

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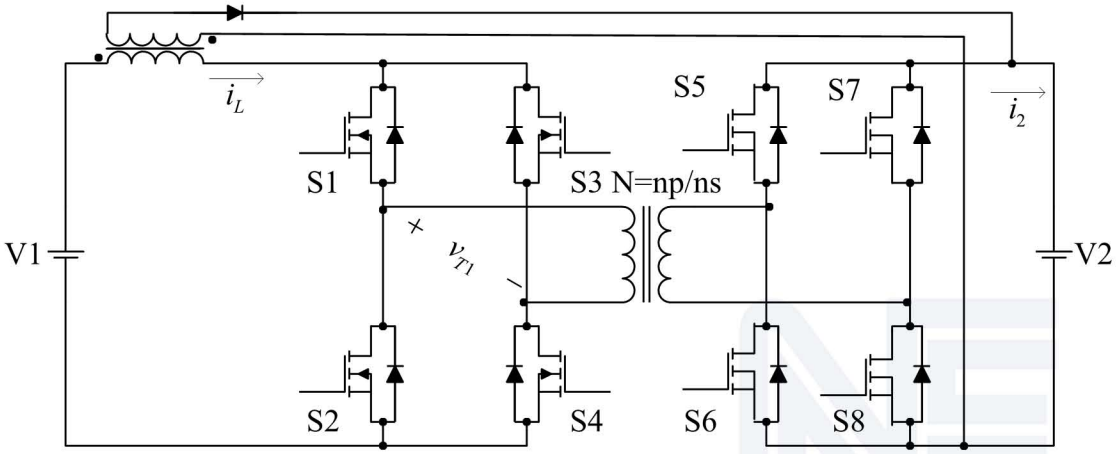
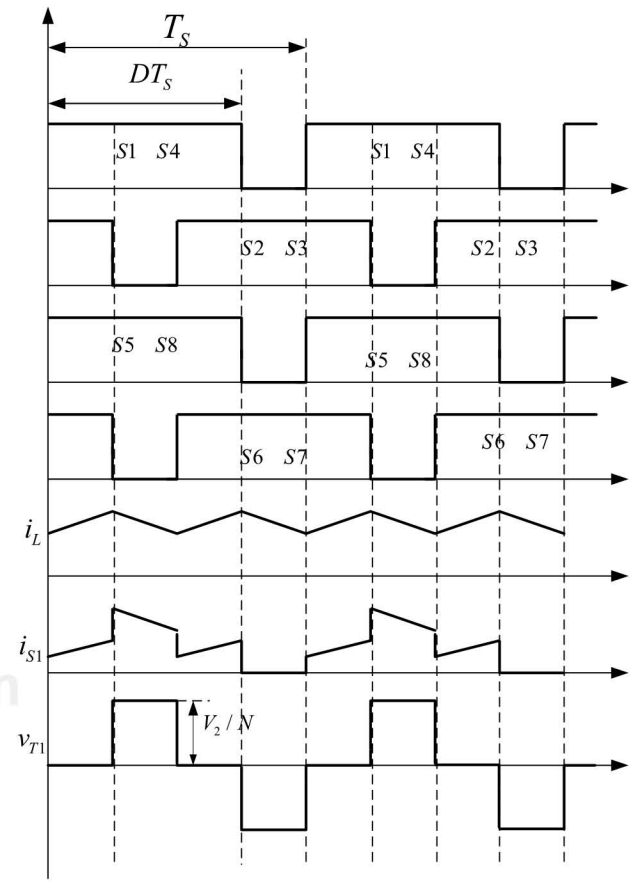
@Xiaodong Li, Ashoka K. S. Bhat, IEEE trans. PE, 2010

Current–fed bi-directional dc/dc converter





Forward mode: Boost converter with hard switching

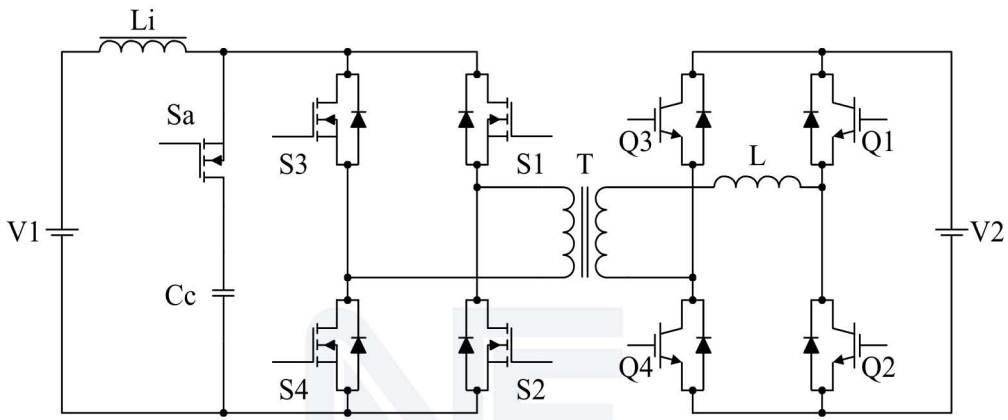
$$M = \frac{V_2}{V_1} = \frac{1}{2N(1-D)} \qquad D > 0.5$$

Backward mode: full bridge buck converter

- Few components
- Transformer with Low leakage is required
- Hard switching

@Pittini Riccardo, Zhang, Zhe, Andersen, Michael A. E. Proceedings of EPE '13

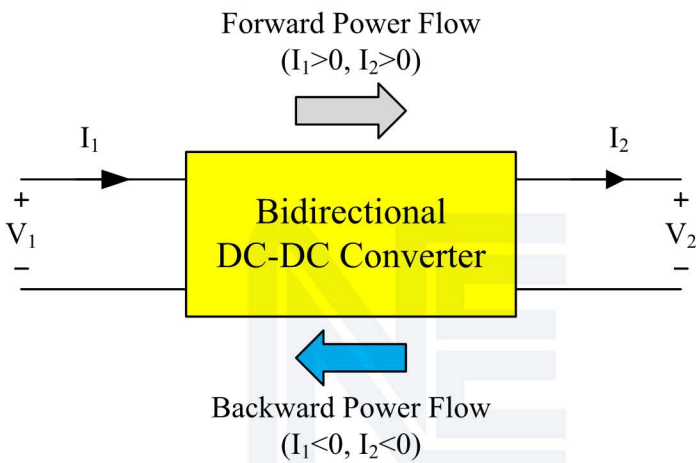
Current–fed bi-dc/dc converter w/ active clamping



- Current-fed for the lower voltage side while voltage fed for high voltage side
- Buck mode using phase-shift control
- Boost mode using primary side duty cycle control
- Soft switching obtained

@K. Wang, F. Lee, and J. Lai, IEEE APEC2000

Requirement to bidirectional DC/DC converters



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Ideal isolated bi-DC/DC converter

- High power conversion efficiency
- Wide voltage gain range(M=V2/V1)
- High frequency and high power density
- Good static and dynamics proformance

Summary

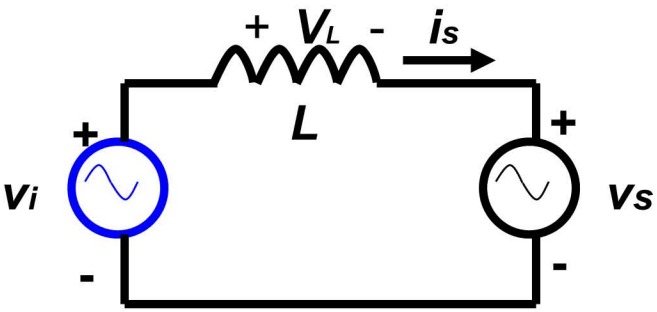
- Operates at both the first quadrant and the second quadrant in V-I plane
- Classified into isolated and non-isolated bi-dc/dc
- Isolated bi-dc/dc converters are classified into DABs with inductor tank, series resonant tank, and high order resonant tank etc.
- Metrics for bi-dc/dc includes efficiency, voltage gain range, high power density, and dynamics etc.

Chapter 2
Modulation of DAB converter

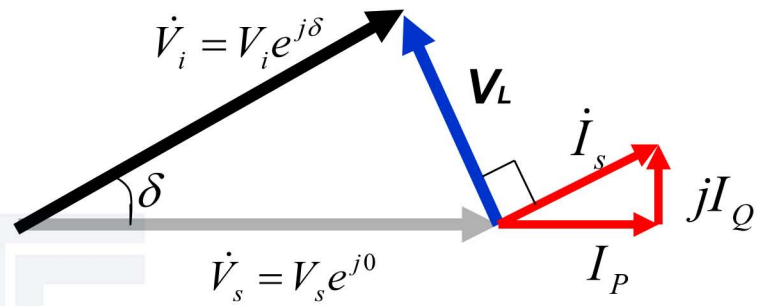
Outline

- Phase shift control
- Trapezoidal modulation
- Summary

Power flow between two sources



$$\dot{V}_s = V_s e^{j0} = V_s \qquad \dot{V}_i = V_i e^{j\delta}$$



L: Inductor between sources

Vi: Voltage source

Vs: Voltage source

Is: Inductor current

$$\dot{I}_s = \frac{\dot{V}_i - \dot{V}_s}{jX} = \frac{V_i e^{j\delta} - V_s}{jX} = \frac{V_i(\cos\delta + j\sin\delta) - V_s}{jX} = \frac{V_i \sin\delta - j(V_i\cos\delta - V_s)}{X}$$

$$\dot{I}_s = I_p + jI_Q = \frac{V_i \sin\delta - j(V_i\cos\delta - V_s)}{X} \qquad X = \omega L, \omega: frequency$$

$$I_P = \frac{V_i \sin\delta}{X} \qquad I_Q = \frac{V_s - V_i\cos\delta}{X}$$

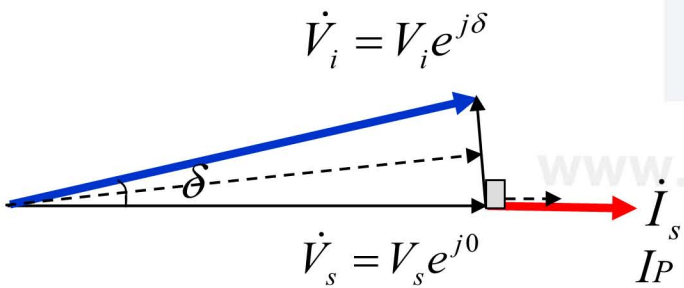
$$P_s = V_s I_P = \frac{V_s V_i \sin\delta}{X} \qquad Q_s = -V_S I_Q = \frac{V_S V_i \cos\delta - V_s^2}{X}$$

Power flow control

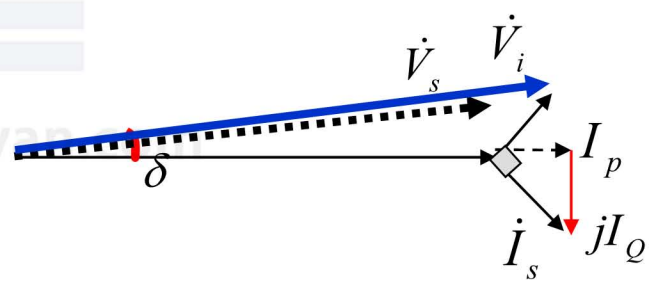
It is assumed that *δ and ΔV=Vi-Vs* are small, then

$$P_s = V_s I_P = \frac{V_s V_i \sin\delta}{X} \approx \frac{V_s V_i}{X}\delta$$

$$Q_s = -V_S I_Q = \frac{V_S V_i \cos\delta - V_s^2}{X} \approx \frac{V_s(V_i - V_s)}{X} = \frac{V_s}{X}\Delta V$$



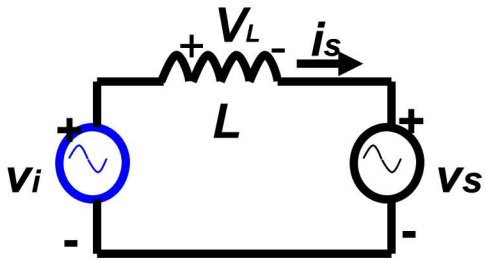
Power is adjusted through *δ*

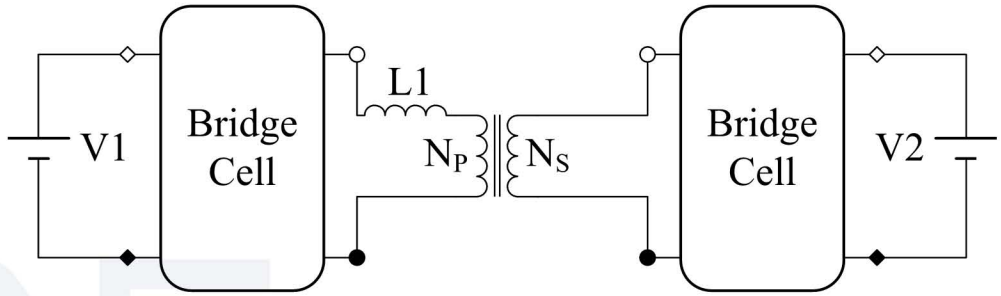


Reactive power is adjusted through *ΔV*

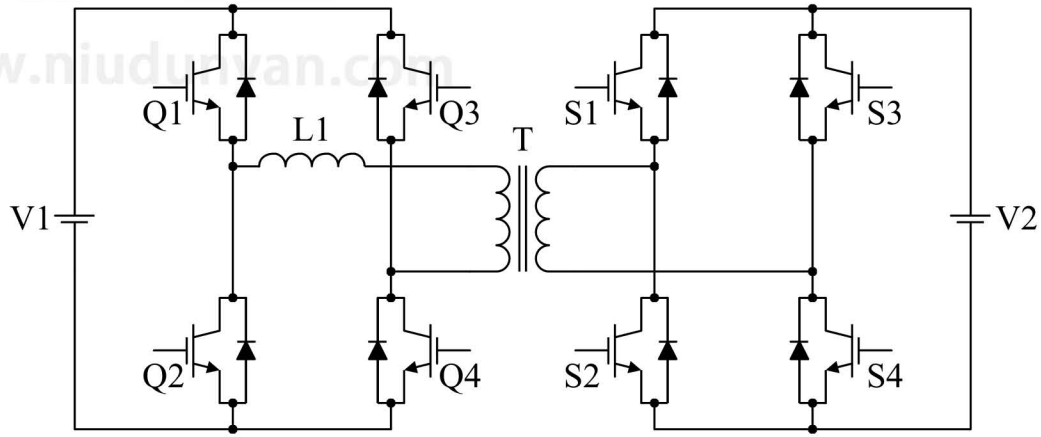
- Power flow is adjustable through phase-shift control
- Amplitude difference between two voltage sources will cause reactive power circulation

Dual active bridge (DAB) converter



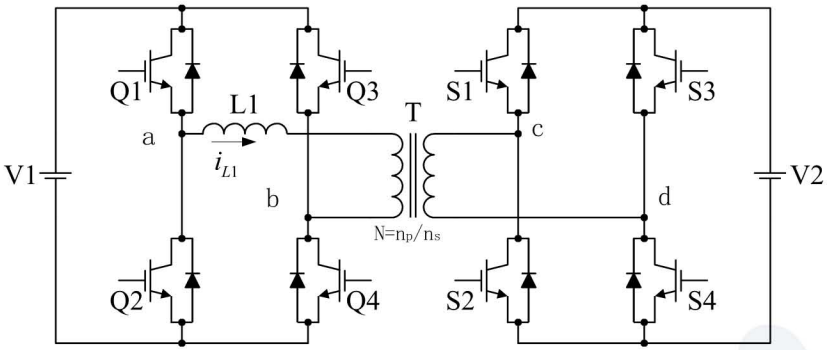


- Converters to emulate the two sources
- Each converter to generate a square wave



*Rik De Doncker, Deepak Divan, Mustansir **H.** Kheraluwala, Trans IA, 1991

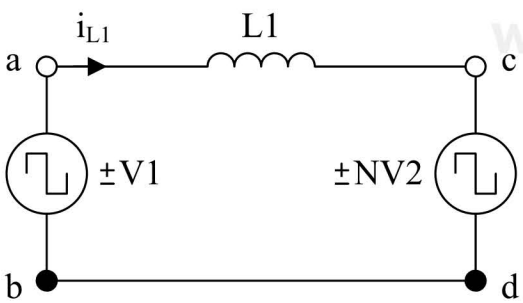
Phase-shift control

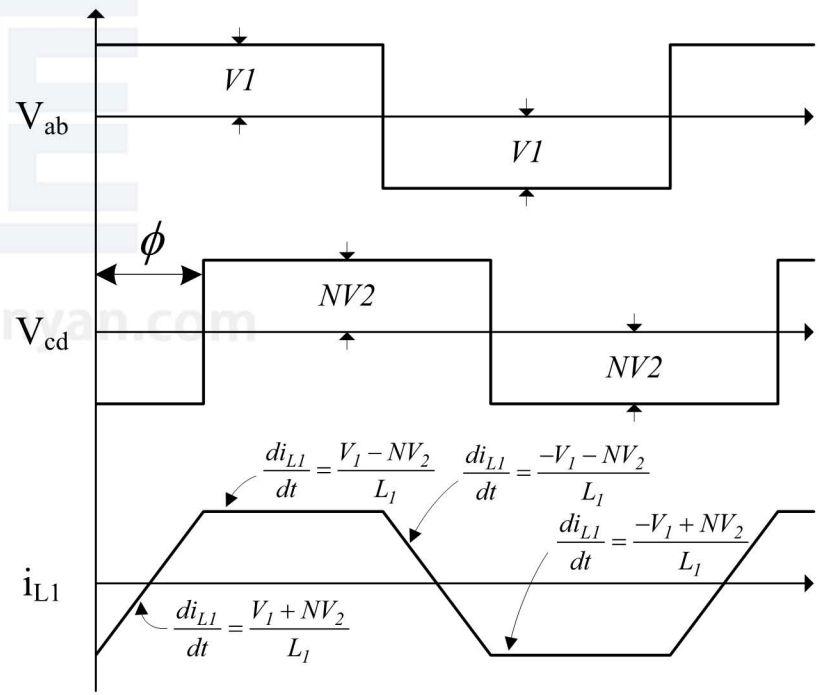


ϕ Phase shift between the primary and secondary

$N = \frac{n_p}{n_s}$ Transformer turn-ratio

- 50% duty cycle for all switches
- Leg a leads lag b by 180 degree
- Leg c leads lag d by 180 degree
- Adjustable phase-shift between Leg a and Leg c



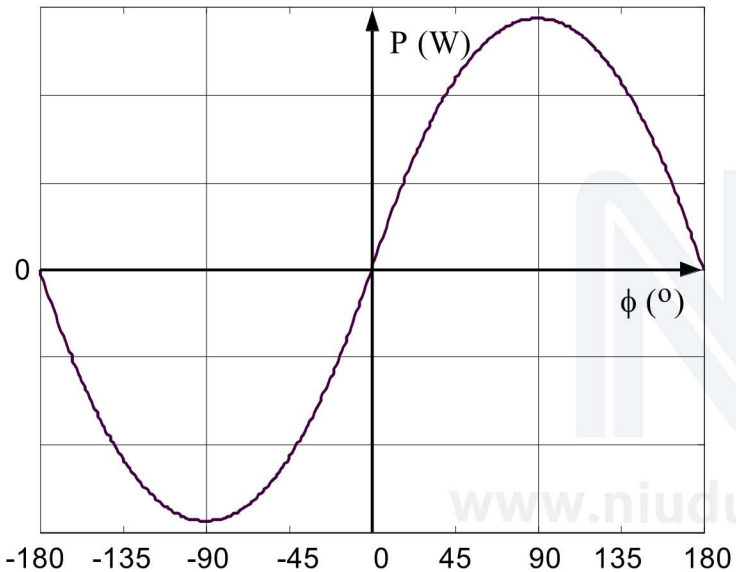


Features

- Buck and Boost functions
- Low voltage stress on the switches
- ZVS turn-on is realized, which is helpful for higher density

Power vs. phase-shift

Average Power $$P = \frac{1}{2\pi}\int_0^{2\pi} V_{ab}(\theta) i_{L1}(\theta) d\theta$$



$$P = \frac{\phi\left(\pi - |\phi|\right) N V_1 V_2 T}{2\pi^2 L_1}$$

ϕ radian

$$P = \frac{\phi\left(180 - |\phi|\right) N V_1 V_2 T}{64800 L_1}$$

ϕ degree

- When phase-shift angle ranges from -90 to 90 degree, power increases with increase of phase shift
- If phase-shift angle is positive, power flow from the primary to the secondary
- If phase-shift angle is negative, power flow from the secondary to the primary

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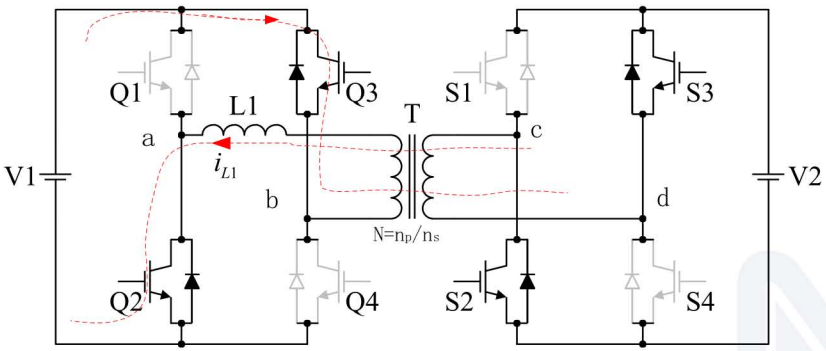
DAB converter with phase-shift control

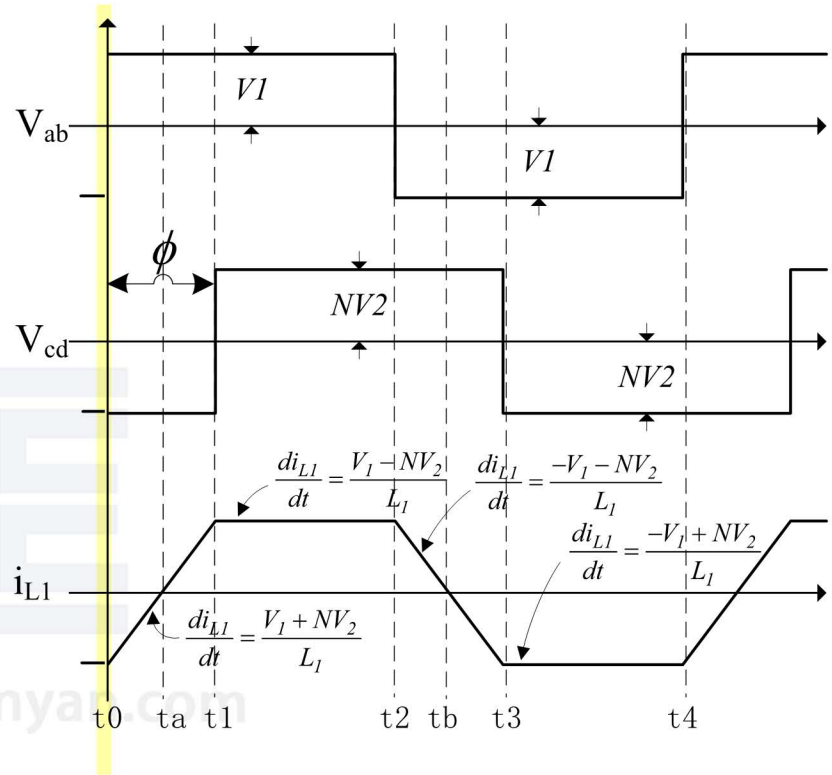
Advantages

- Bidirectional power flow with buck-boost capability
- Simple to control
- Fixed-frequency operation
- Zero voltage switching(ZVS) for all switches
- Incorporation of the parasitic leakage inductances of the transformer as effective power transfer elements

Stage analysis: Initial Stage

T<t0





$$V_{ab} = -V1 \qquad V_{cd} = -V2$$

i_{L1} is negative

- The inductor current flows through the primary side switch Q2 and Q3
- The initial stage ends when at t=t0, Q2 and Q3 are turned off

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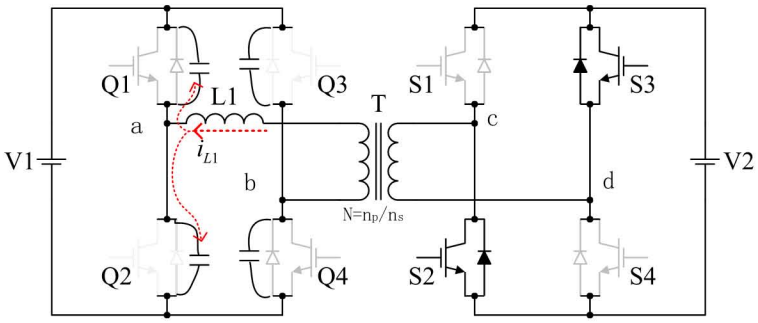
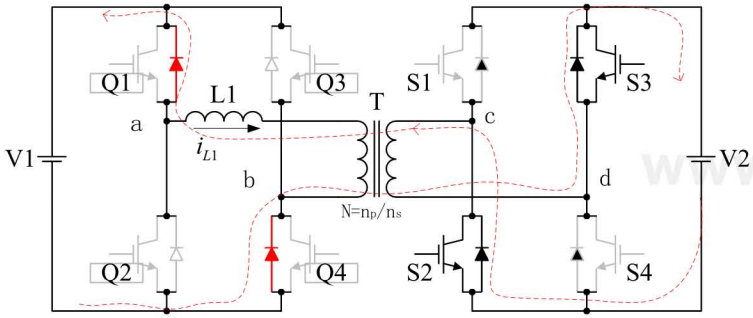
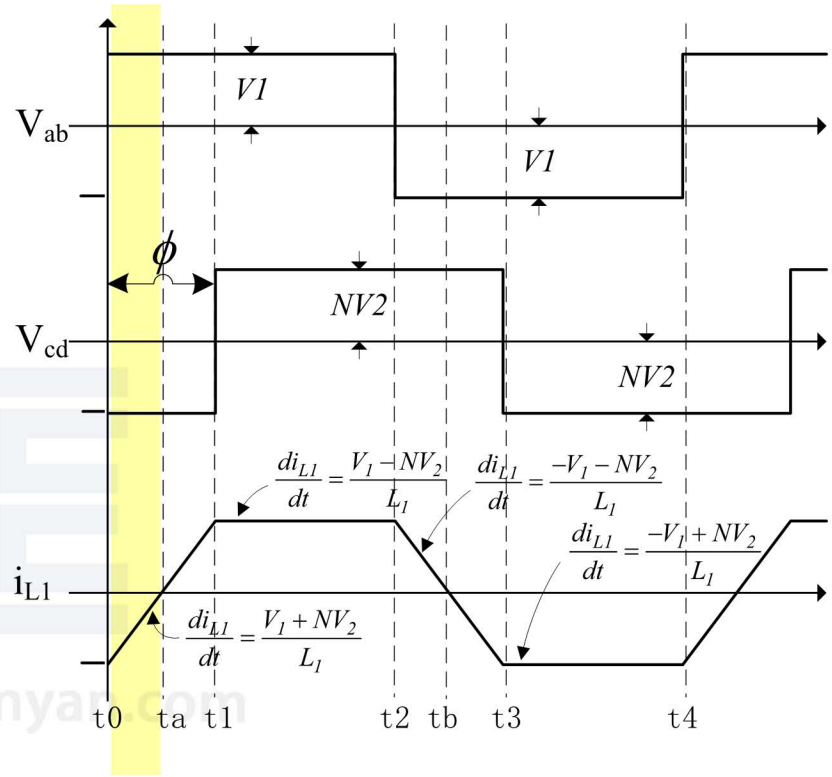
Stage analysis: Stage (t0,ta), Inductor charging

t=t0



t=t0+





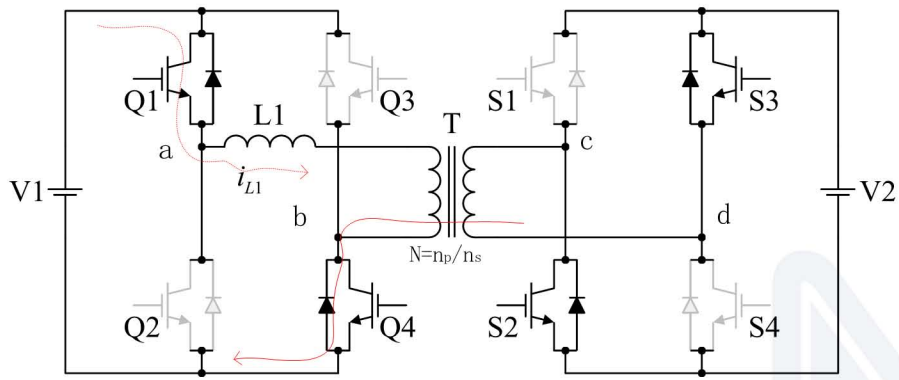
The voltage on Inductor: $v_L = V_1 + NV_2$

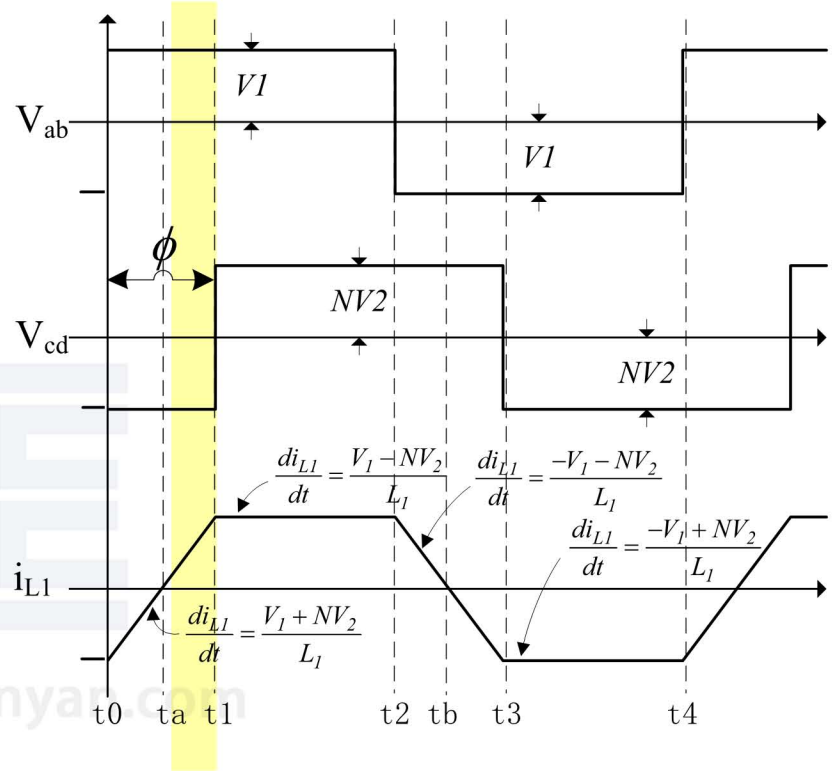
Inductor current linearly increase

- At t=t0, Q2 and Q3 are turned off while negative current iL1(t0) discharge the paralleled capacitors of Q 1 and Q4.
- Once the voltage on Q1 and Q4 capacitors are discharged to zero, the anti-parallel diodes of Q1 and Q4 is turned on. It creates ZVS turn-on condition for Q1 and Q4
- ZVS condition may not satisfy in light load. It also depend on d=NV2/V1

Stage analysis: Stage (ta,t1), Inductor charging

Stage (ta,t1)





- At t=ta, the inductor current changes direction, then Q1 and Q4 turn on with ZVS
- This stage ends when the secondary switch S2 and S3 are turned off

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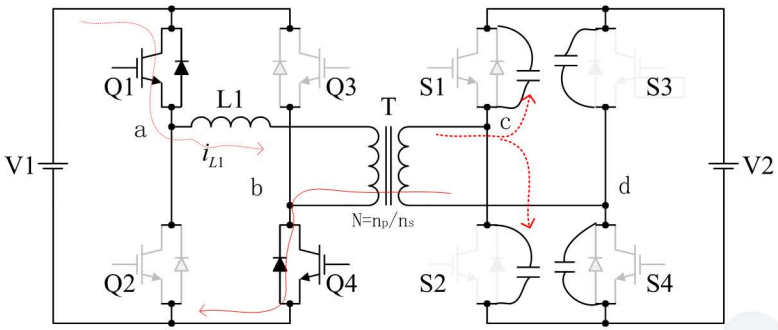
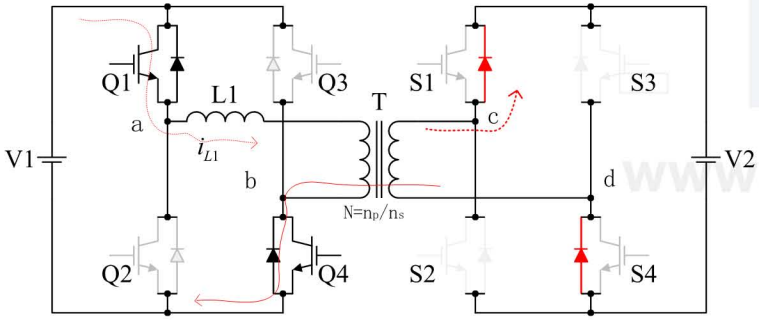
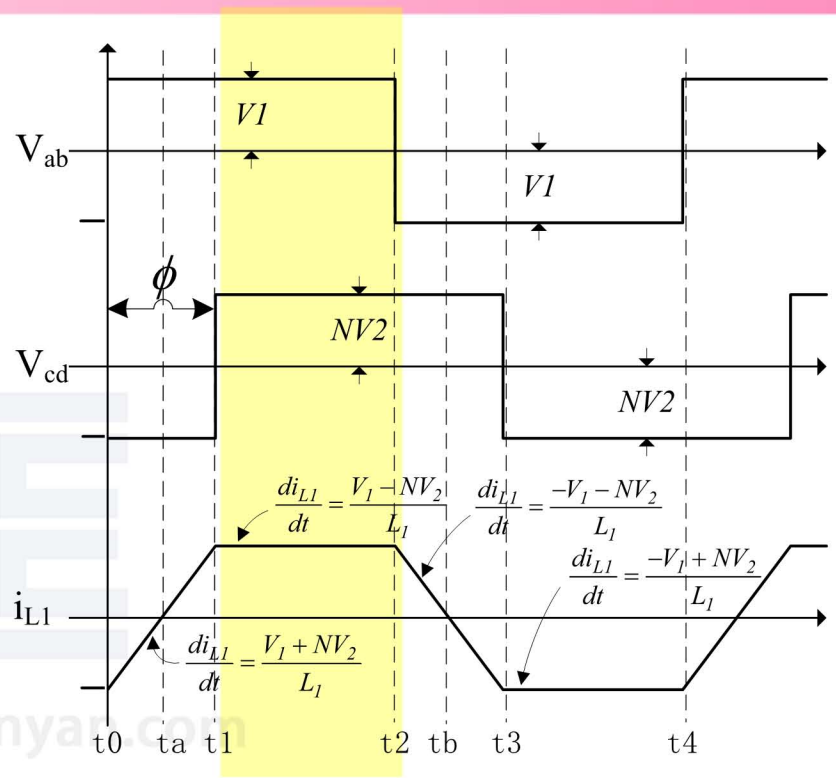
Stage analysis: Stage (t1,t2), Active power transfer

t=t1



t=t1+





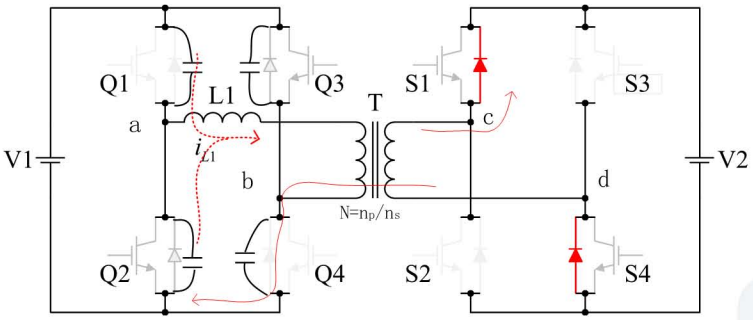
Inductor current change rate $\frac{di_{L1}}{dt}=\frac{V_1-NV_2}{L_1}$

Polarity of the change rate depends on both input and output voltages

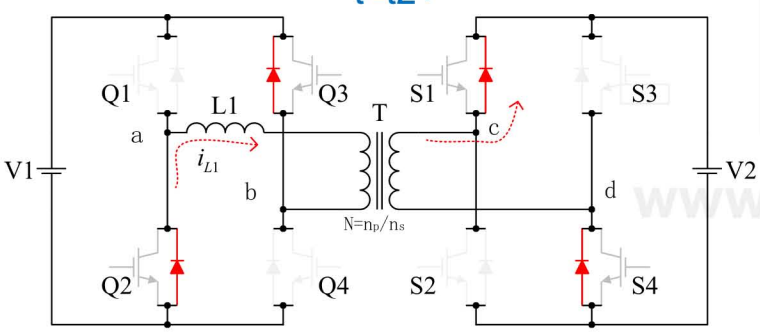
- At t=t1, S2 and S3 are turned off while positive current iL1'(t1) discharge the capacitors of S 1 and S4.
- Once the voltage on S1 and S4 discharged to zero, the anti-parallel diodes of S1 and S4 is turned on. It creates ZVS turn-on condition for S1 and S4
- ZVS turn-on condition for S1 and S4 is easily realized since the inductor just undergoes a charging stage before
- This stage ends when the primary side switch Q1 and Q4 turns off

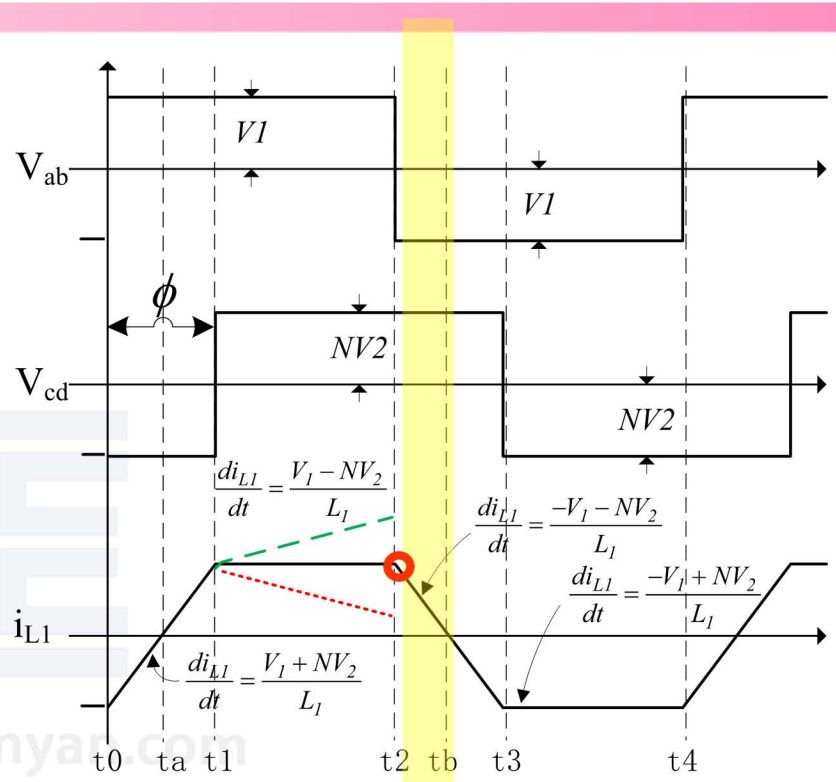
Stage analysis: Stage (t2,tb), Inductor charging

t=t2



t=t2+



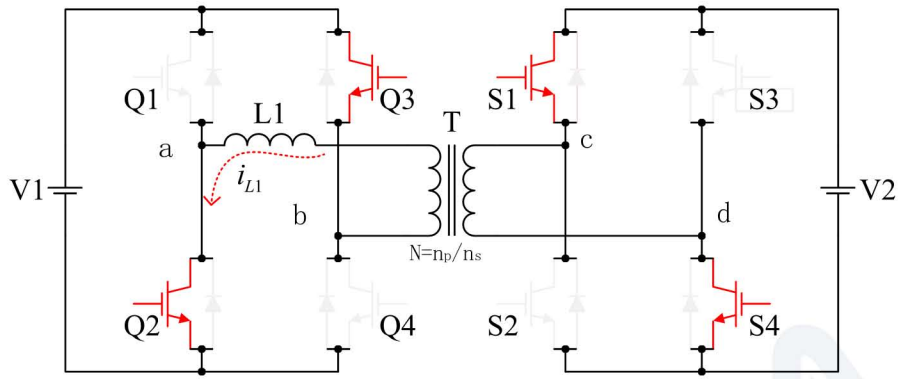


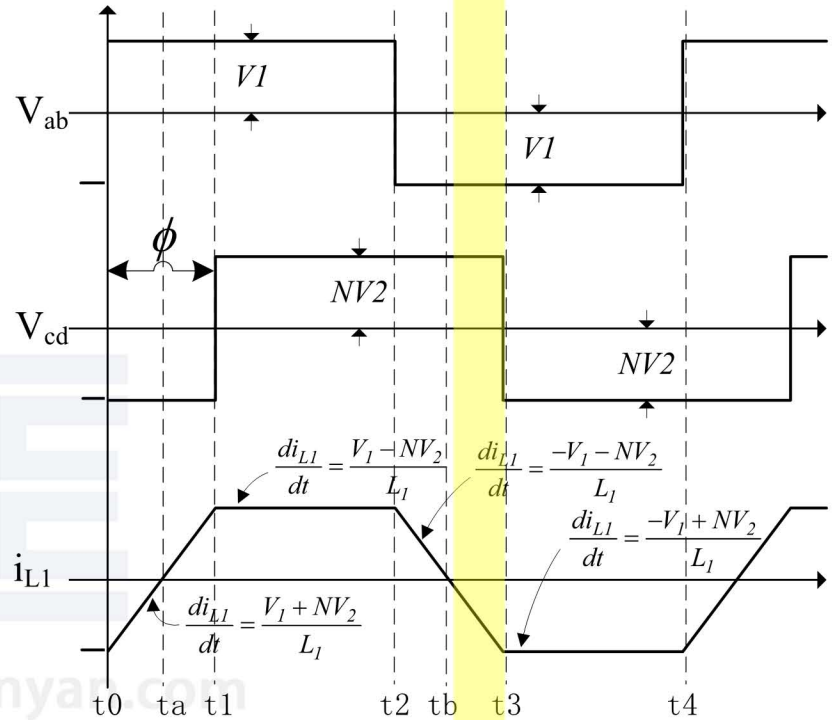
- At t=t2, Q1 and Q4 are turned off while positive current iL1(t2) discharge the capacitors of Q2 and Q3.
- Once the voltage on Q2 and Q3 discharged to zero, the anti-parallel diodes of Q2 and Q3 is turned on. It creates ZVS turn-on condition for Q2 and Q3
- This stage ends when the inductor change direction at tb

ZVS for Q2 and Q3 depend on $i_{L1}(t2)$

It relates to the inductor current change rate of last stage

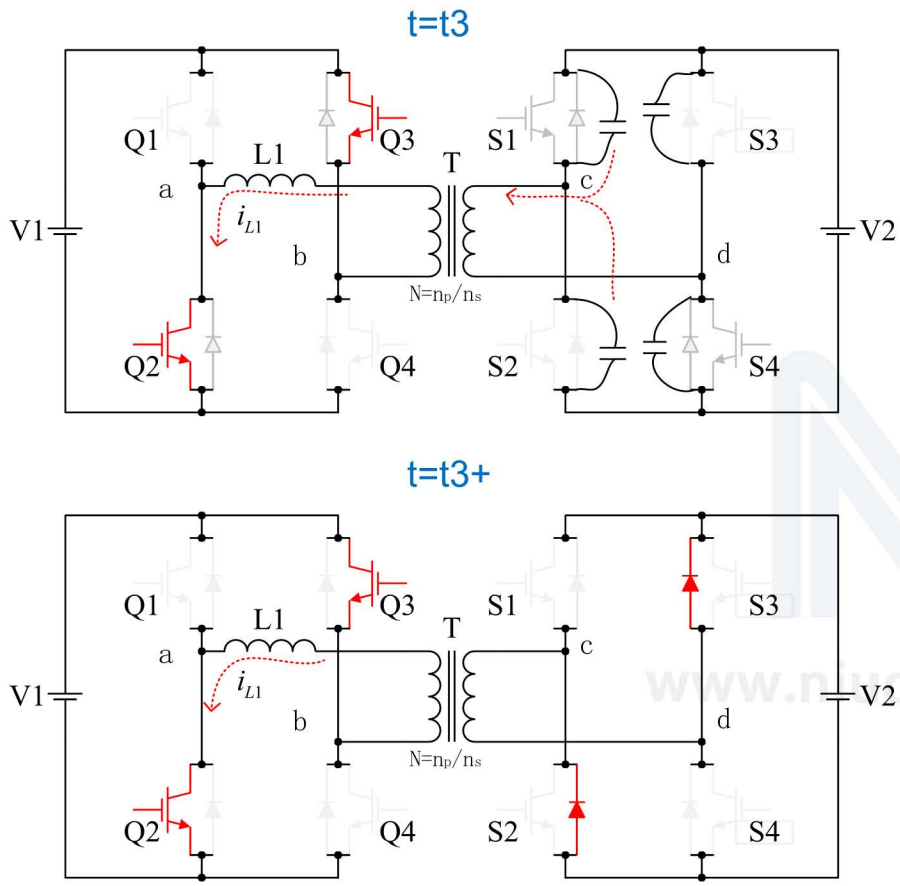
Stage analysis: Stage (tb,t3), Inductor charging

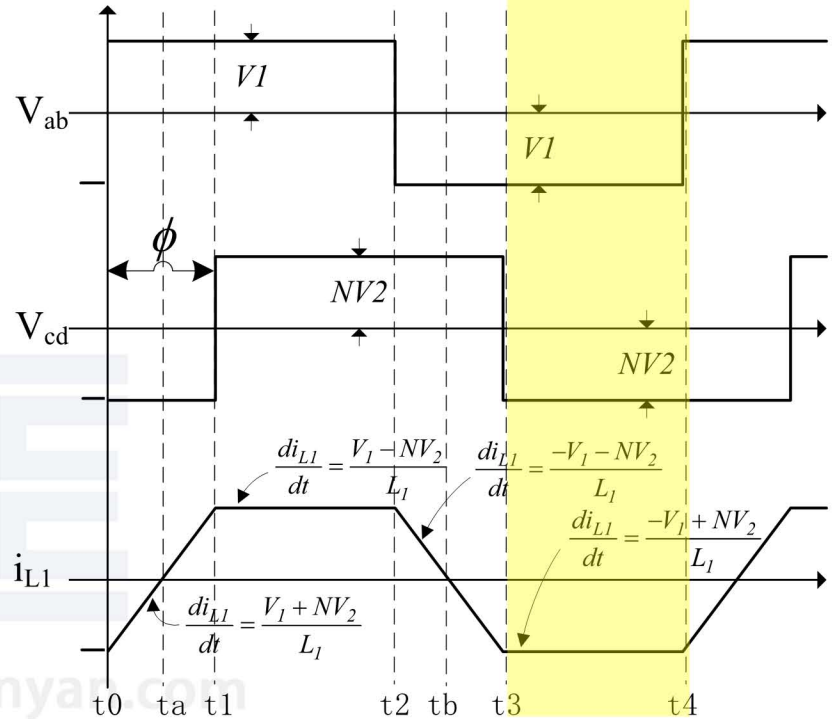




- At t=tb, the inductor change direction, then the primary switch Q2 and Q3 are turned on with ZVS
- The secondary switch S1 and S4 are also turned on with ZVS
- This stage ends when the secondary side switch S1 and S4 turns off

Stage analysis: Stage (t3,t4), Active power transfer

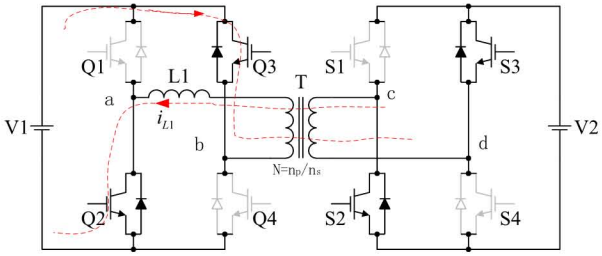




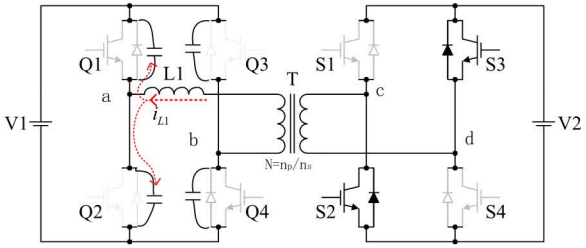
- At t=t3, the secondary side switch S1 and S4 turns off while negative current iL1'(t3) discharges the terminal voltages of S2 and S3
- Once the voltage on S2 and S3 discharged to zero, the anti-parallel diodes of S2 and S3 is turned on. It creates ZVS turn-on condition for S2 and S3
- This stage ends when the primary side switch Q2 and Q3 turns off

ZVS condition for the primary switches

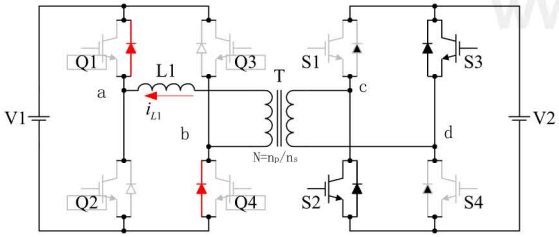
t=t0-

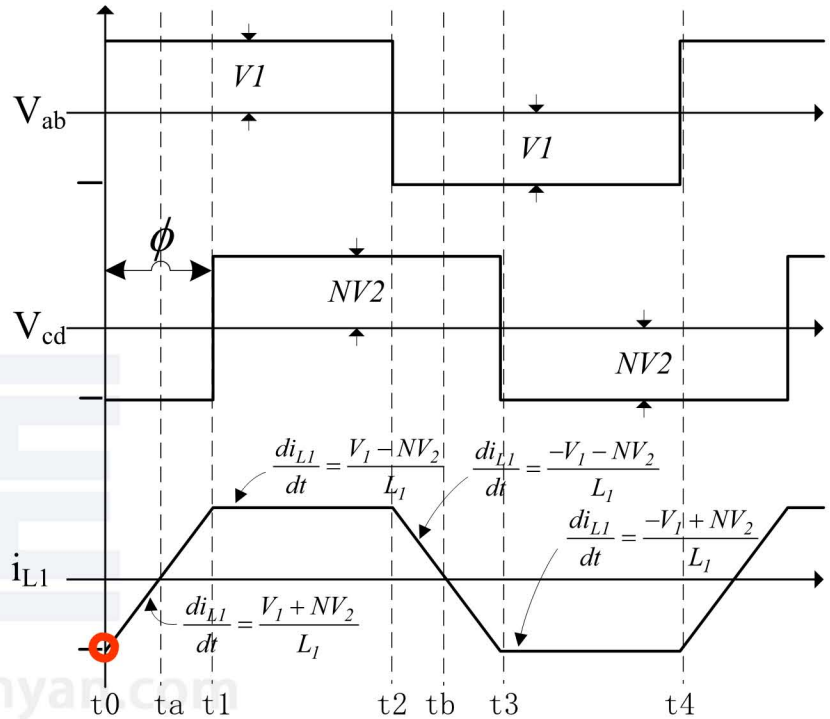


t=t0



t=t0+





ZVS condition for the primary side

- At t=t0, Q2 and Q3 are turned off while negative current iL1(t0) discharge the terminal voltages of Q 1 and Q4.
- Once the voltage on Q1 and Q4 discharged to zero, the anti-parallel diodes of Q1 and Q4 is turned on. It creates ZVS turn-on condition for Q1 and Q4

ZVS condition: $\frac{1}{2}L_1\left[i_{L1}(t_0)\right]^2 > C_p V_1^2$

Cp: paralleled capacitor of the primary switch

Necessary ZVS condition: $i_{L1}(t_0) < 0$

- ZVS condition may not satisfy in light load. It also depend on d=NV2/V1

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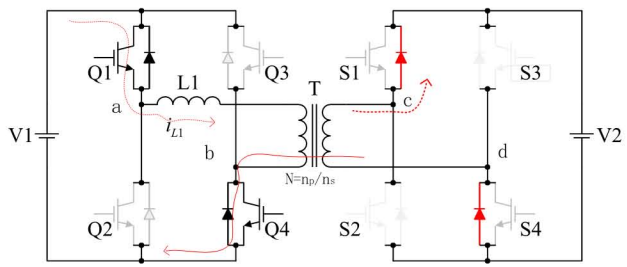
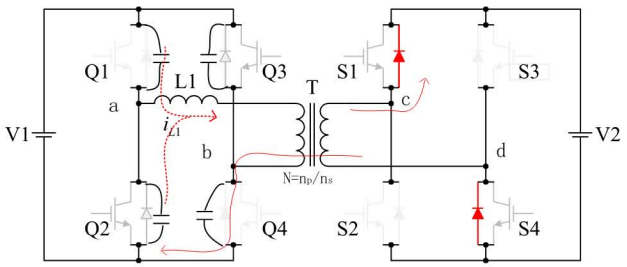
ZVS condition for the primary switches(cont.)

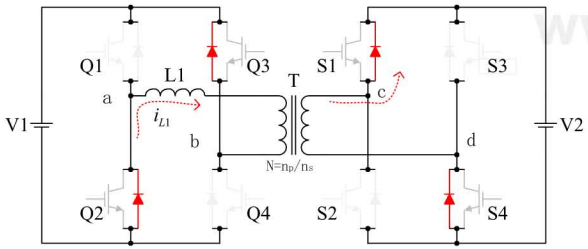
t=t2-

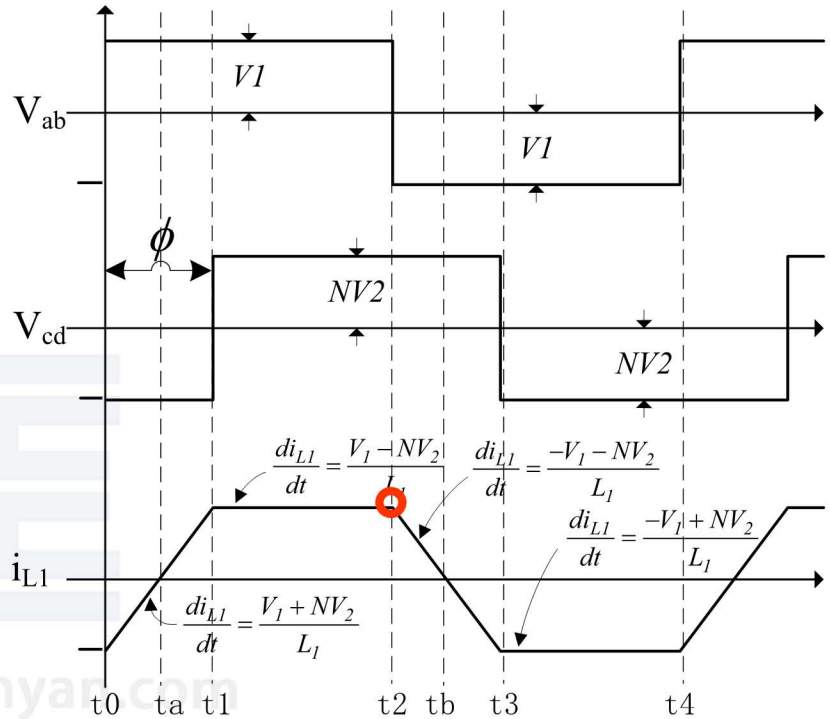


t=t2



t=t2+





ZVS condition: $\frac{1}{2} L_1 \left[i_{L1}(t_2) \right]^2 > C_p V_1^2$

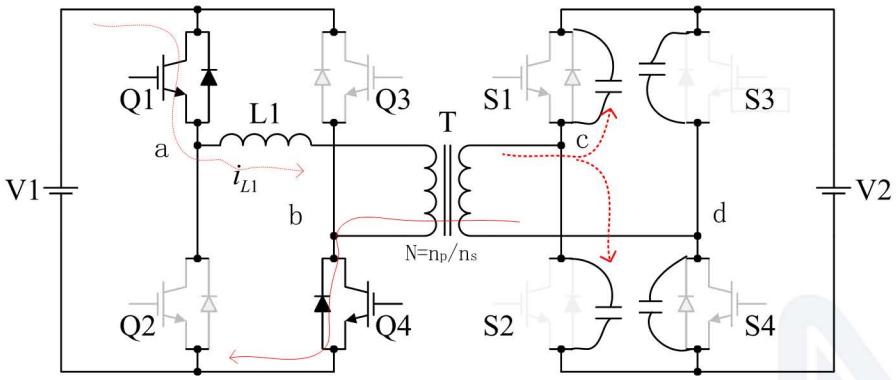
ZVS condition for the primary side

- At t=t2, Q1 and Q4 are turned off while positive current iL1(t2) discharges the terminal voltages of Q 2 and Q3
- Once the voltage on Q2 and Q3 discharged to zero, the anti-parallel diodes of Q2 and Q3 is turned on. It creates ZVS turn-on condition for Q2 and Q3

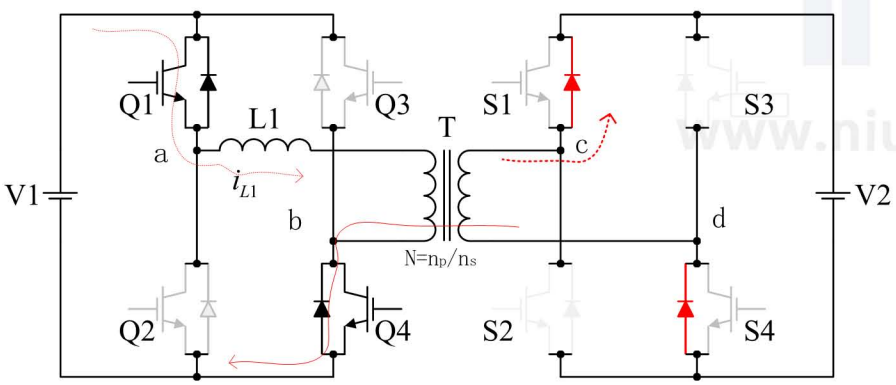
- ZVS condition may not satisfy in light load. It also depend on d=NV2/V1

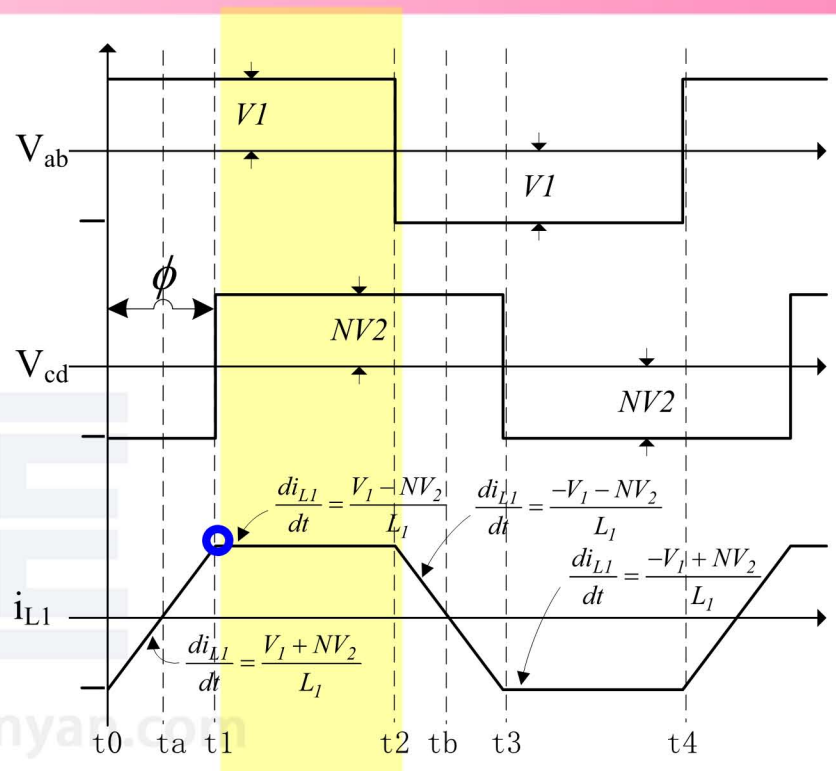
ZVS condition for the secondary switches

t=t1



t=t1+





ZVS condition: $\frac{1}{2} L_1 \left[i_{L1}(t_1) \right]^2 > C_S V_2^{\,2}$

Cs: paralleled capacitor of the secondary switch

Necessary ZVS condition: $i_{L1}(t_1) > 0$

- At t=t1, S2 and S3 are turned off while positive current iL1'(t1) discharge the capacitors of S 1 and S4.
- Once the voltage on S1 and S4 discharged to zero, the anti-parallel diodes of S1 and S4 is turned on. It creates ZVS turn-on condition for S1 and S4
- ZVS is easily realized since the inductor just undergoes a charging stage before

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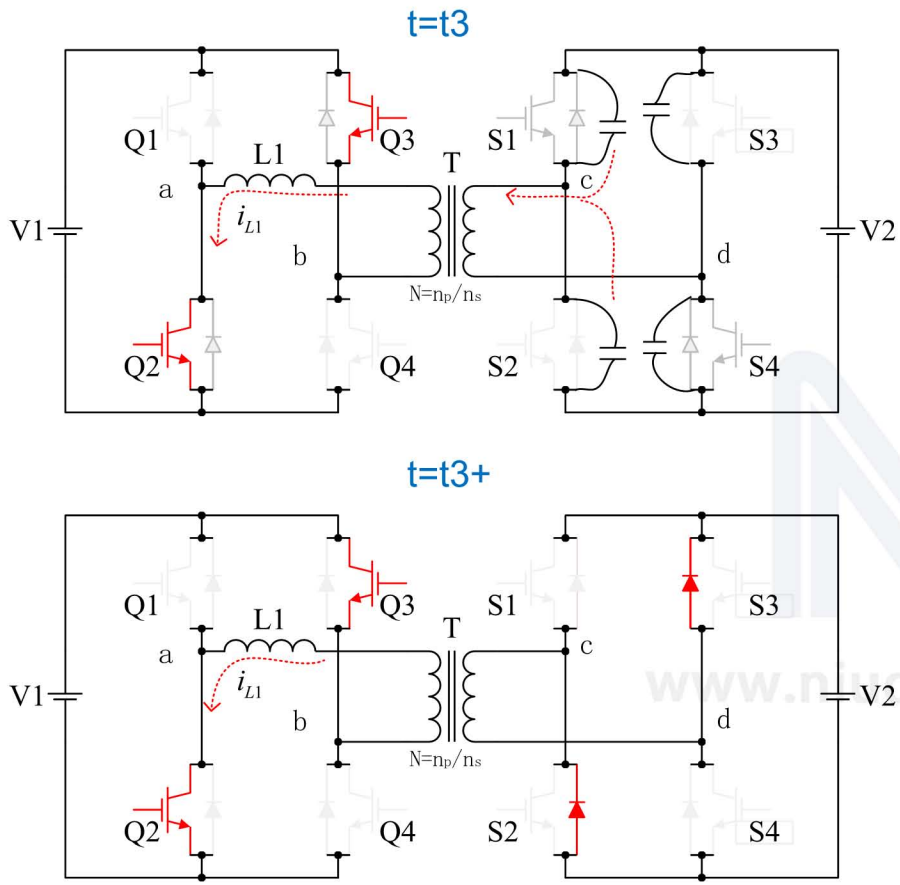
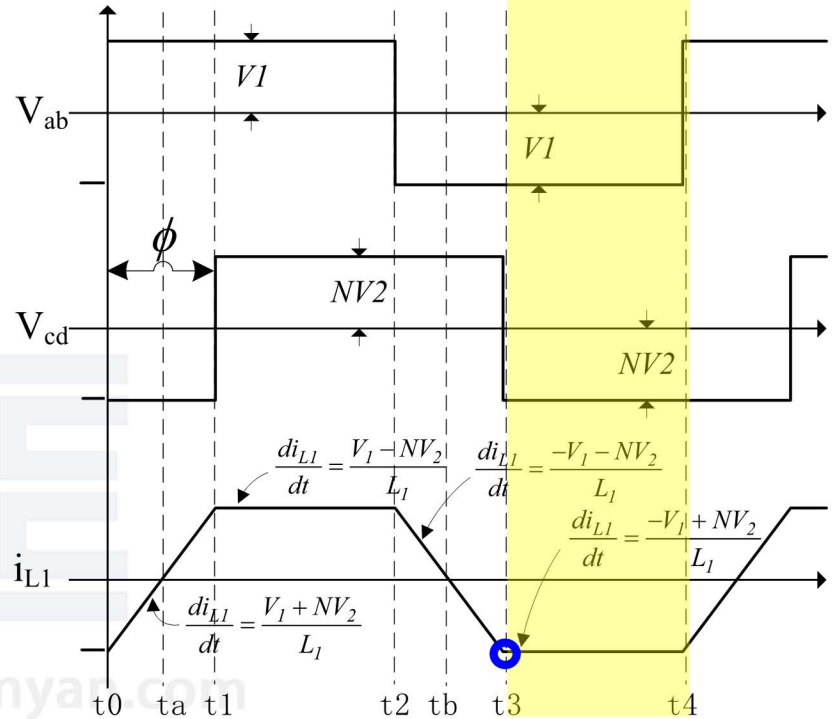
ZVS condition for the secondary switches(Cont.)



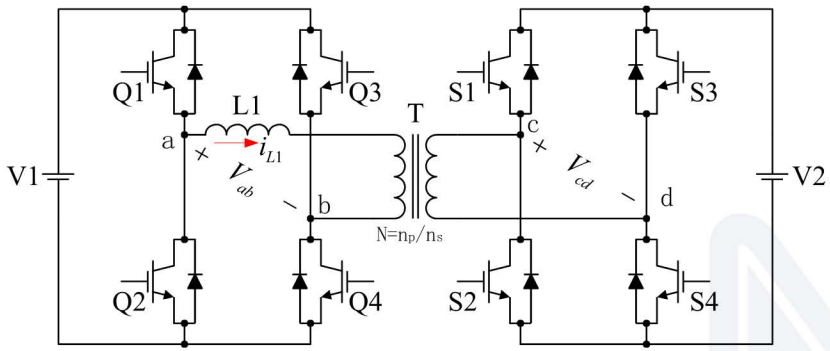


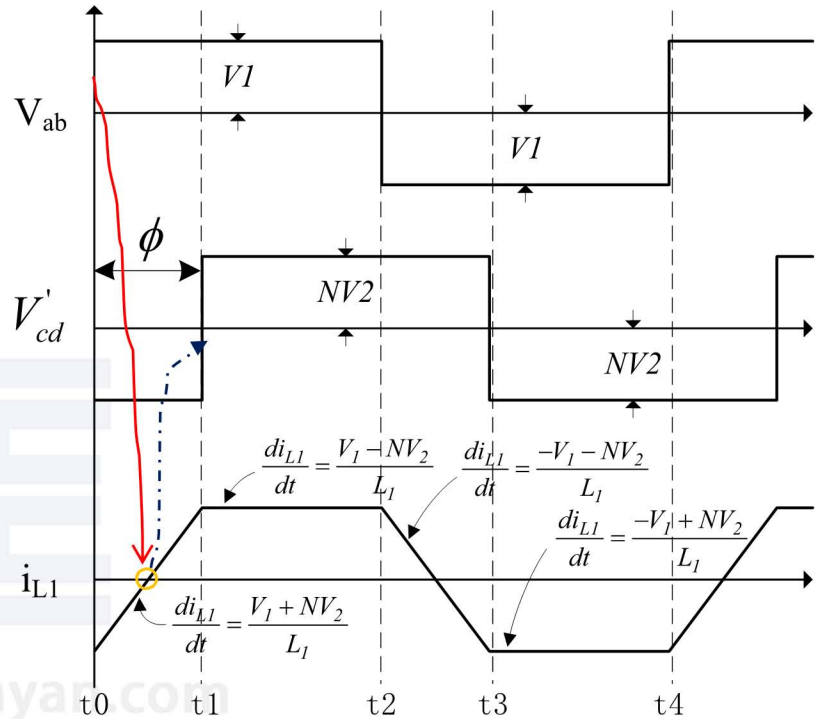
ZVS condition: $\frac{1}{2} L_1 \left[i_{L1}(t_3) \right]^2 > C_S V_2^{\,2}$

- At t=t3, the secondary side switch S1 and S4 turns off while negative current iL1'(t3) discharges the terminal voltages of S2 and S3
- Once the voltage on S2 and S3 discharged to zero, the anti-parallel diodes of S2 and S3 is turned on. It creates ZVS turn-on condition for S2 and S3
- ZVS is easily realized since the inductor just undergoes a charging stage before

ZVS condition at balanced input and output voltage

$$@\, d = \frac{NV_2}{V_1} = 1$$





- Trapezoidal inductor current $-i_{L1}(t_0) = i_{L1}(t_1) = i_{L1}(t_2) = -i_{L1}(t_3) = I_{L1}$
- Vab is leading inductor current, the primary inverter output load is inductive
- Vcd is lagging inductor current, , the secondary inverter output load is inductive
- Larger phase shift, easier to satisfy the ZVS condition

ZVS condition for primary switches:

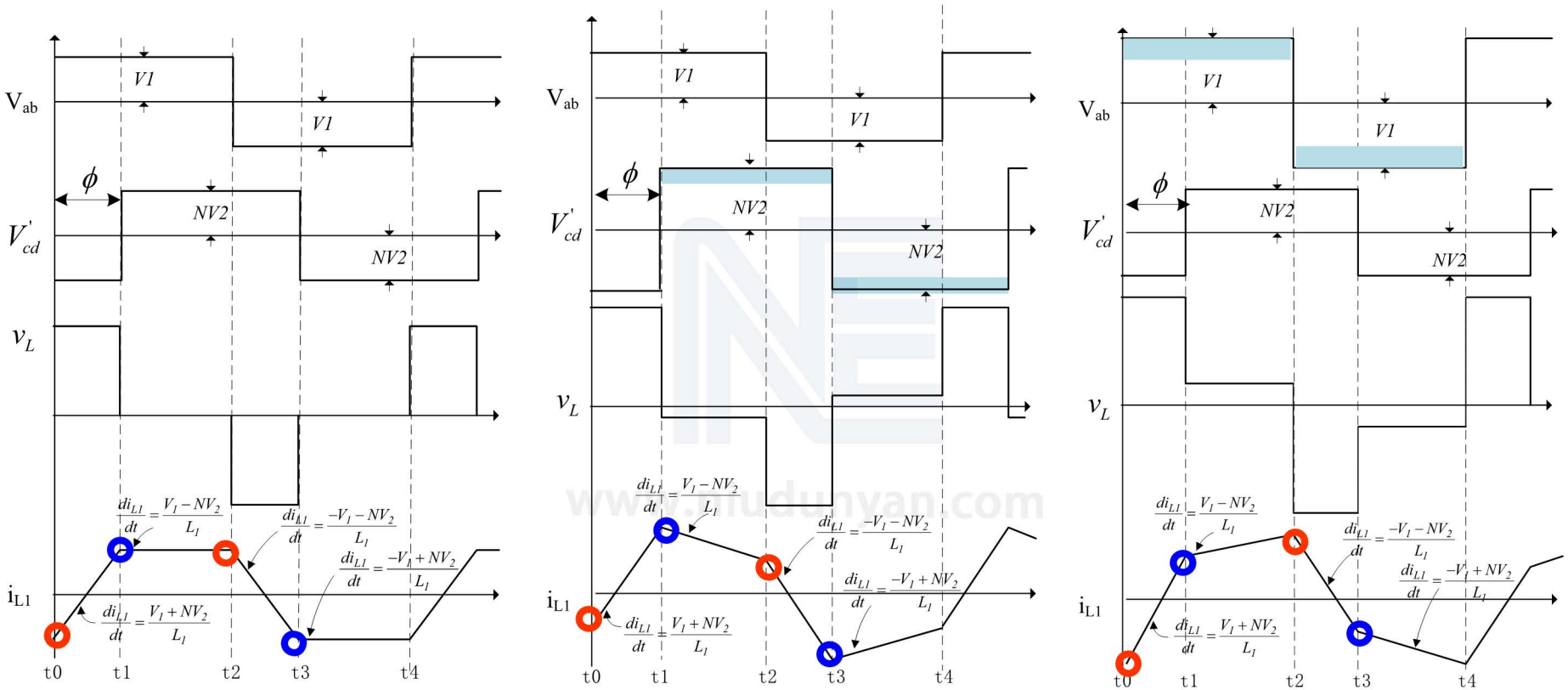
$$\frac{1}{2} L_1 I_{L1}^{\ 2} > C_p V_1^2$$

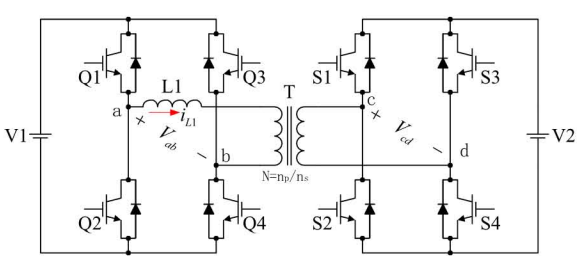
ZVS condition for secondary swithches:

$$\frac{1}{2} L_1 I_{L1}^{\ 2} > C_S V_2^{\ 2}$$

Effect of unbalanced input and output @phase angle>0

d=NV2/V1=1 ***d=NV2/V1>1*** ***d=NV2/V1<1***





- when d>1, primary switches ZVS condition become difficult while the secondary switch ZVS condition is easy to realize
- when d<1, primary switch ZVS condition become easy to realize while the secondary switch ZVS condition become difficult
- when d is not equal to 1, inductor current changes from trapezoidal to triangle alike waveform

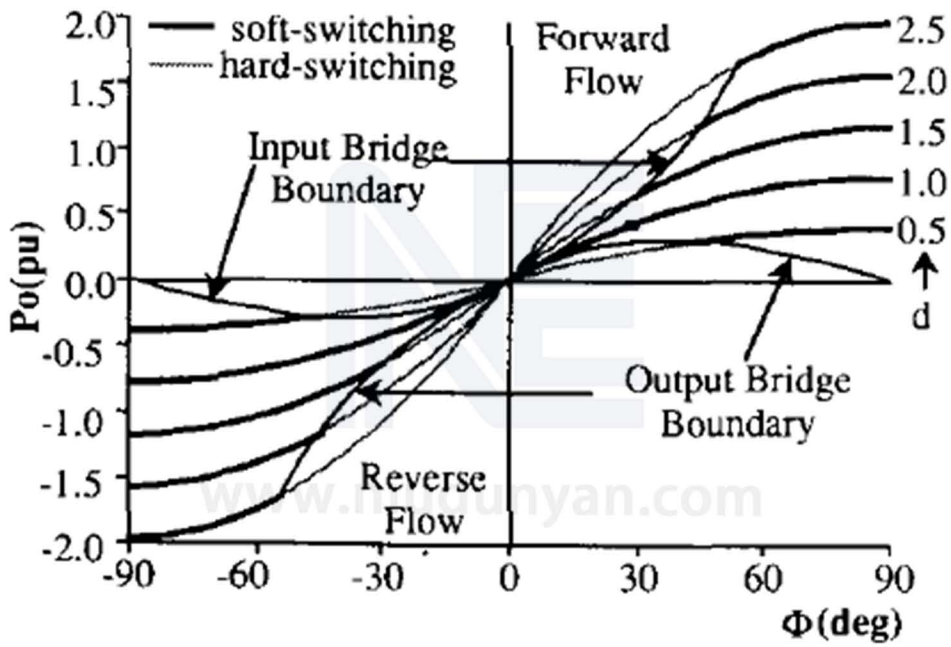
ZVS region

$$P_o = \frac{V_1^2}{X_L} d\phi[1 - \frac{|\phi|}{\pi})$$

$$X_L = \omega L_1$$

$$d = \frac{NV_2}{V_1}$$

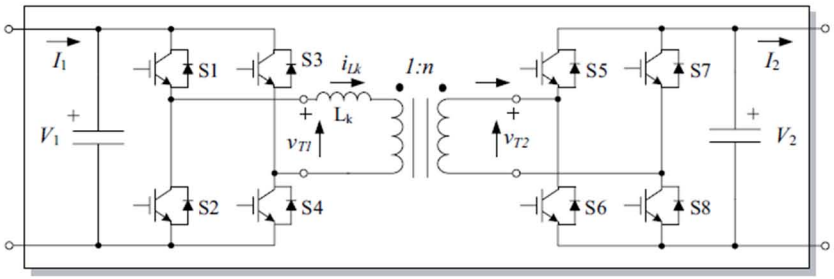
Assumption:
Magnetizing inductance is infinite
Device capacitance negligible



- Full control range under soft switching is achievable for d = 1
- For buck (d < 1) or boost (d > 1) operation, ZVS range is reduced
- Smaller magnetizing inductance will broaden the ZVS region while larger Device capacitance reduces the ZVS region

@M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, etal, IEEE Trans. IA.1992.

Trapezoidal modulation



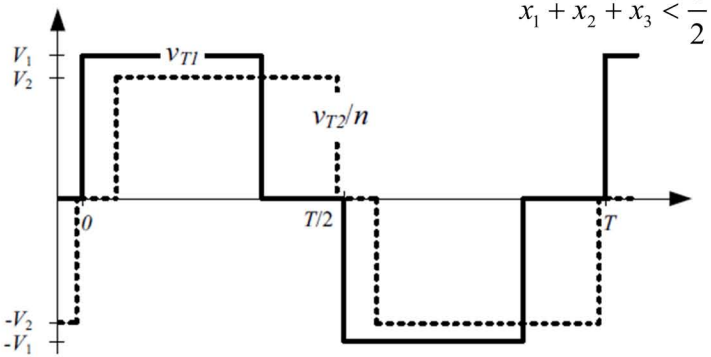
- More freedom to control of the inductor current profile compared with the phase-shift modulation
- Reduction of the circulation current

Average input $\bar{I}_1 = x_1 I_L + x_2 (I_L + I_H)$

Average output $\bar{I}_2 = \frac{V_1}{V_2}\bar{I}_1 = \frac{V_1}{V_2}[x_1 I_L + x_2(I_L + I_H)]$

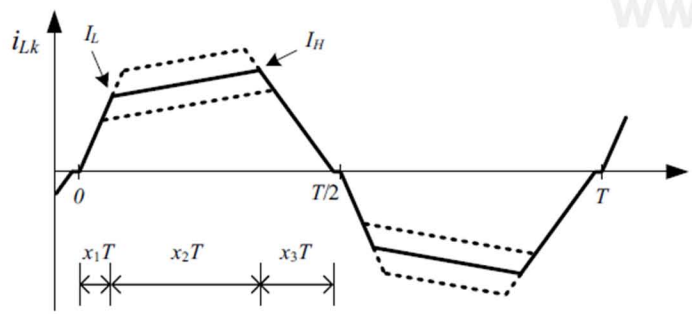
$$\bar{I}_2 = \frac{1}{n}[x_2(I_L + I_H) + x_3 I_H]$$

$$x_1 + x_2 + x_3 < \frac{1}{2}$$

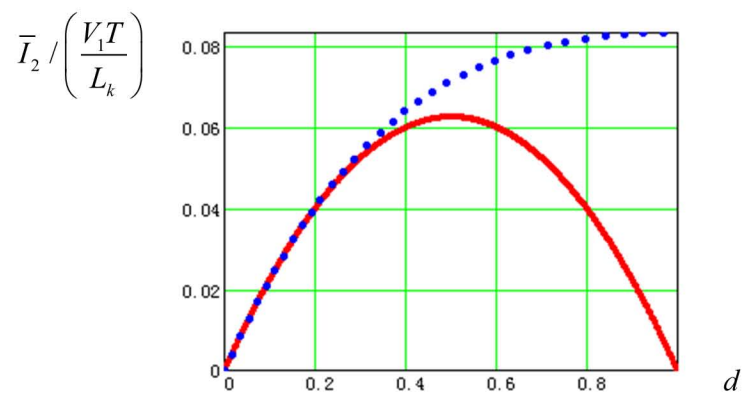


$$x_1 = \frac{I_L L_k}{V_1 T}, \quad x_2 = \frac{(I_H - I_L)L_k}{(V_1 - V_2/n)T}, \quad x_3 = \frac{I_H L_k}{T V_2/n}$$

$$x_3 = \frac{1}{2} - x_1 - x_2 \quad \Rightarrow \quad \frac{1}{4}M(1-M) < \frac{\bar{I}_2}{I^*} \le \frac{1}{4}\frac{M}{1+M+M^2}$$



where $I^* = \frac{V_1 T}{L_k}$ $\quad d = M = \frac{V_2}{nV_1}$



@F. Krismer, S. Round, J. W. Kolar, *PESC*, Jun. 2006

@Todor Todorcevic, Rick van Kessel, Pavol Bauer, and Jan Abraham Ferreira, IEEE JESPE 2015

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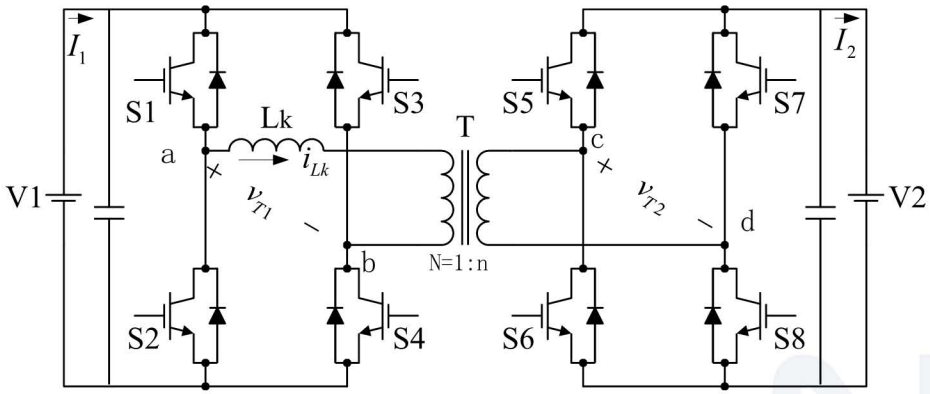
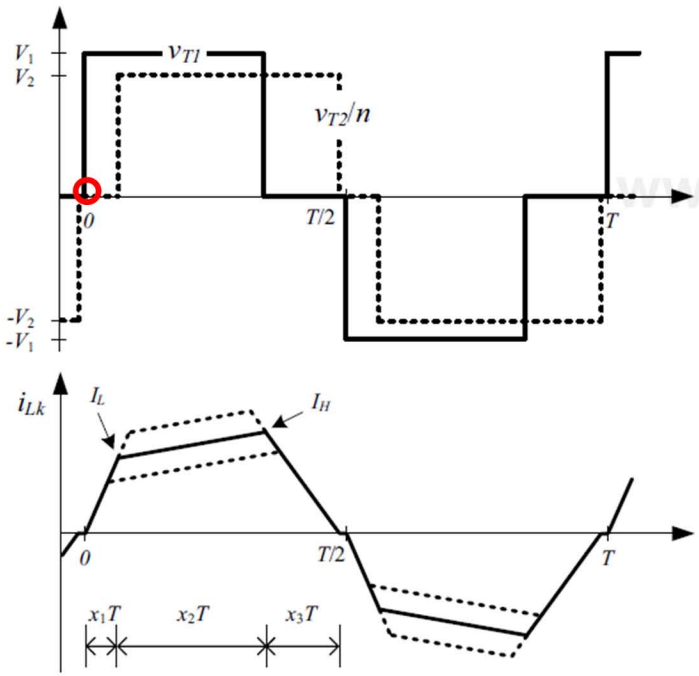
Soft switching analysis for trapezoidal modulation



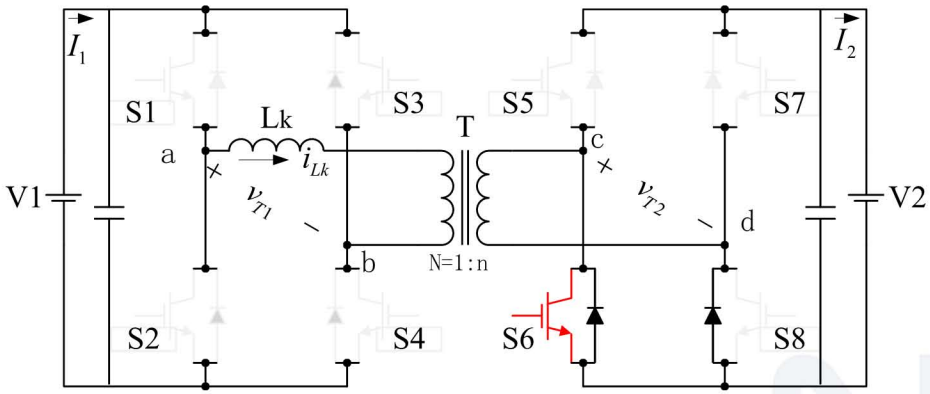
- Switches work on either ZCS or ZVS condition
- ZCS turn-off is more suitable to IGBT devices



Soft switching Status of Switches

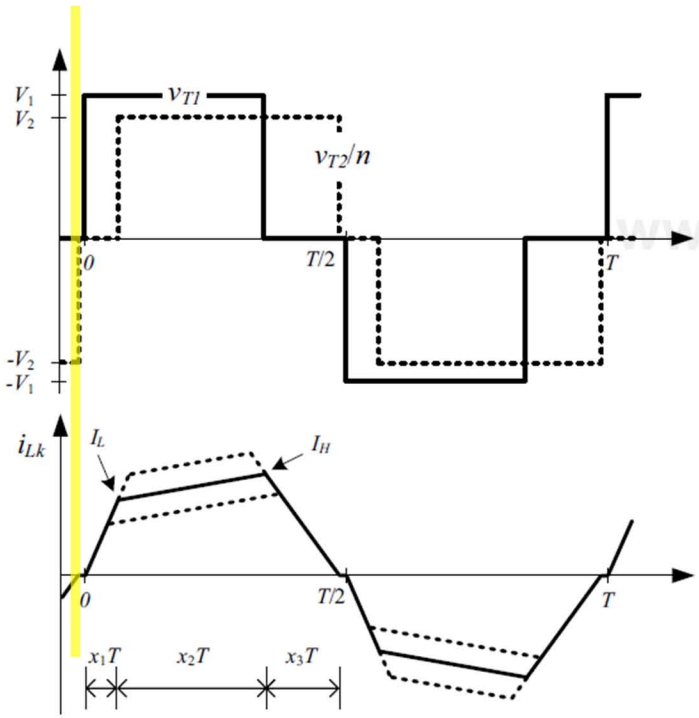
- At t=0-, there is no current flowing in the transformer and all switches
- At t=0, S1 and S4 are turned on with ZCS-on while at the secondary side switch S6 keep conducting form last switching period and anti-parallel diode of S8 turns on with ZCS
- At t=x1T, at the secondary S6 is ZVS turned off while S5 turned on with ZVS due to the inductor current I_L
- At t=(x1+x2)T, S1 ZVS turned off while S2 antiparallel diode is ZVS turned on
- At t=(x1+x2+x3)T, S2 antiparallel diode and S4 are ZCS turned off due to the inductor current decay to zero. At the same time, at the secondary side, S8 antiparallel diode and S5 are ZCS turned off. However gate drive to S5 keep enabled.

Soft switching analysis for trapezoidal modulation



- Initial state

- At t=0-, there is no current flowing in the transformer and all switches



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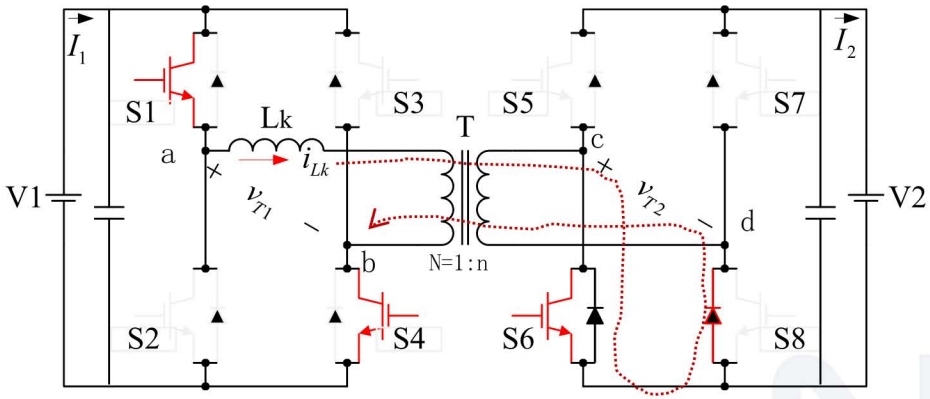
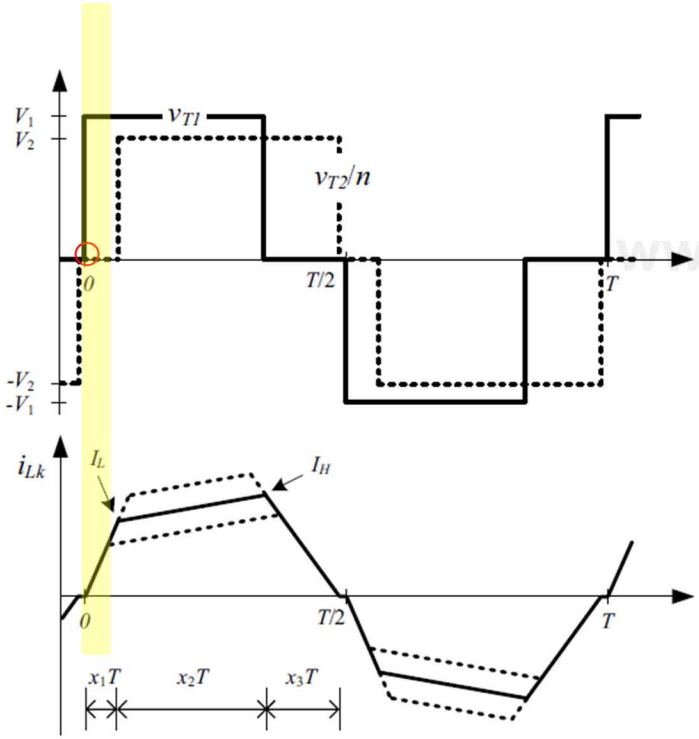
Soft switching analysis for trapezoidal modulation



- Inductor charging stage

Enough inductor current I_L is required to realize ZVS turn-on of S5 in next stage



- At t=0, S1 and S4 are turned on with ZCS-on while at the secondary side switch S6 keep conducting form last switching period and anti-parallel diode of S8 turns on with ZCS.
- At this stage, inductor current linearly increases.

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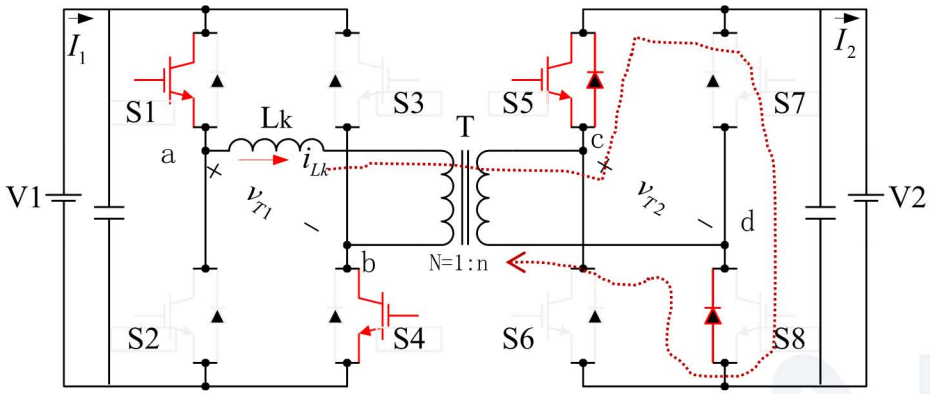
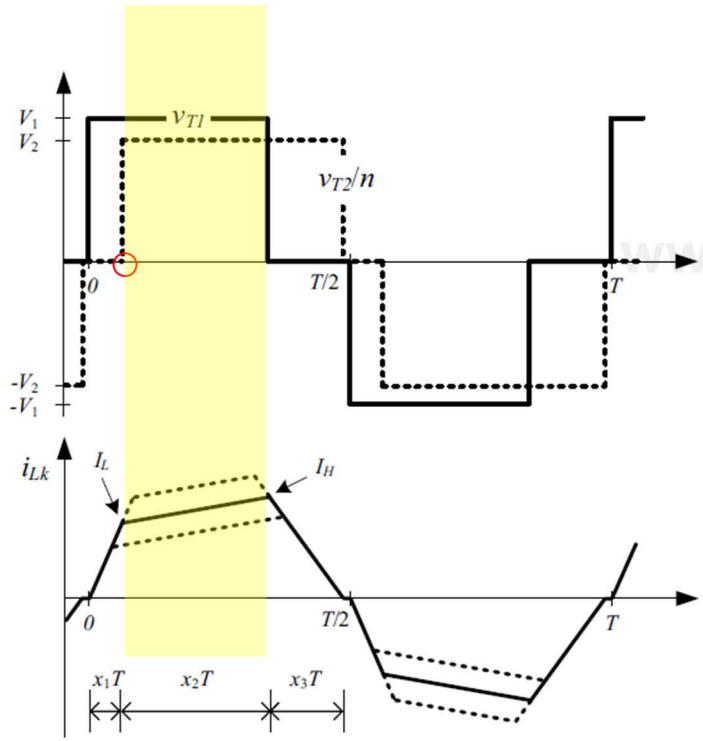
Soft switching analysis for trapezoidal modulation



- Power transfer stage



- At t=x1T, at the secondary S6 is ZVS turned off while S5 turned on with ZVS due to the inductor current I_L
- At this stage, inductor changing rate depends on ***d***

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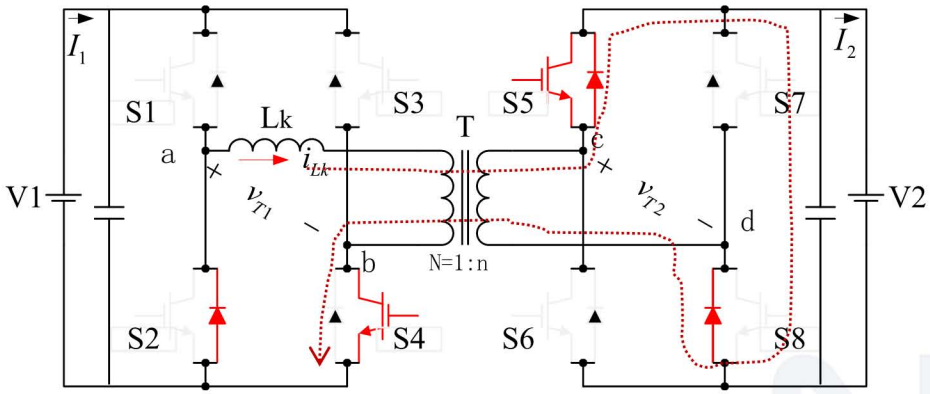
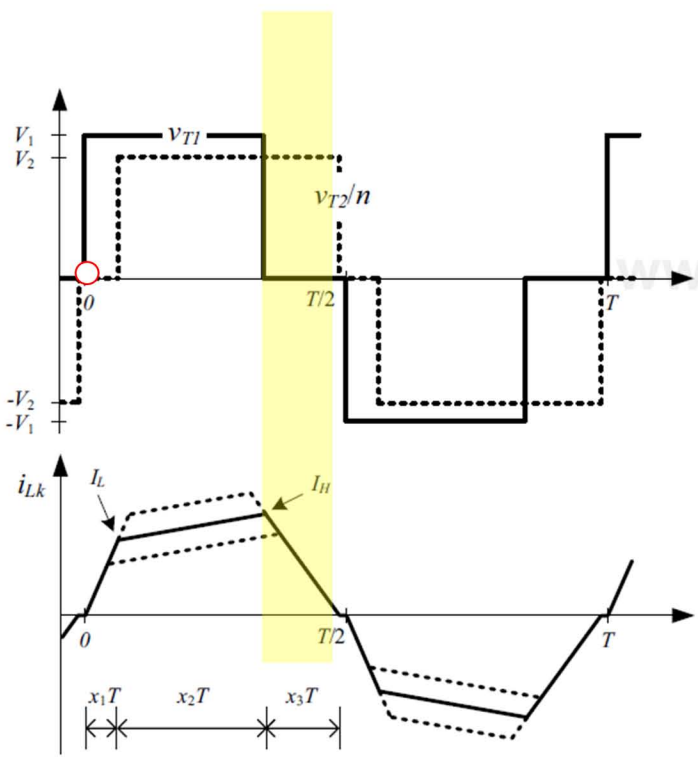
Soft switching analysis for trapezoidal modulation



- Inductor discharging stage

ZVS turn-on of S2 is easily realized due to higher value of I_H



- At t=(x1+x2)T, S1 ZVS turned off while S2 antiparallel diode is ZVS turned on
- At this stage, inductor current decreases

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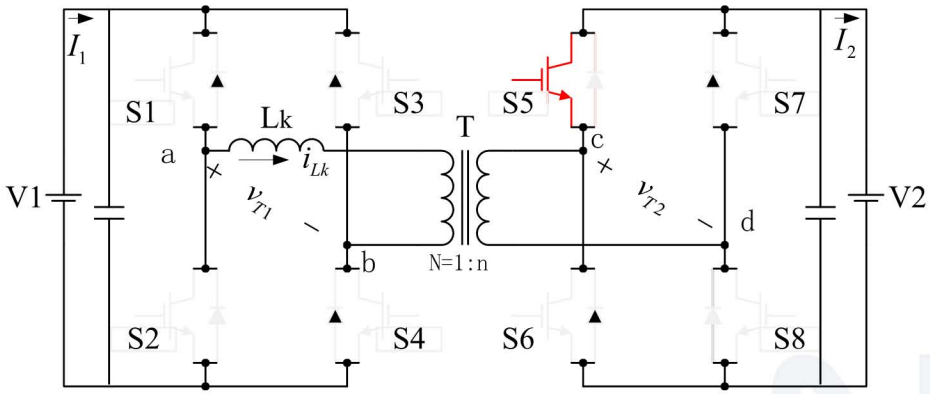
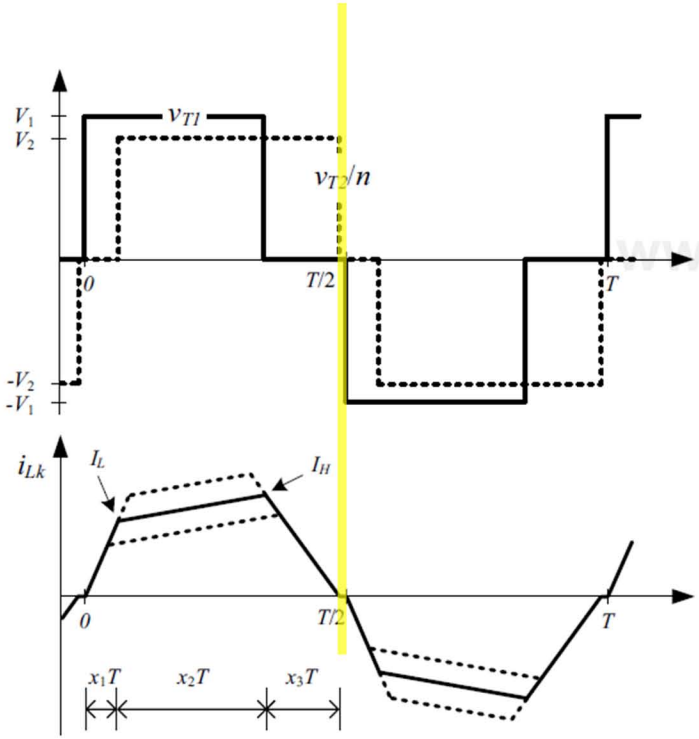
Soft switching analysis for trapezoidal modulation



- Idle stage



- At t=(x1+x2+x3)T, S2 antiparallel diode and S4 are ZCS turned off due to the inductor current decay to zero.
- At the same time, at the secondary side, S8 antiparallel diode is ZCS turned off. However gate drive to S5 keep enabled.

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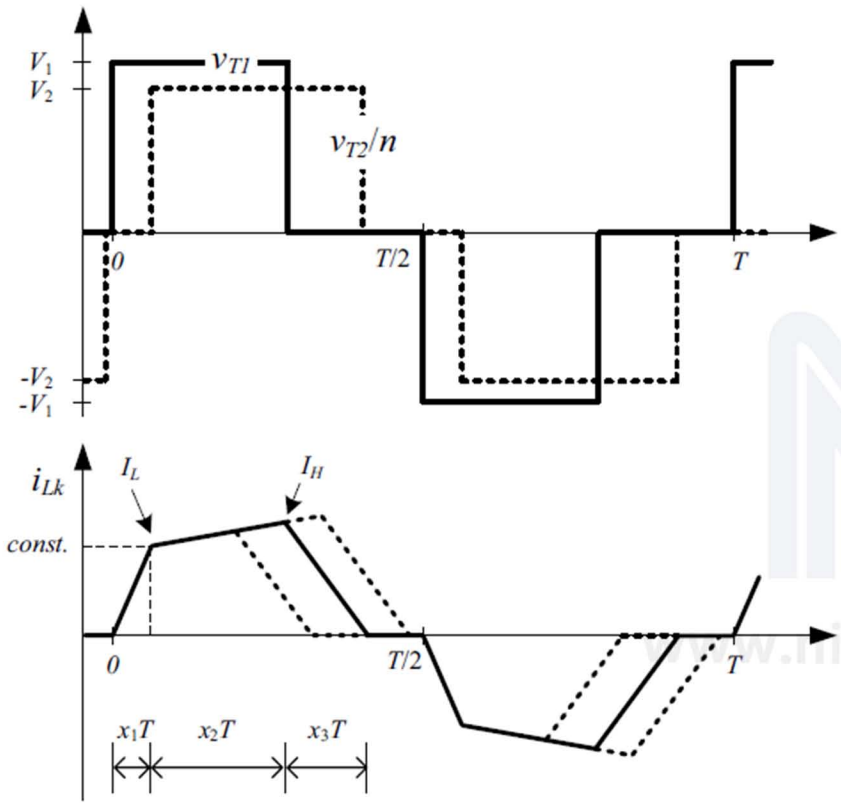
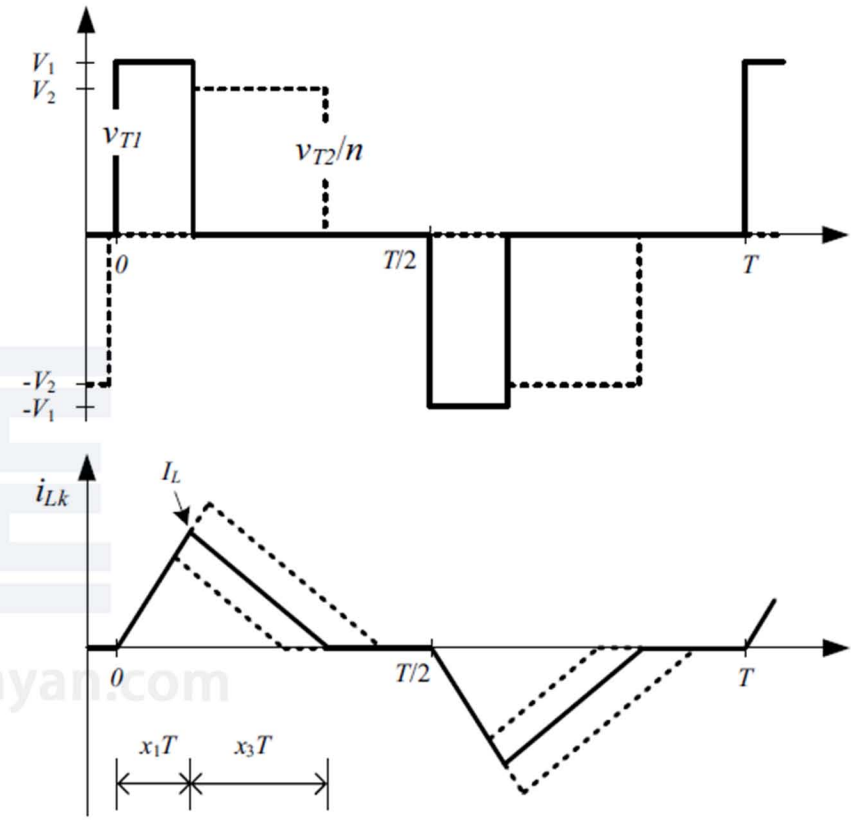
Trapezoidal modulation to cover low output range





- Cover low DAB output current I_2 values
- To preserve the ZVS by maintaining I_L constant

Minimum value $$\overline{I}_2 = \frac{L_k}{TV_2} I_L^{\,2}$$

- Triangular modulation is a special case of the trapezoidal modulation
- Operate as Buck-boost converter
- Less efficient than trapezoidal control mode
- Cover extremely low voltages and current

Summary

Phase-shift control

- Phase shift control is simple to realize
- ZVS turn-on may be realized for all switches
- ZVS soft switching is more suitable to MOSFET
- Significant switch turn-off loss exists due to turn-off of the highest inductor current in a switching period
- Large circulation current loop in the circuit for boost mode including 4 switches and two DC sources
- When d deviates from 1, higher RMS current in the inductor tank and higher loss in the inductor
- When d deviates from 1, higher turn-off switch loss while ZVS condition become difficult to realize

Trapezoidal modulation

- More accurate control of inductor profile, which is not so sensitive to variation of ***d*** as Phase-shifting control. Allow for better control of the inductor current compared with the phase-shift control
- Inductor current is discontinuous
- All switches are soft switching
- Some switches are ZCS turn-off or ZCS turn-on while others are ZVS turn-on or turn-off
- For half period, the primary side:3 ZCS(2 ZCS on, 1 ZCS off), 1 ZVS operation while the secondary side:2 ZVS(1 ZVS-on. 1 ZVS-off), 1 ZCS-off operation. However for phase shift control 8 switch operations(4 tentative ZVS-on, 4 ZVS-off) in a switching period.
- ZCS dominating soft switching is more suitable to IGBT
- Circulation current loop length is reduced in comparison to phase-shift control
- Control is complex

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Chapter 3
Synthesizing Phase-shift Bidirectional DC/DC Converters

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Outline

- Review of phase-shift controlled bidirectional DC-DC
- Switch Cell
- New family of phase-shift bi-directional DC-DC
- Example: build new phase-shift bi-directional DC-DC
- Summary

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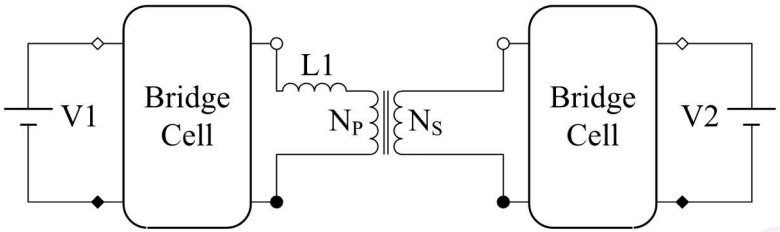
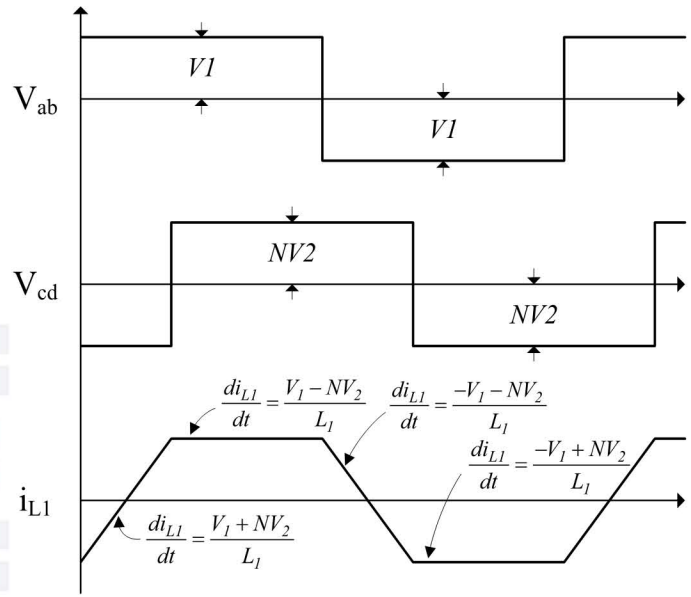
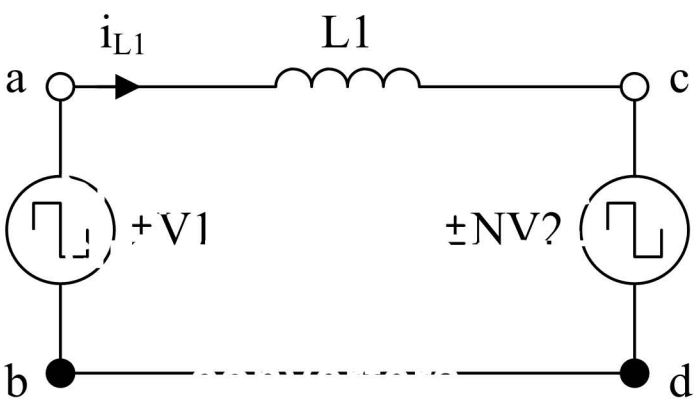
Concept of phase-shift bi-directional DC-DC converter

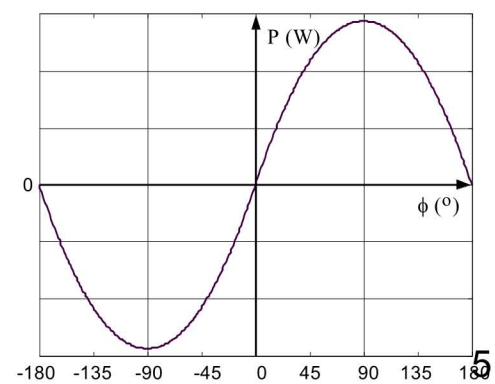




Two square-wave voltage sources on the both ends.

Waveforms of the simplified circuit.





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How do we get square-wave voltage source？

In non-isolated bidirectional DC-DC converter, the voltage waveform across the inductor is square wave when the duty cycle is 50%

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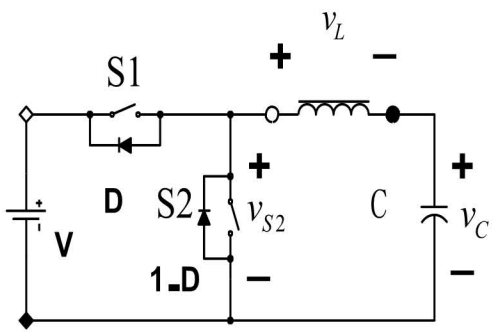
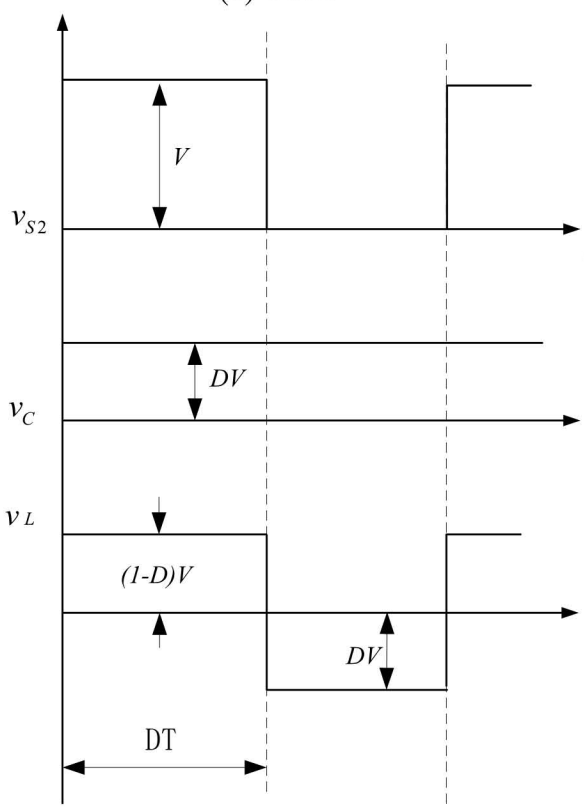
Switch cell to generate square wave



(a) buck

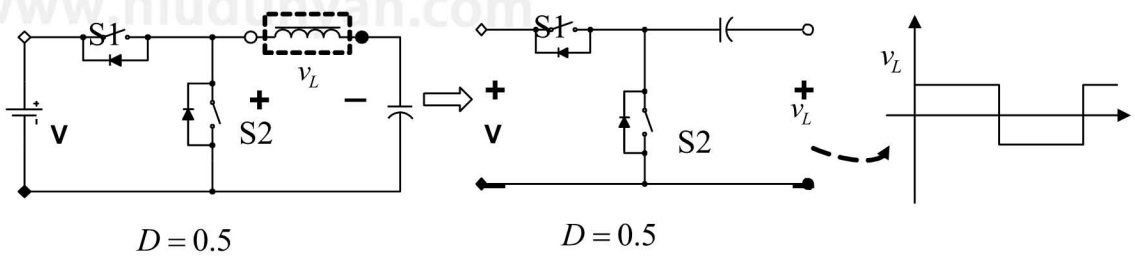


- In the steady state, output DC voltage of buck converter $v_c = DV$

Inductor voltage

$$v_L = v_{S2} - v_C$$

If D=0.5, inductor voltage is square wave



- With duty cycle=0.5, the switch cell output is square wave

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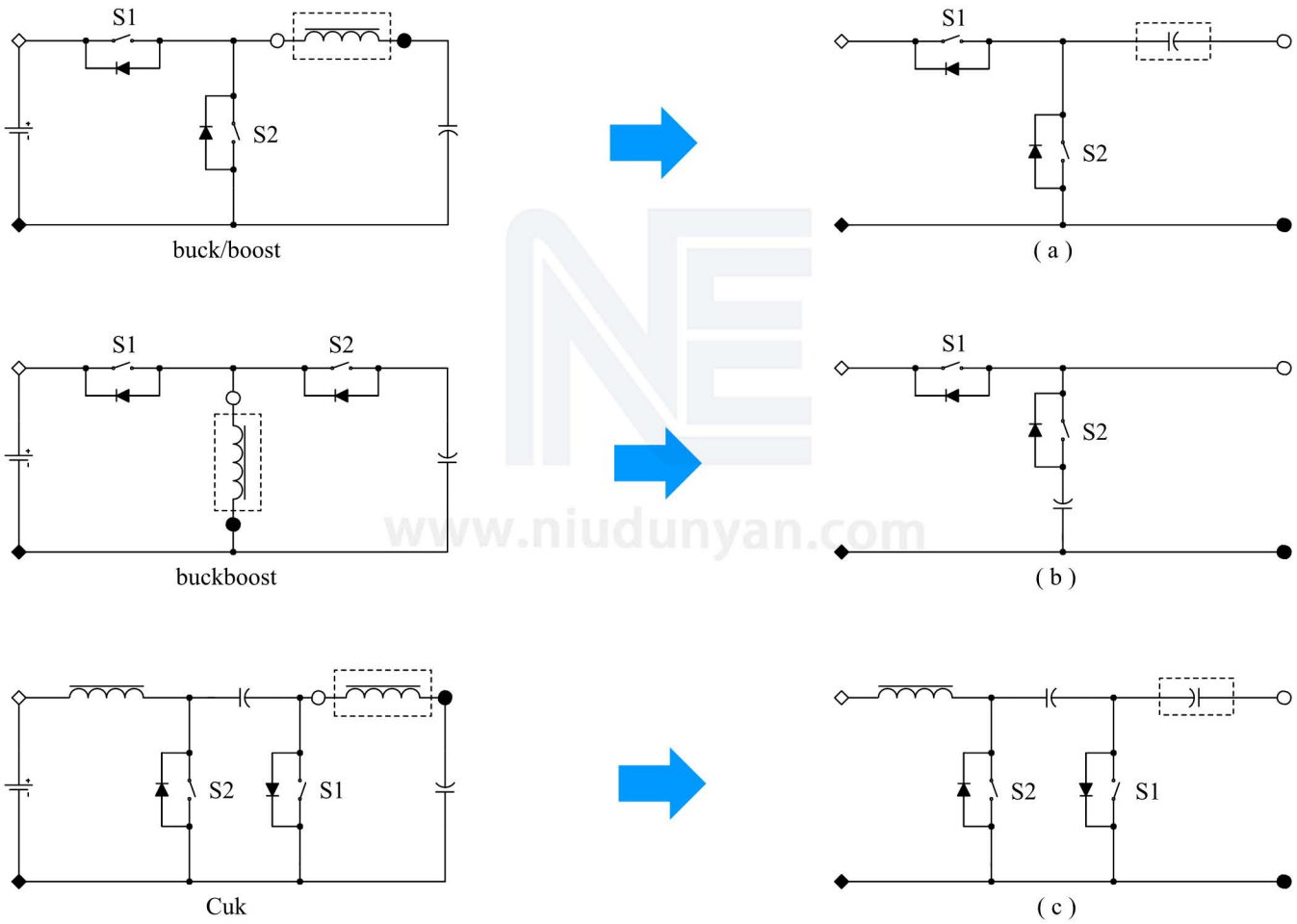
Switch Cells --- (1/4)



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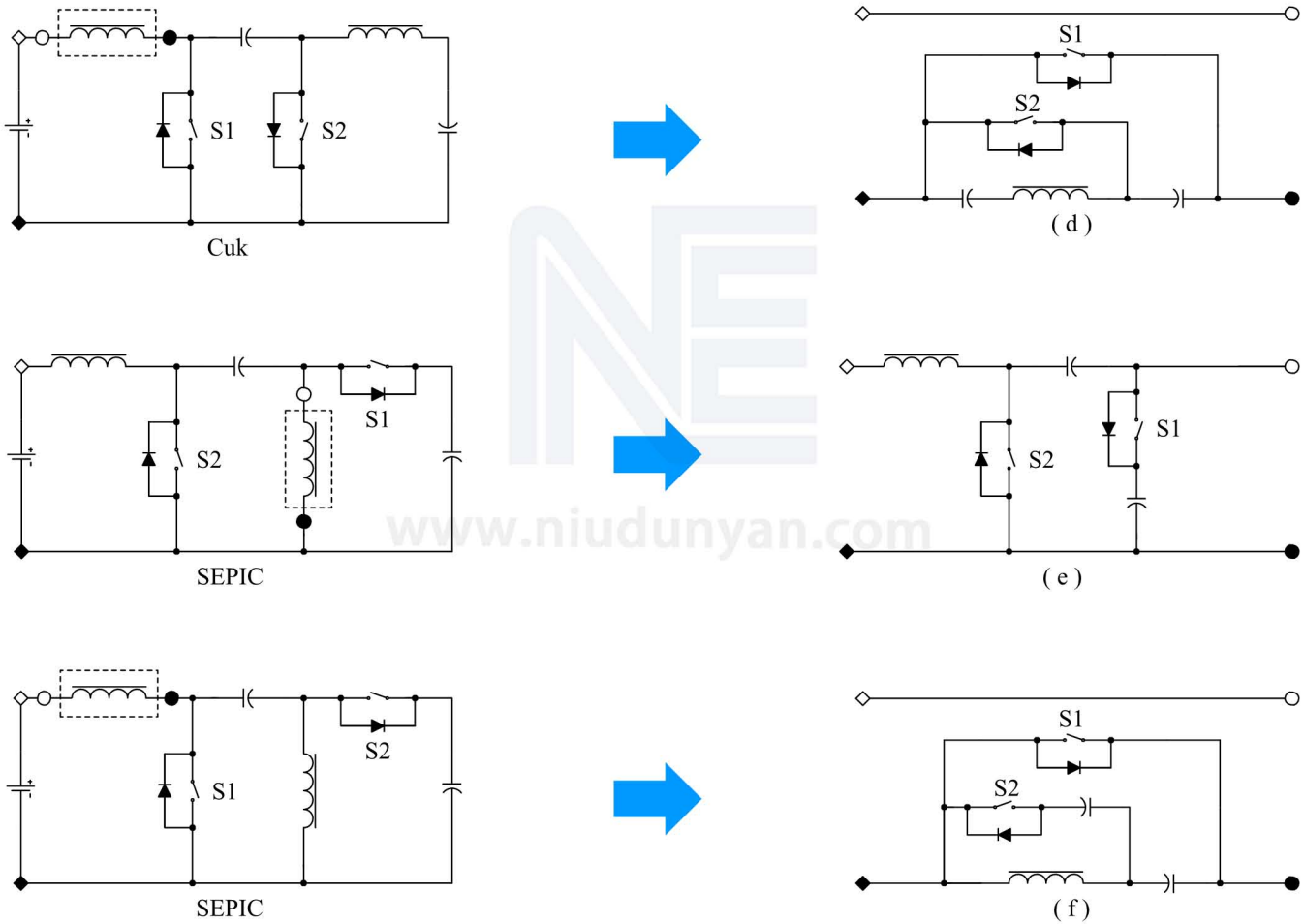
Switch Cells --- (2/4)



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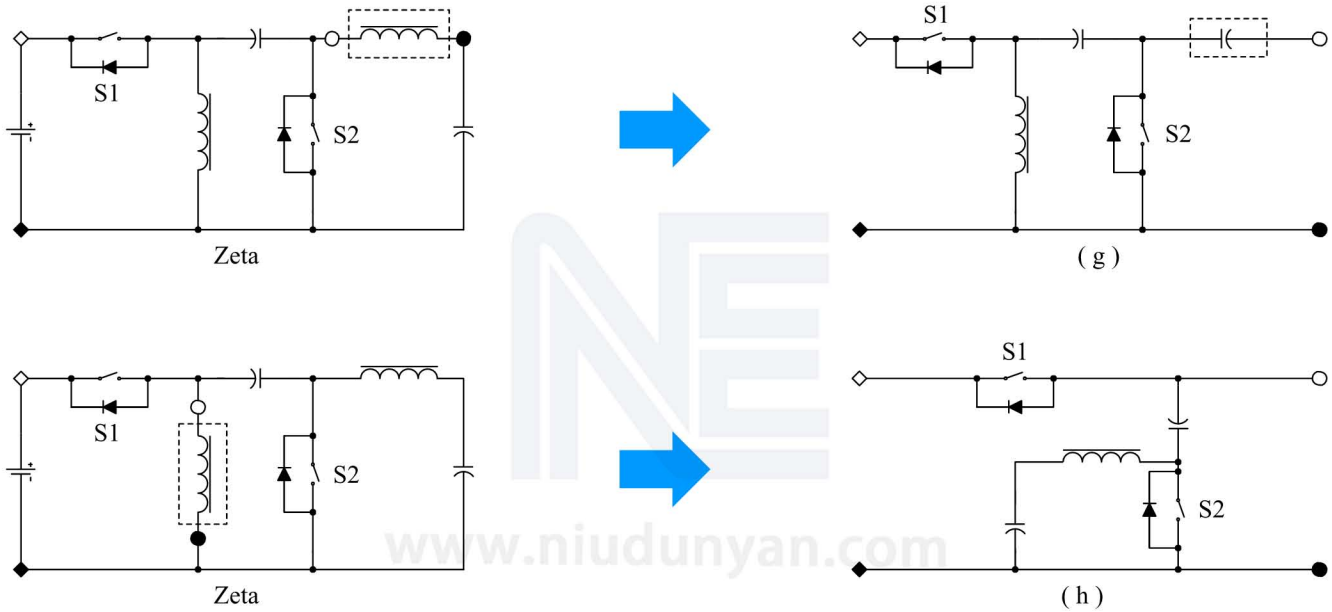
Switch Cells --- (3/4)



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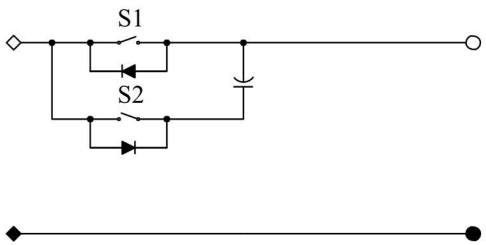
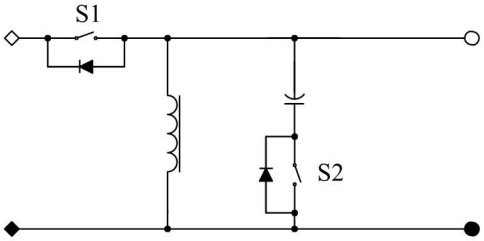
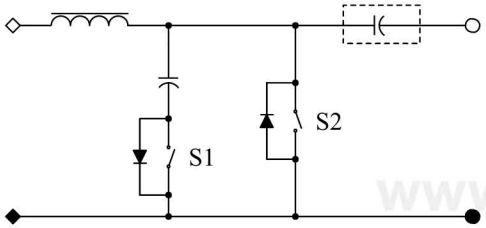
Switch Cells --- (4/4)



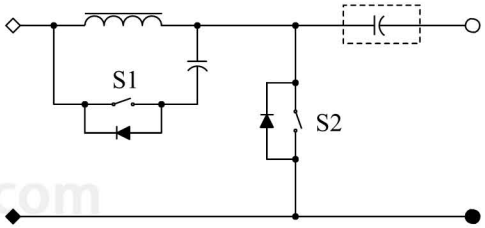
(i)



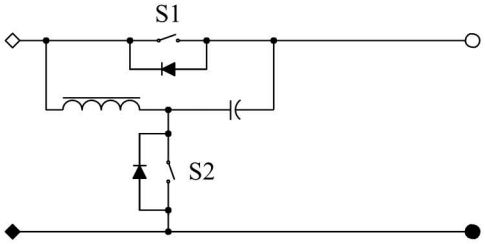
(j)



(k)



(l)



(m)

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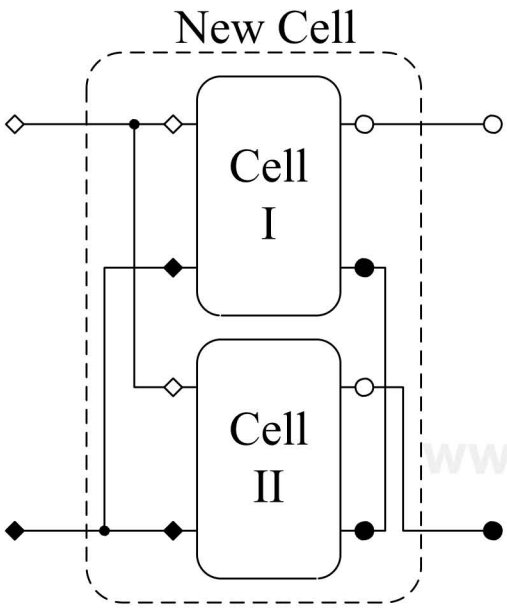
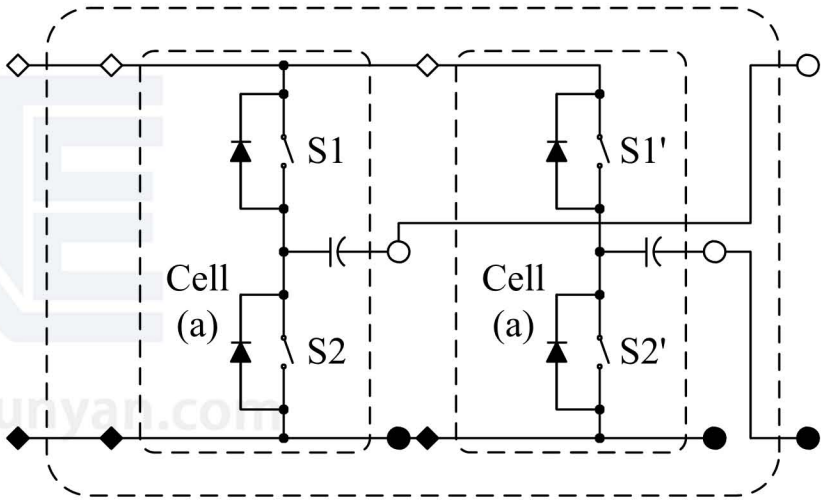
New switch cells generation with switch cells



New Switch cell generation

example



New switch cell

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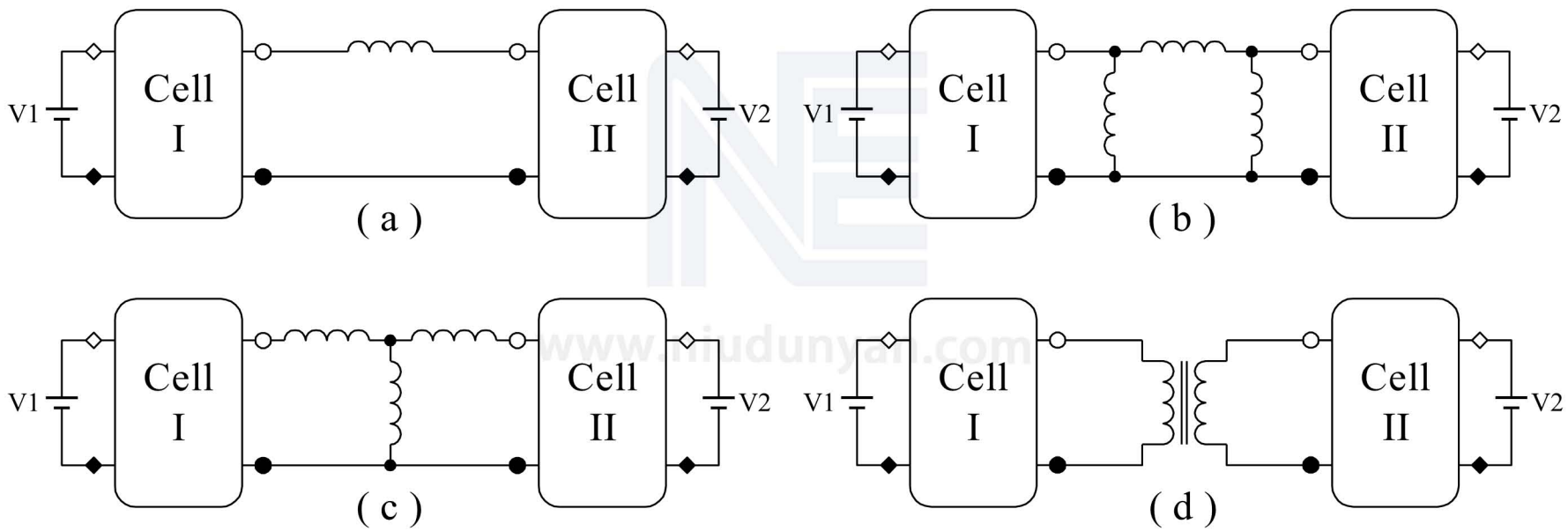
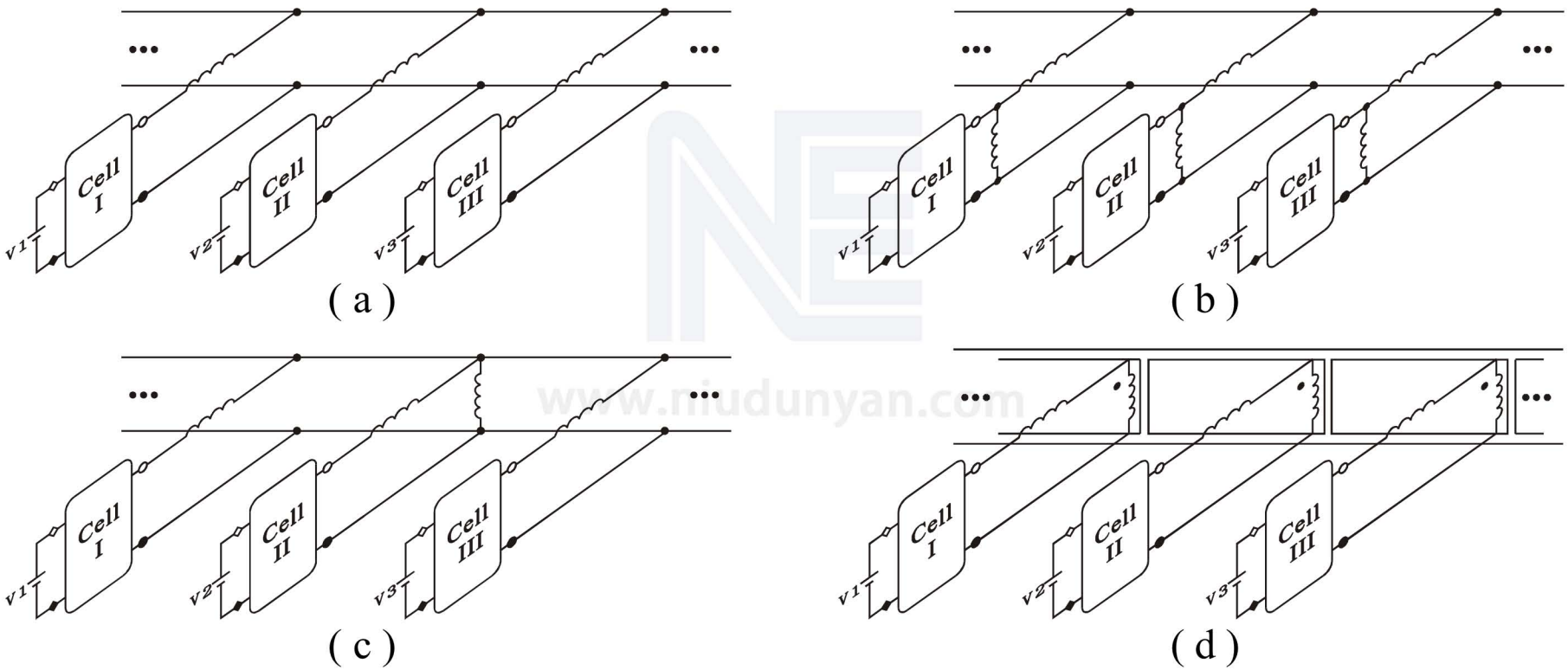
New family of phase-shift bi-directional DC-DC

Single-input and single-output converter



New family of phase-shift bi-directional DC-DC

Multi-input and/or multi-output converter



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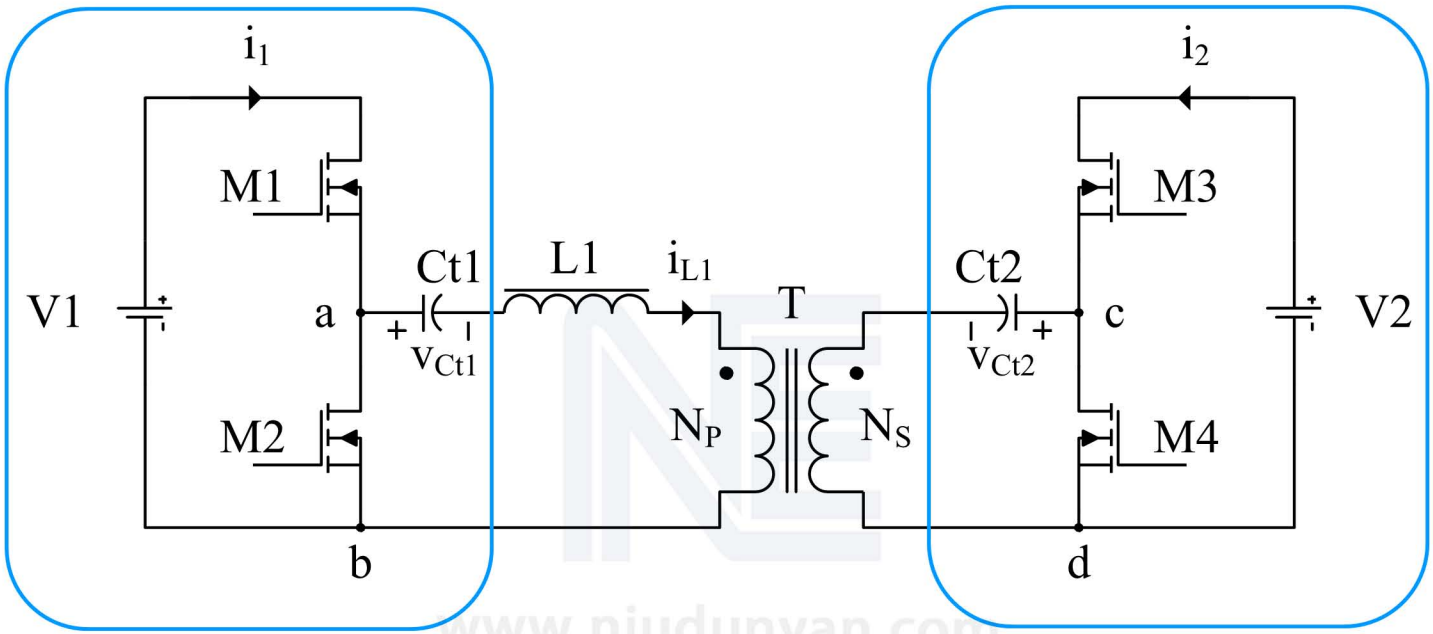
Example 1: build new phase-shift bi-directional DC-DC with Switch Cells



Switch cell (a)

Switch cell (a)

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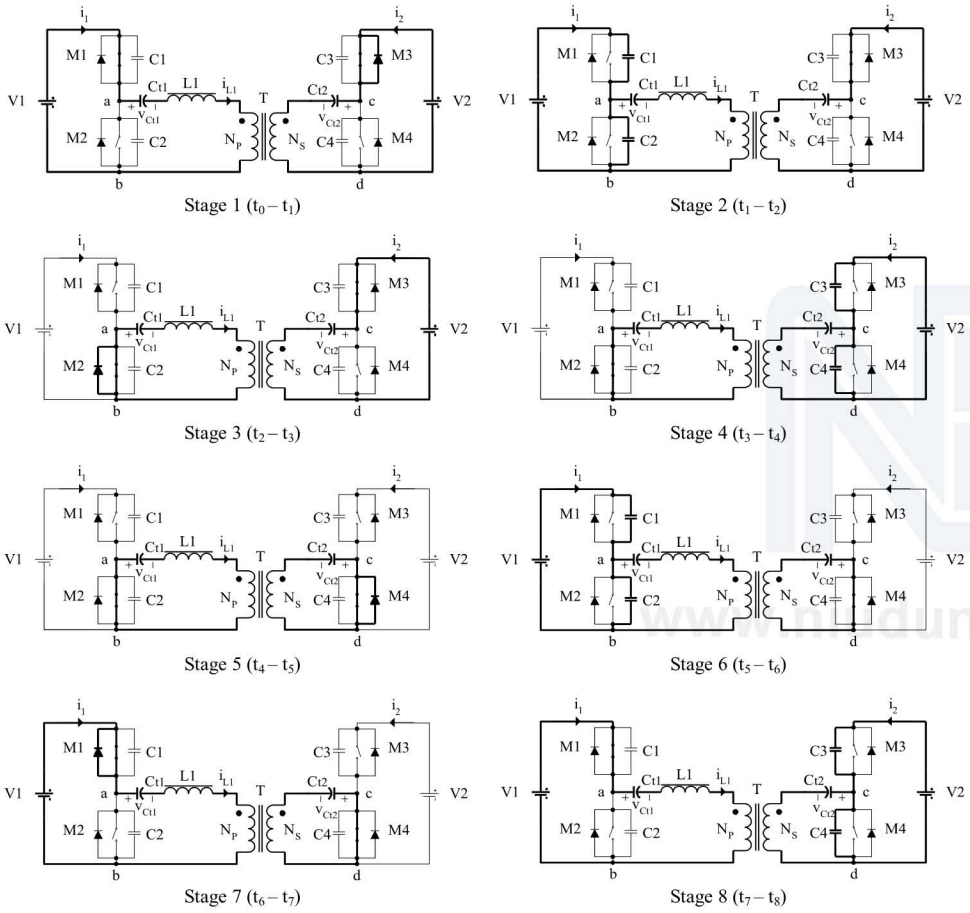
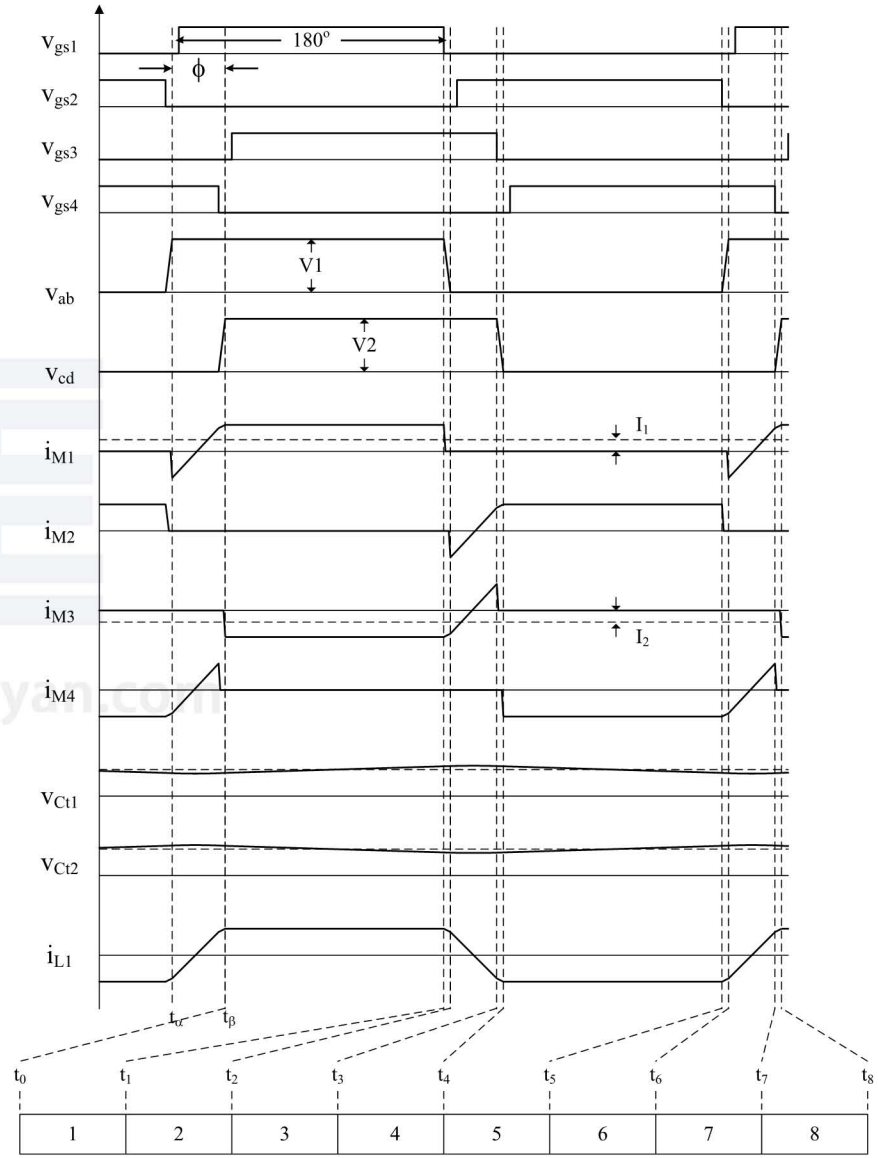
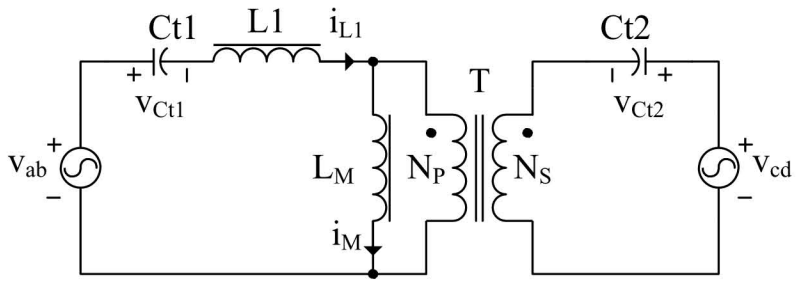
Stage Analysis in the Forward Mode





Steady state analysis



$$\frac{d}{dt}\begin{bmatrix} I_M \\ I_{L1} \\ V_{Ct1} \\ V_{Ct2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & \frac{-N}{L_M} \\ 0 & 0 & \frac{-1}{L_1} & \frac{N}{L_1} \\ 0 & \frac{1}{C_{t1}} & 0 & 0 \\ \frac{N}{C_{t2}} & \frac{-N}{C_{t2}} & 0 & 0 \end{bmatrix} \begin{bmatrix} I_M \\ I_{L1} \\ V_{Ct1} \\ V_{Ct2} \end{bmatrix} + \begin{bmatrix} 0 & \frac{N}{2L_M} \\ \frac{1}{2L_1} & -\frac{N}{2L_1} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} V_{ab} \\ V_{cd} \end{bmatrix}$$

$$V_{Ct1} = \frac{V_1}{2} \qquad V_{Ct2} = \frac{V_2}{2}$$

V1 I_1 I_2 V2

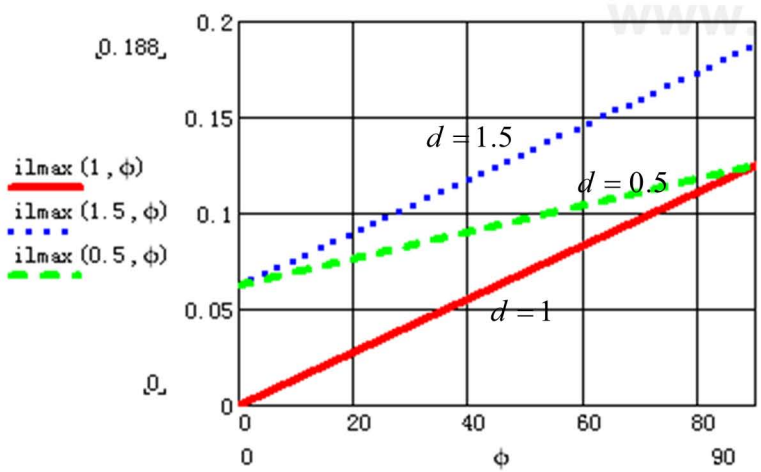
I_M is magnetizing current L_M, I_{L1} is inductor *L1 current*

$$P = \frac{\phi(180 - |\phi|) N V_1 V_2 T}{259200 L_1}$$

Peak inductor current

$$|i_{L1(\max)}| = \frac{\left[\max(V_1, NV_2) - \left(1 - \frac{\phi}{90}\right)\min(V_1, NV_2)\right]T}{8L_1}$$

$$|i_{L1(\max)}| / \frac{V_1 T}{L_1} = \frac{\left[\max(1, d) - \left(1 - \frac{\phi}{90}\right)\min(1, d)\right]}{8}$$



Peak Inductor current vs. *d* and *Φ*

Peak inductor current increases when *d* deviates from unit

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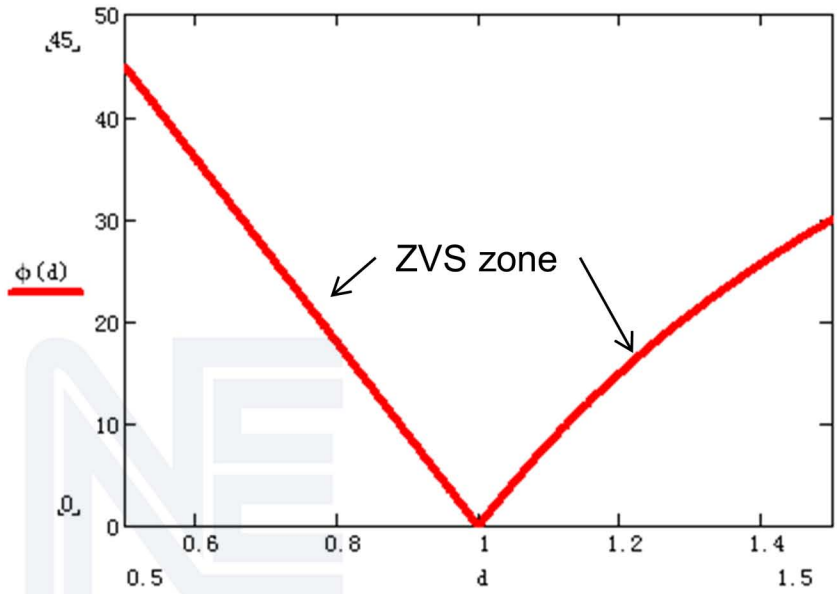
ZVS condition

$$|\phi| > \frac{90|1-d|}{\max(1,d)}$$



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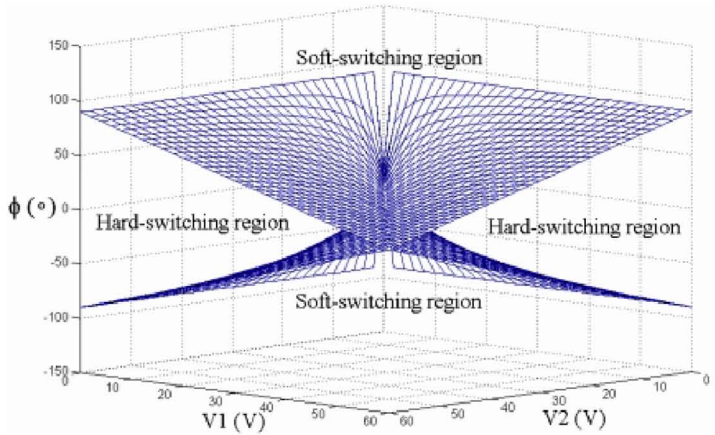
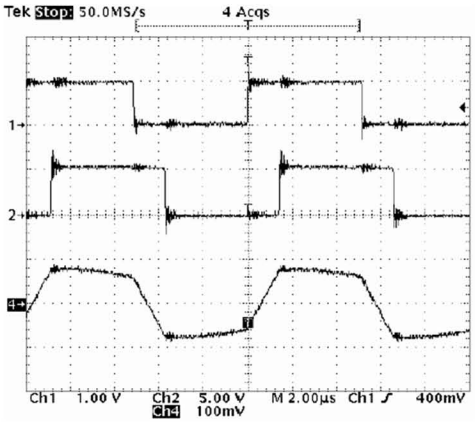
$$|\phi| > \frac{90|V_1 - NV_2|}{\max(V_1, NV_2)}$$

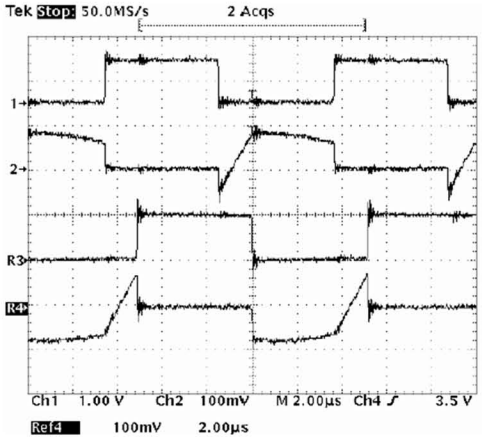


Experiment

Parameters:V_1=48V(40V~60V)； V_2=48V(40V~60V)；
N=1； L1=5.2uH； Ct1=Ct2=8.6uF； f=100kHz

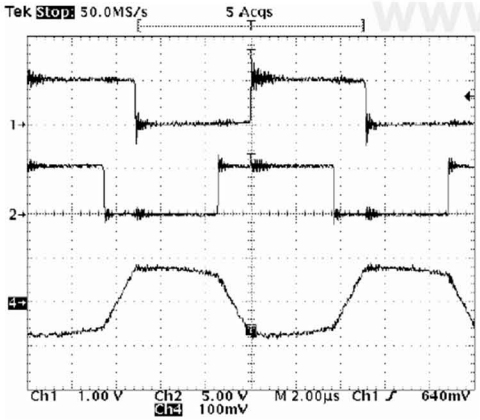


(1): v_{ab} (50V/div); (2): v_{cd} (50V/div);
(3): i_P (10A/div).

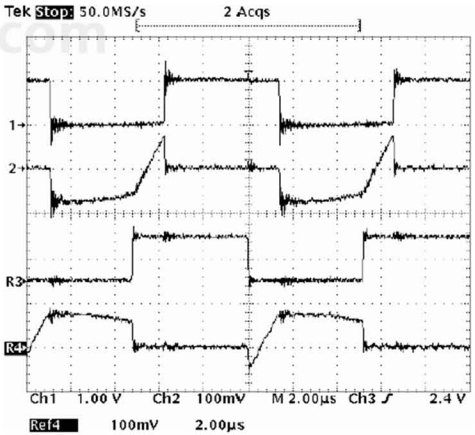


(1): v_{ds} (M1) (50V/div); (2): i_d (M1) (10A/div);
(3): v_{ds} (M3) (50V/div); (4): i_d (M3) (10A/div).

Forward mode



(1): v_{ab} (50V/div); (2): v_{cd} (50V/div);
(3): i_P (10A/div).



(1): v_{ds} (M1) (50V/div); (2): i_d (M1) (10A/div);
(3): v_{ds} (M3) (50V/div); (4): i_d (M3) (10A/div).

Backward mode

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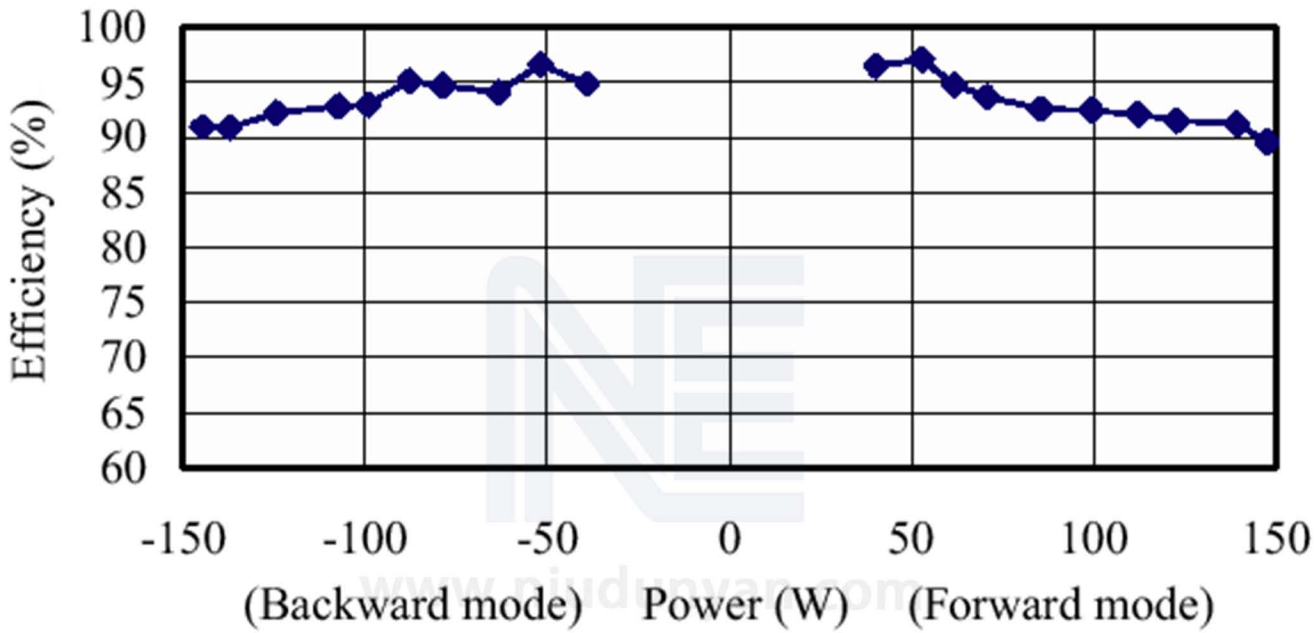
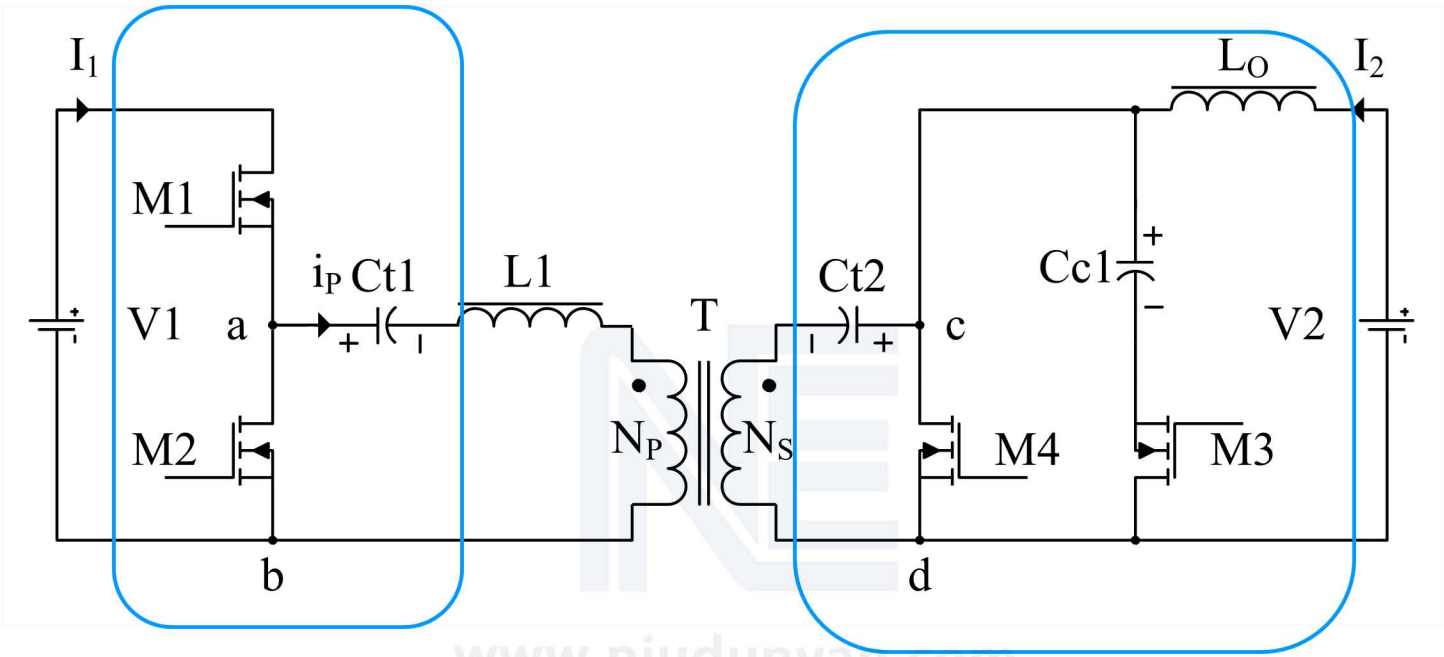
Experiment



Conversion efficiency vs. power

Example 2: build new phase-shift bi-directional DC-DC with Switch Cells

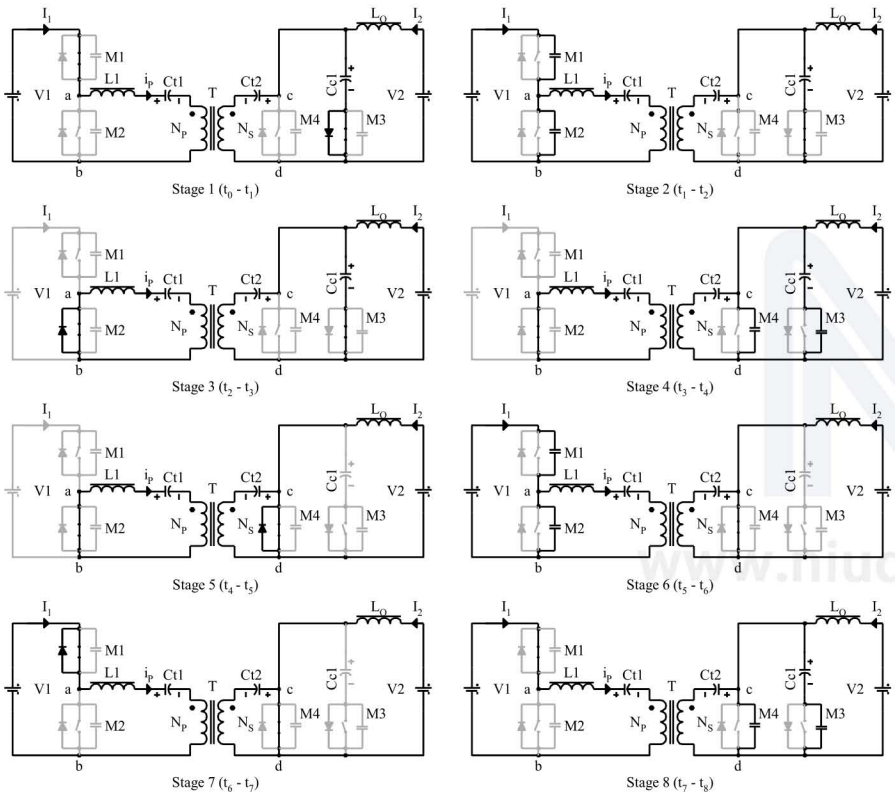


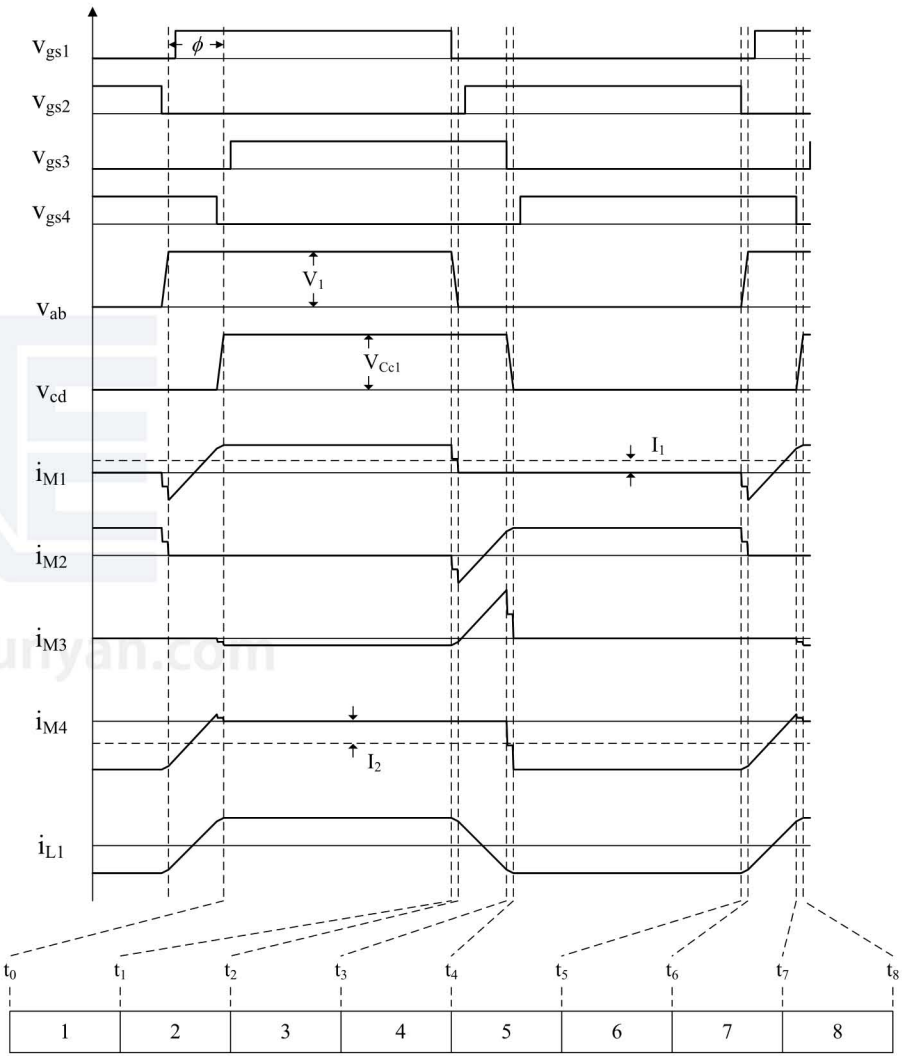
Switch cell (a)

Switch cell (k)

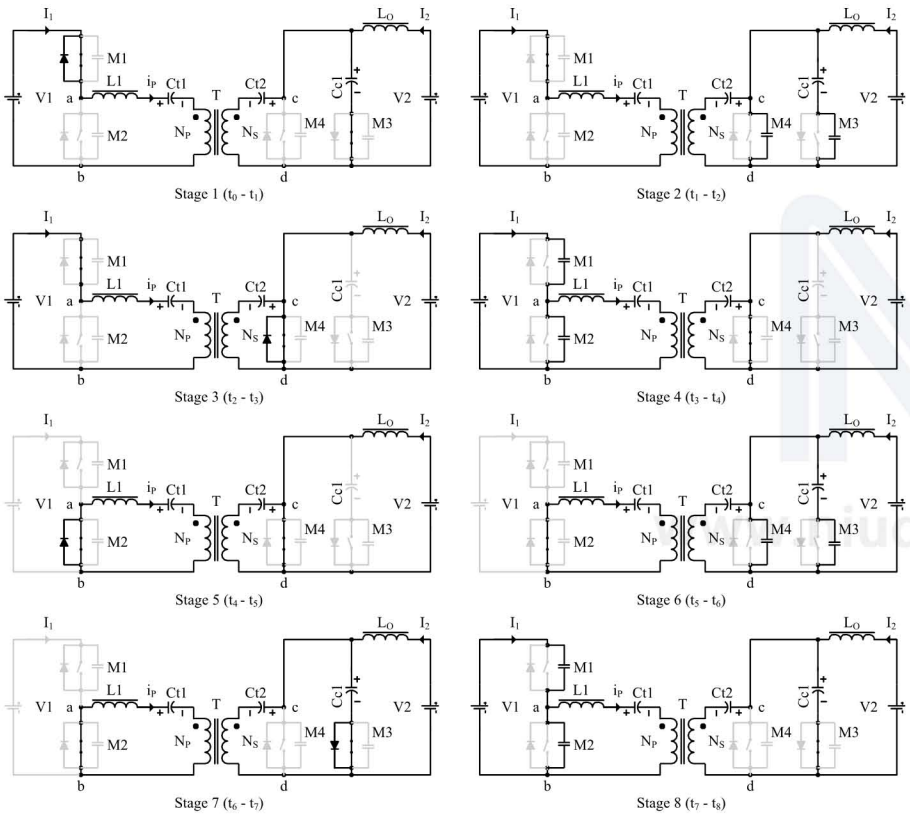
By adjusting the phase angle between two switch cells, power flow can be controlled

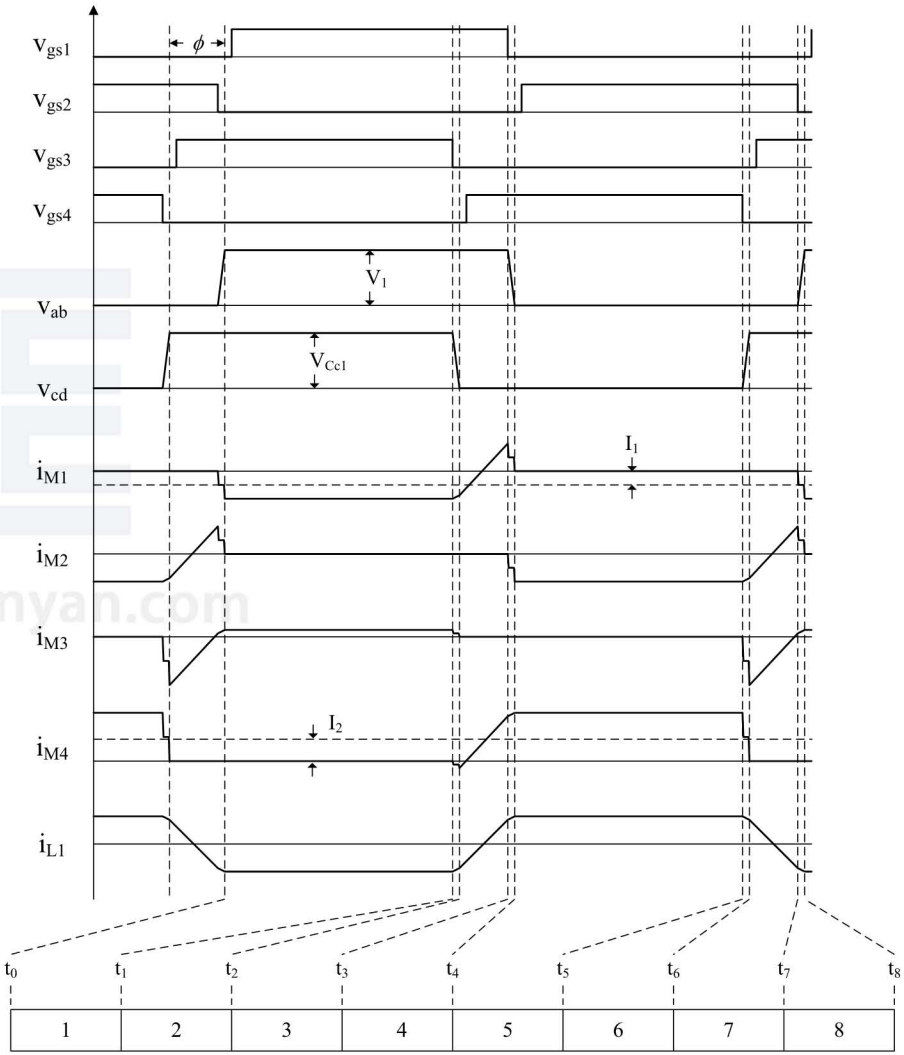
Stage Analysis in the Forward Mode



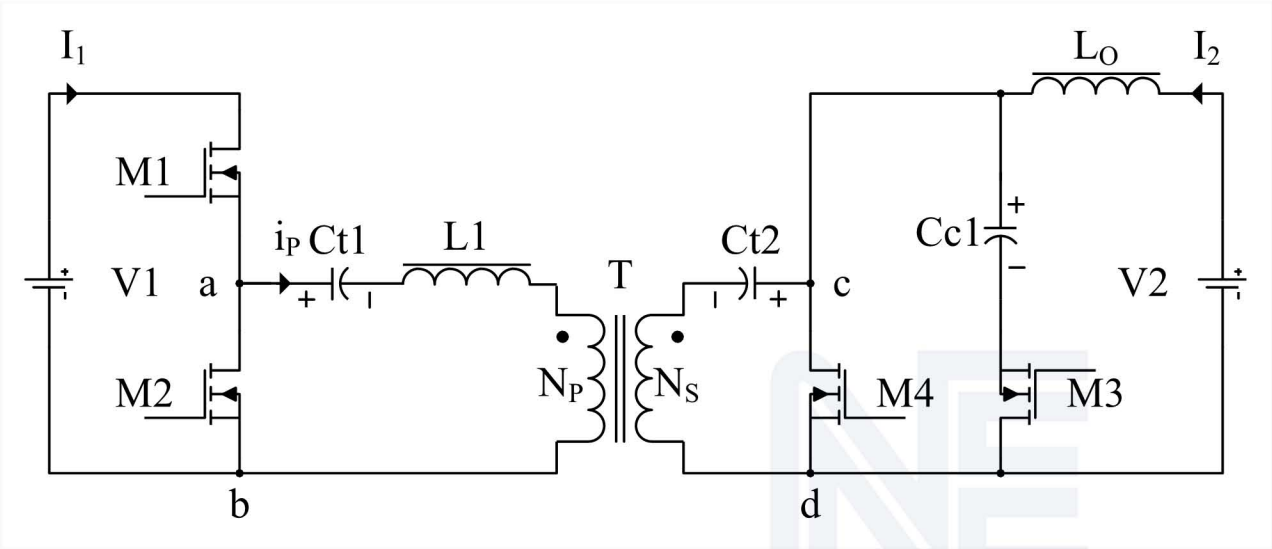


Stage Analysis in the Backward Mode





Power Control



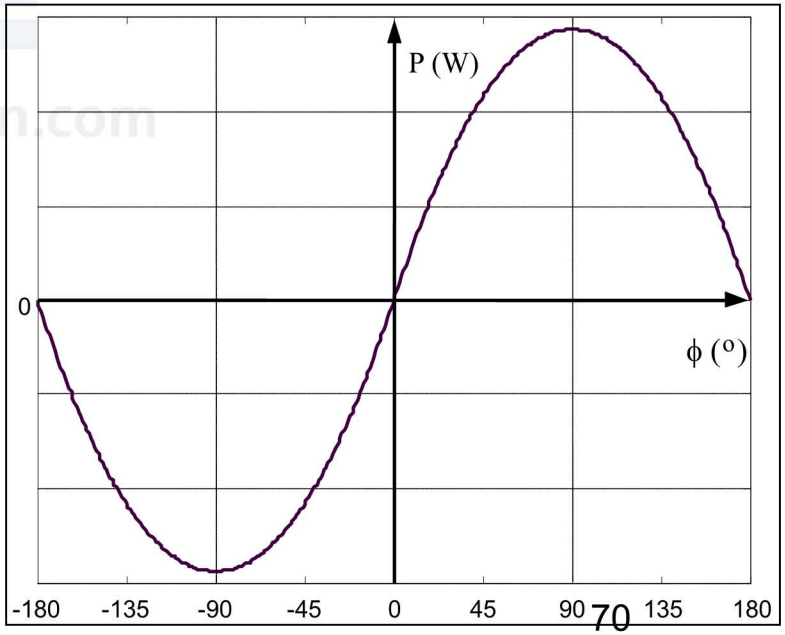
$$V_{Ct1} = \frac{V_1}{2}$$

$$V_{Ct2} = V_2$$

$$V_{Cc1} = 2V_2$$

Vab: square with peak to peak value of V_1
Vcd: square with peak to peak value of $2*V_2$

$$P = \frac{\phi\left(180 - |\phi|\right) N V_1 V_2 T}{129600 L_1}$$



Summary

- A technique to generate phase-shift bi-directional DC-DC converters is proposed.
- Examples of deriving new bi-dc/dc is presented
- All switches achieve ZVS in both the forward mode and the backward mode in theory

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Chapter 4
Bidirectional DC/DC converter with PWM plus phase-shift control

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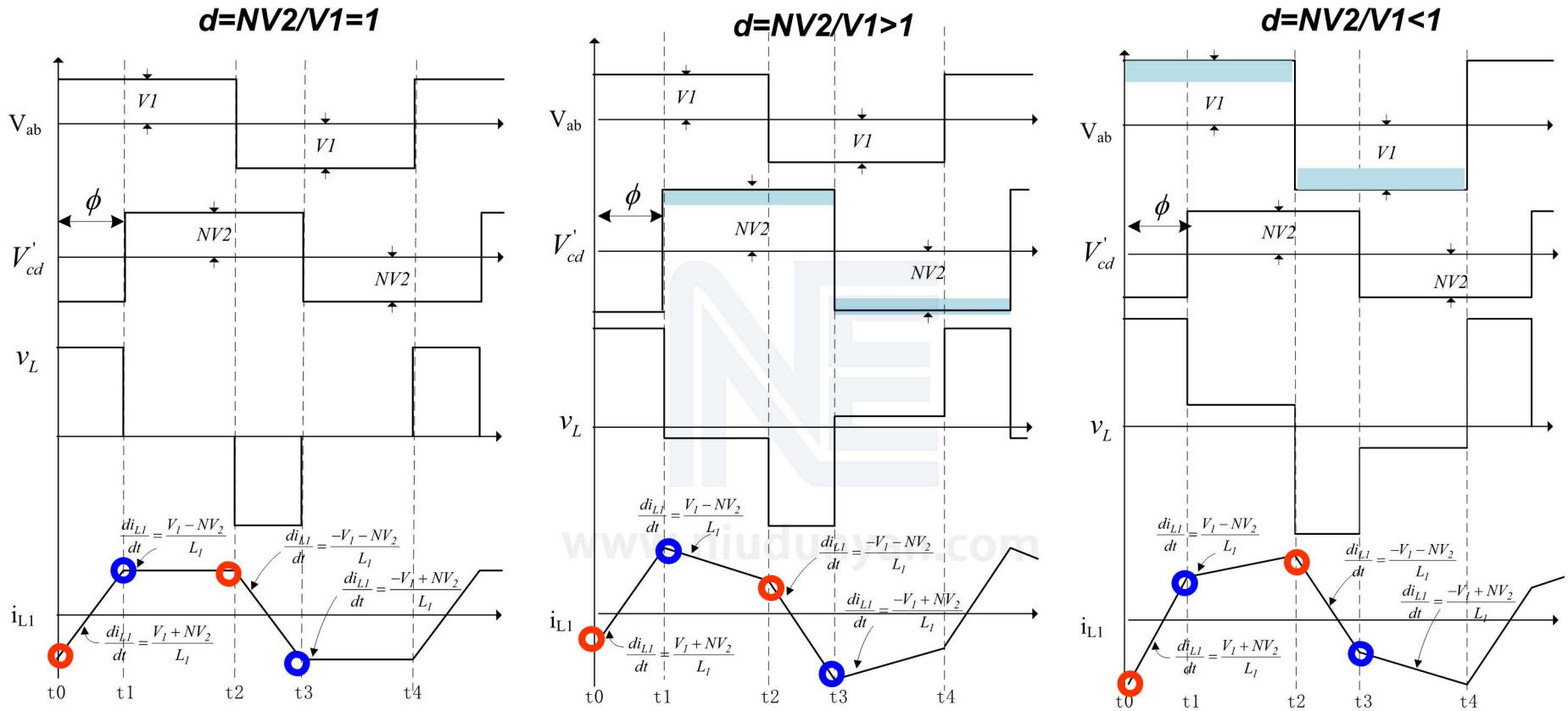
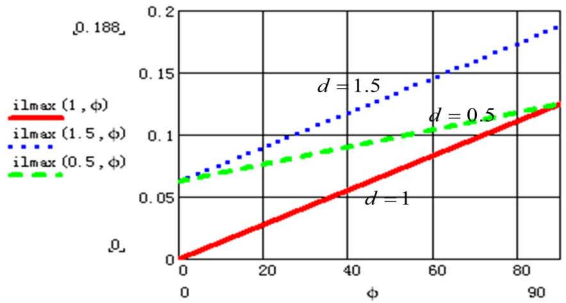
Outline

- Why PWM plus phase-shift control?
- Example of bidirectional DC-DC converter with PWM plus phase-shift
- Synthesis of bidirectional DC-DC converters topologies with PWM plus phase-shift
- Summary

DAB with phase-shift control

@phase angle>0



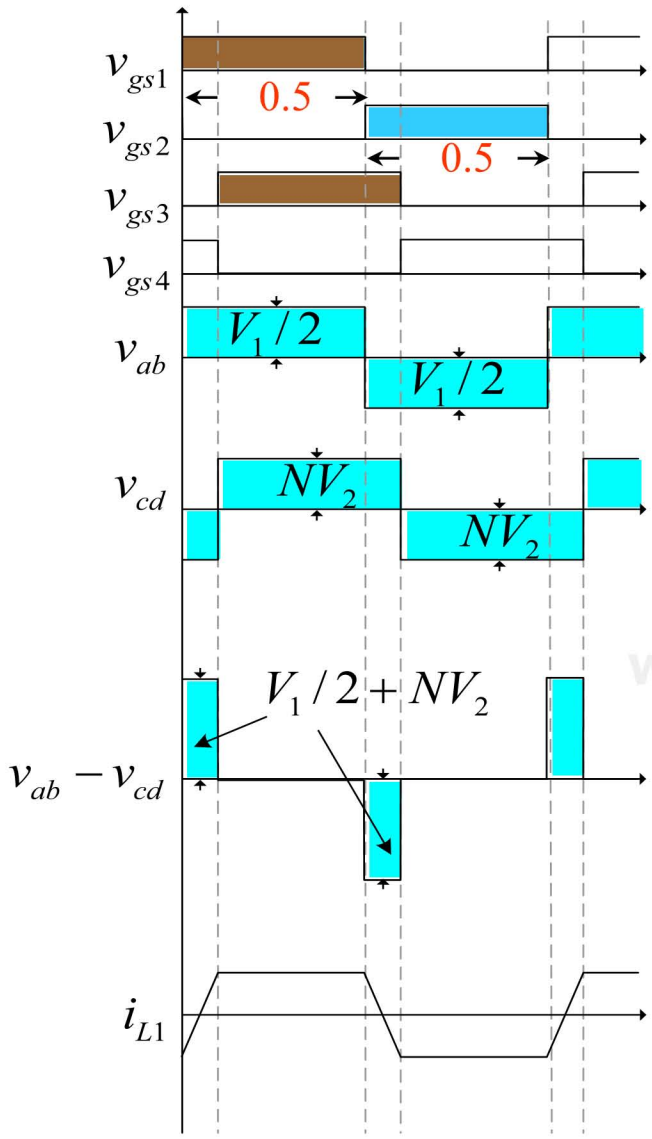


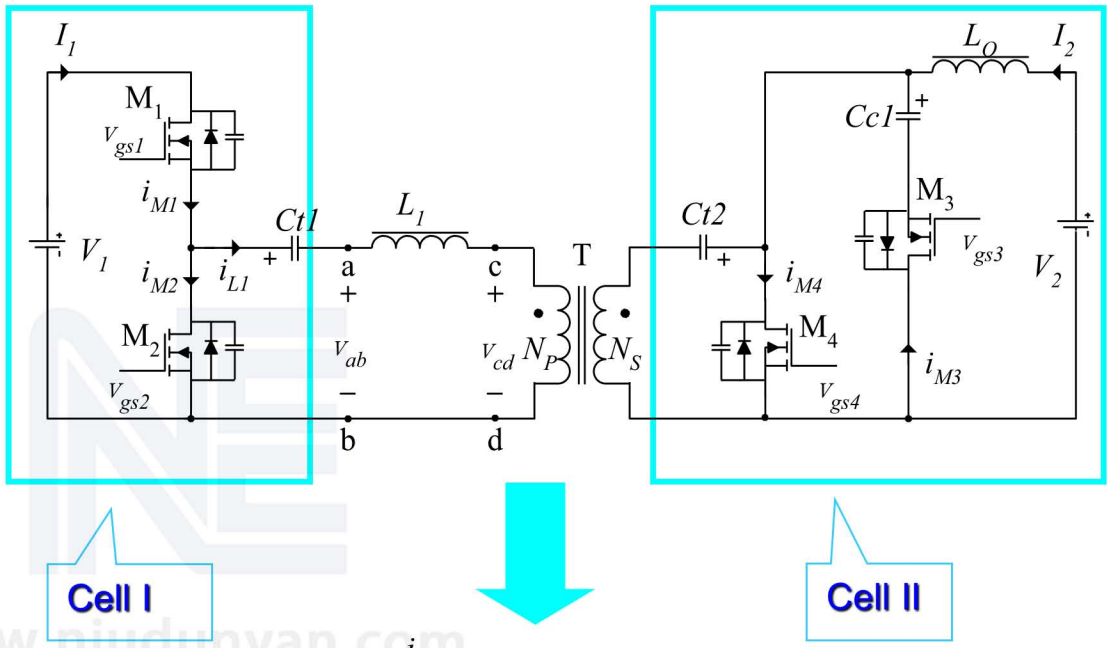
Peak inductor current vs. d and Φ

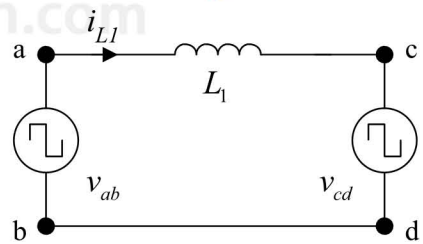
Problems when *d* deviates from 1

- Higher peak inductor current
- Higher turn-off loss due to turning off high peak inductor current
- ZVS condition of one side bridge become difficult to realize in light load
- Higher RMS current in the inductor tank and higher conducting loss

Phase-shift control with matched input and output



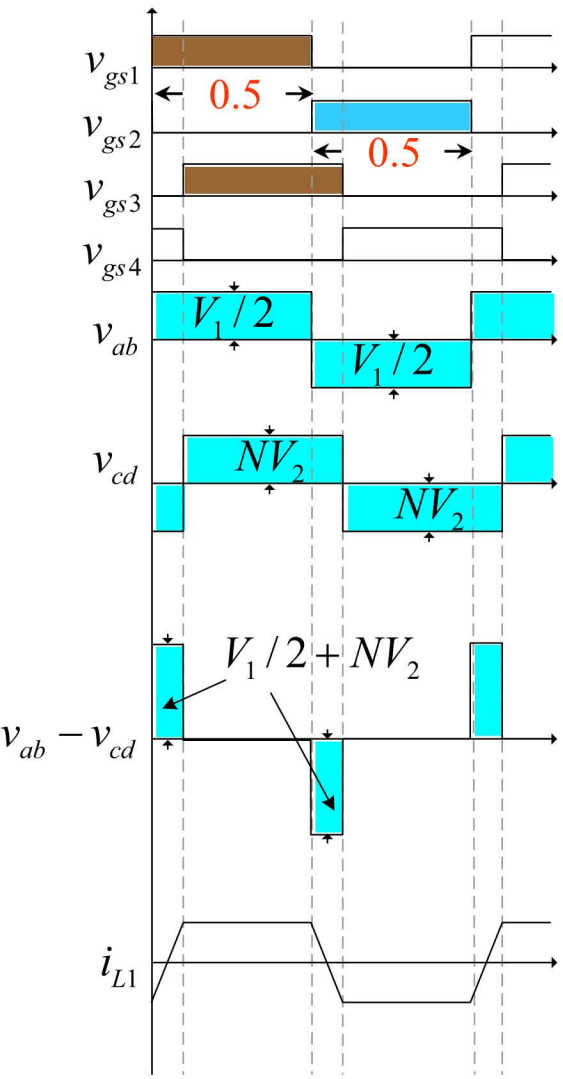




Vab: square with amplitude of 1/2V1
Vcd: square with amplitude of NV2

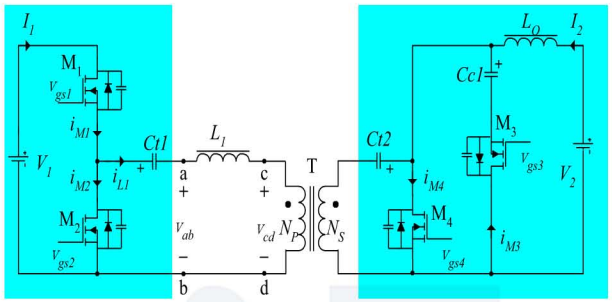
- Three level voltage is applied on the inductor
- Trapezoidal inductor current

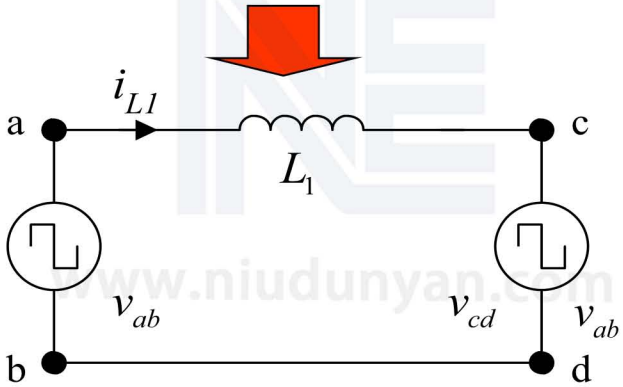
Problem of Phase-shift control



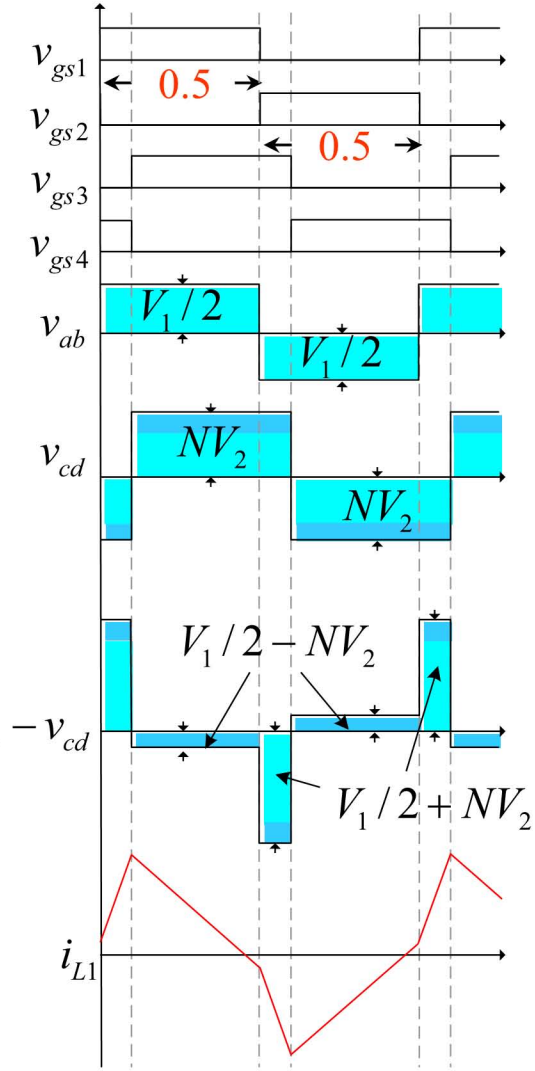
PS control when $V_1/2=NV_2$

- Three level voltage is applied on the inductor
- Trapezoidal inductor current





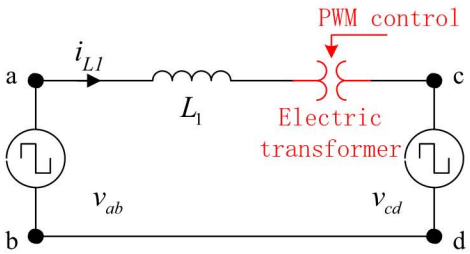
Simplified circuit of PS control

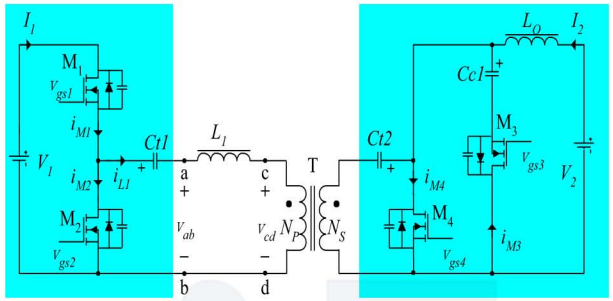


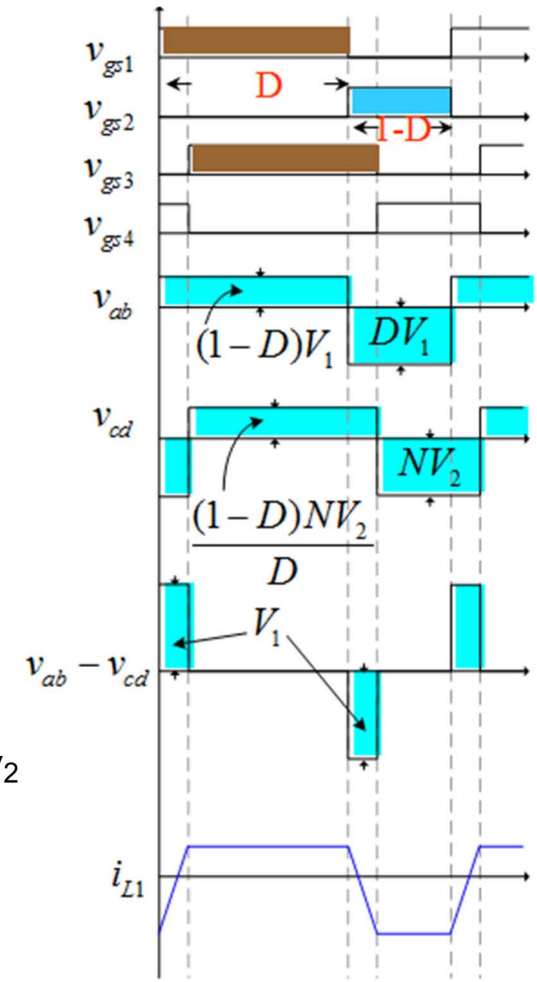
PS control when $V_1/2<NV_2$

- Four level voltage is applied on the inductor
- Triangle alike inductor current

Introducing duty cycle control







Let change the duty cycle is from 50% to D

Input converter: $V_{Ct1} = DV_1$

Vab positive amplitude : (1-D)V1
Vab negative amplitude :DV1

Output converter: $V_{Ct2} = V_2$ $\quad V_{Cc1} = \frac{V_2}{D}$

Vcd positive amplitude : (1-D)/DNV2
Vcd negative amplitude :NV2

To match the positive amplitude of both sides

$$(1-D)V_1 = \frac{(1-D)NV_2}{D} \quad \Rightarrow \quad DV_1 = NV_2$$

PPS control when $V_1/2<NV_2$

- Negative amplitude of both sides is also matched
- By introducing duty cycle control, the current recovers trapezoidal

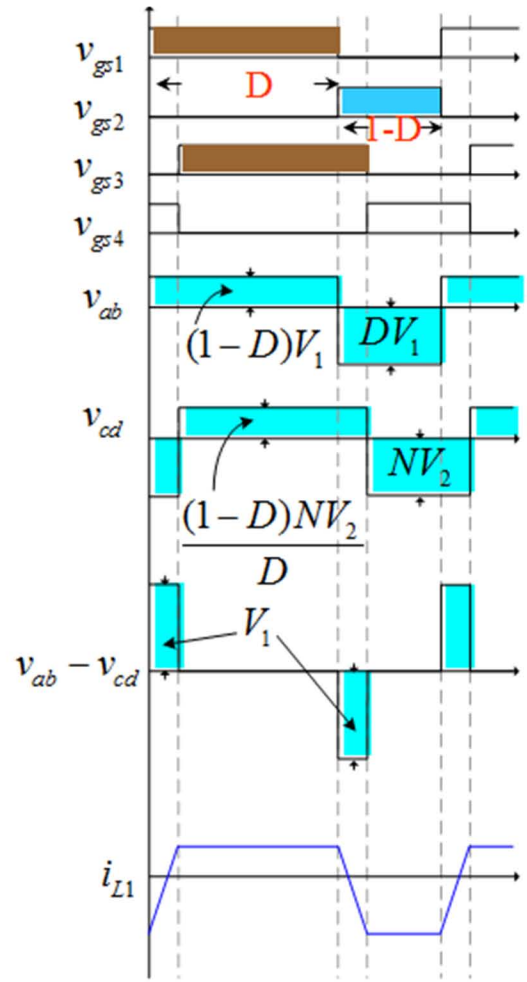
PWM + phase-shift control(PPS)

Duty cycle introduced

$$D = \frac{NV_2}{V_1}$$

Duty cycle of M1 AND M3: D

Duty cycle of M2 and M4 : 1-D



- Duty cycle depends on the input and output voltages
- When V1 or V2 deviate, primary current *ip* keep constant in stage 2 and stage 4. The current recovers trapezoidal
- Peak current reduced , current rms value is reduced
- ZVS condition is improved
- Both conducting loss and switching loss are reduced

PPS control when $V_1/2<NV_2$

Power control under PWM+phase-shift (PPS) control

Power transferred with PPS

$$P = \frac{NV_1V_2T}{2\pi L_1}\phi(1 - D - \frac{|\phi|}{4D\pi})$$

For Phase-shift control, D=0.5

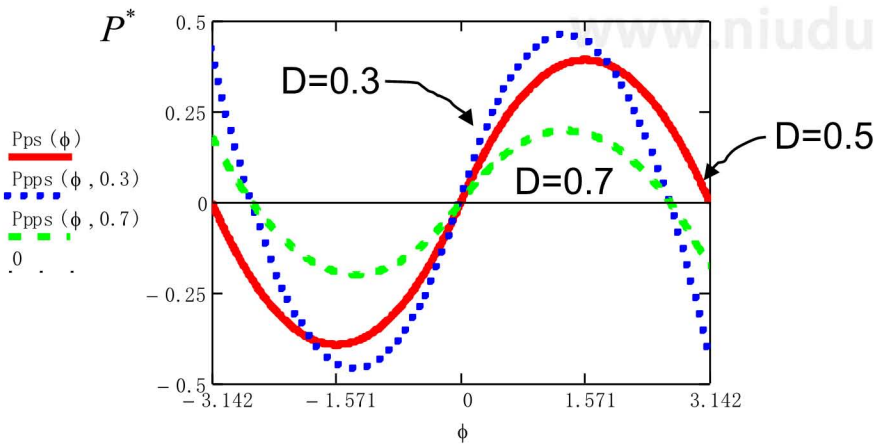
$$P = \frac{NV_1V_2T}{2\pi L_1}\phi(1 - 0.5 - \frac{|\phi|}{4\times 0.5\pi}) = \frac{NV_1V_2T}{2\pi L_1}\phi(0.5 - \frac{|\phi|}{2\pi})$$

For PPS control with $D = \frac{NV_2}{V_1}$

$$P = \frac{NV_1V_2T}{2\pi L_1}\phi(1 - \frac{NV_2}{V_1} - \frac{|\phi|V_1}{4\pi NV_2})$$

Definition: $P^* = P / \frac{NV_1V_2T}{2\pi L_1} = \phi(1 - D - \frac{|\phi|}{4D\pi})$

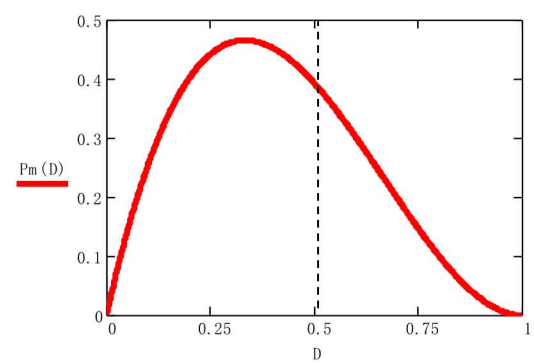
For PPS, power vs Φ relation still looks like sinusoidal profile as phase shift control



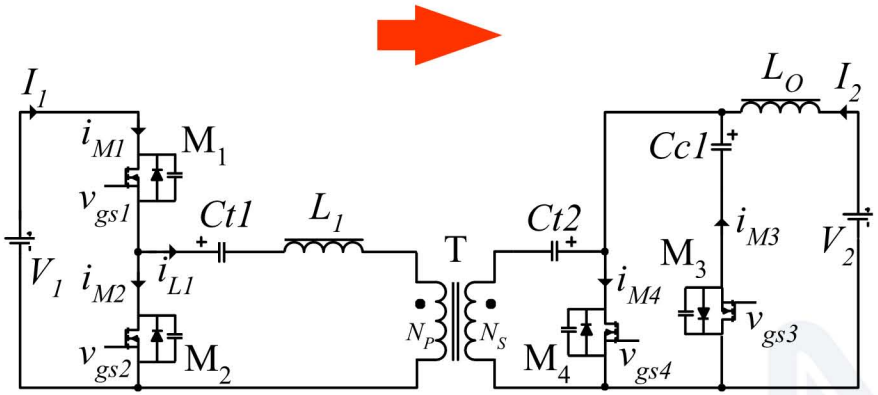
PPS controlled power vs Φ relation with different D

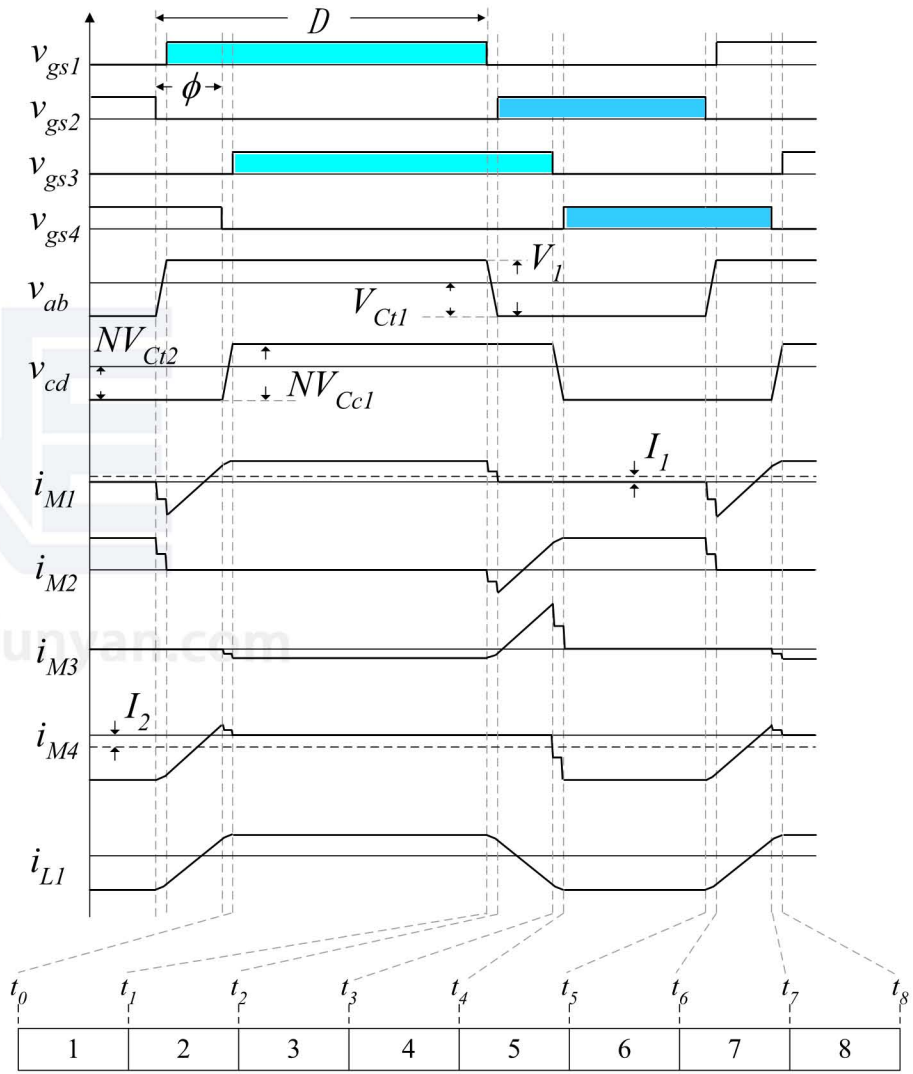
Phase-shift Φ range: $[-2\pi(1-D)D, 2\pi(1-D)D]$

Peak power: $P^*_{\max} = \pi D(1-D)^2$



Forward mode





Gate signals of M_1 and M_2 leading to those of M_3 and M_4.

Duty cycle

$$D = \frac{NV_2}{V_1}$$

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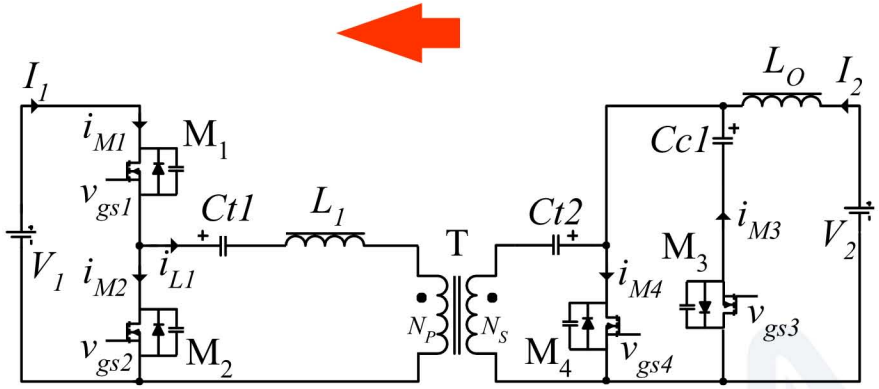
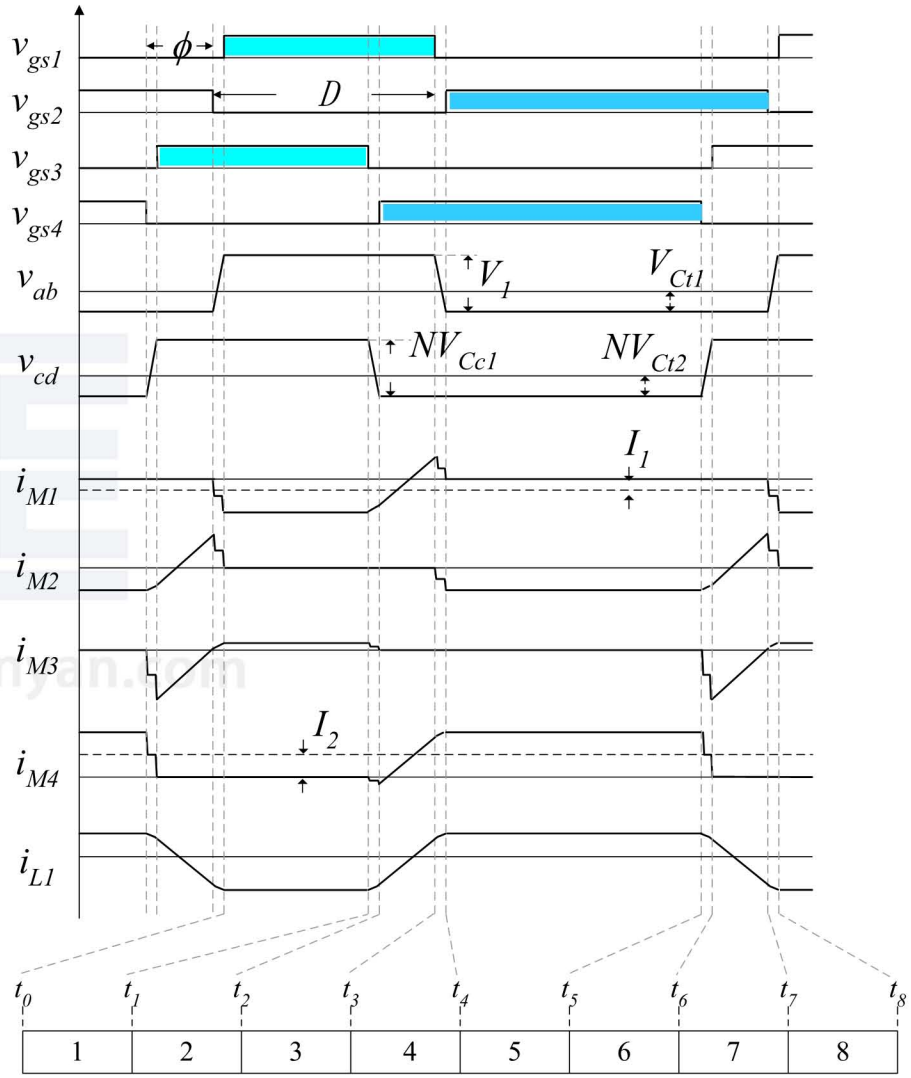
Backward mode





Gate signals of M_3 and M_4 leading to those of M_1 and M_2.

Duty cycle

$$D = \frac{NV_2}{V_1}$$

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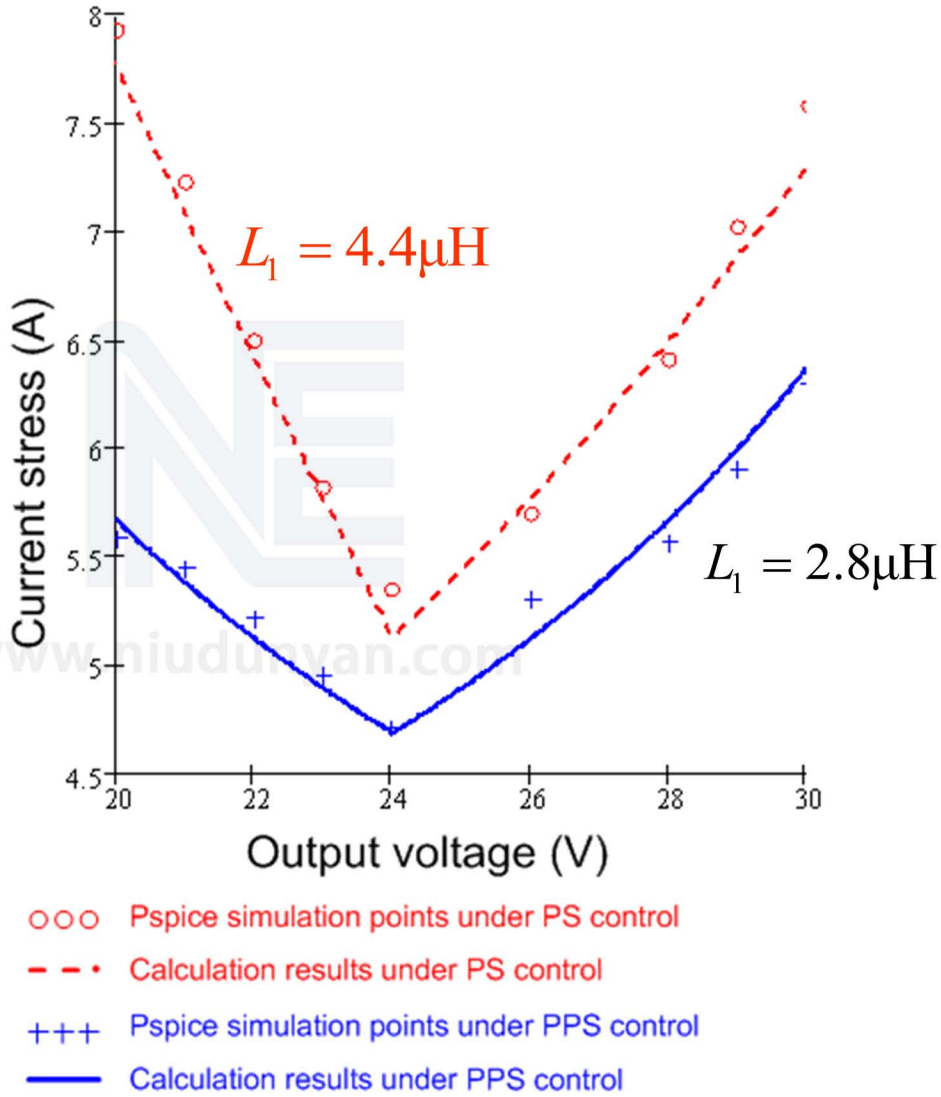
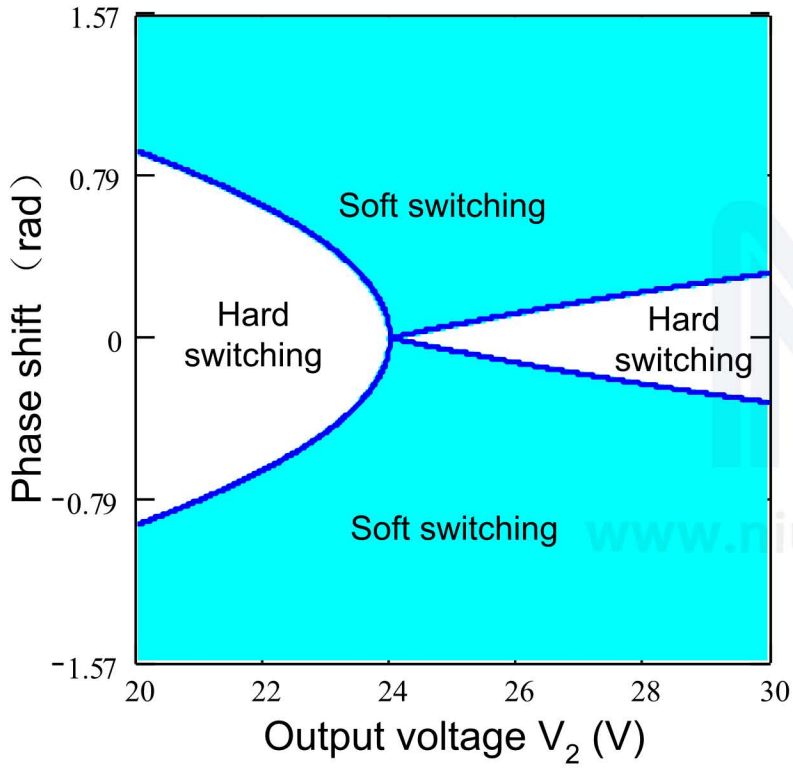
Phase control vs. PPS
Comparison of Current stress

Parameters:
V_1=48Vdc;
V_2=20Vdc ~ 30Vdc;
N_p:N_s=1:1;
P=100W
f=100kHz
Optimized Inductance is used for each case

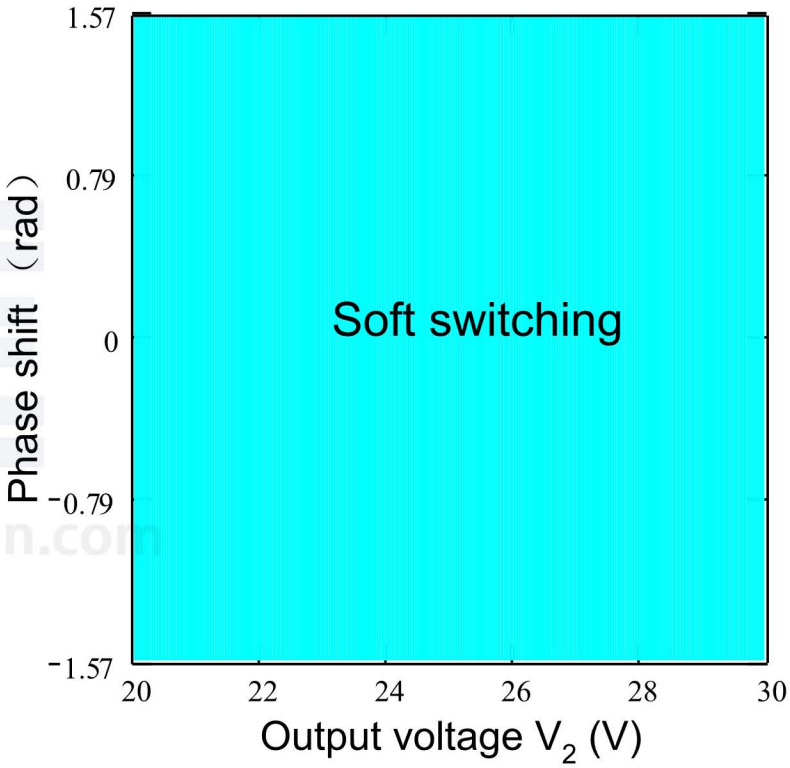


Phase control vs. PPS

Comparison of ZVS range

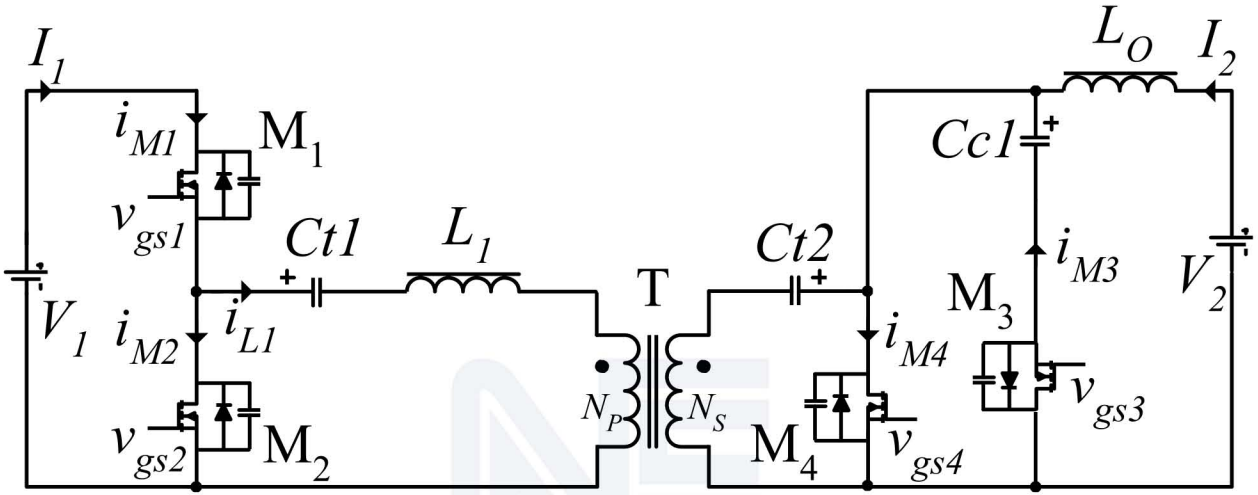


ZVS range under PS control



ZVS range under PPS control

Experiment(1/5)



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Conditions:

V_1=48Vdc, V_2=24Vdc~30Vdc, *Np: Ns*=1:1,

L_0=140μH, *Ct1*=*Ct2*=13μF, *Cc1*=2.2μF, *f*=100kHz,

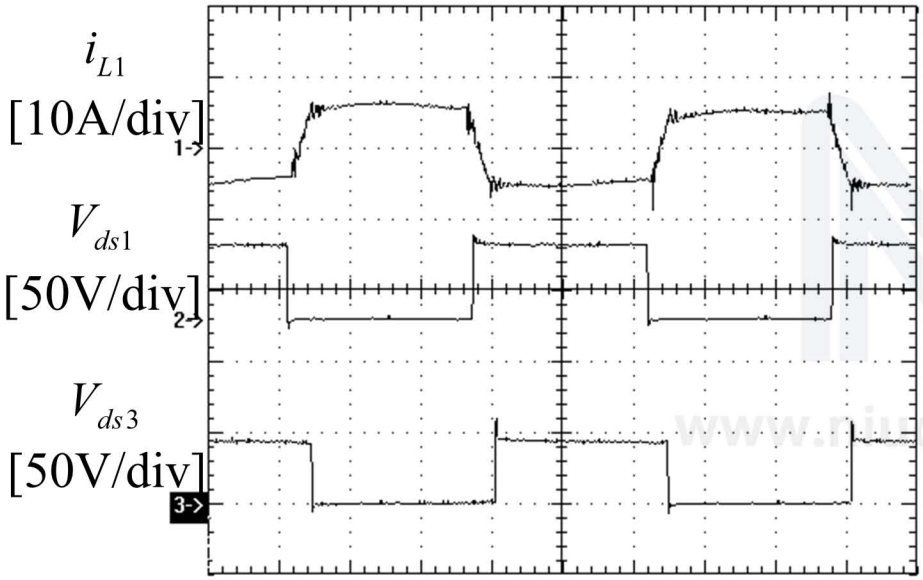
M_1~M_4: *MOSFET*

PPS control: L_1=2.8μH

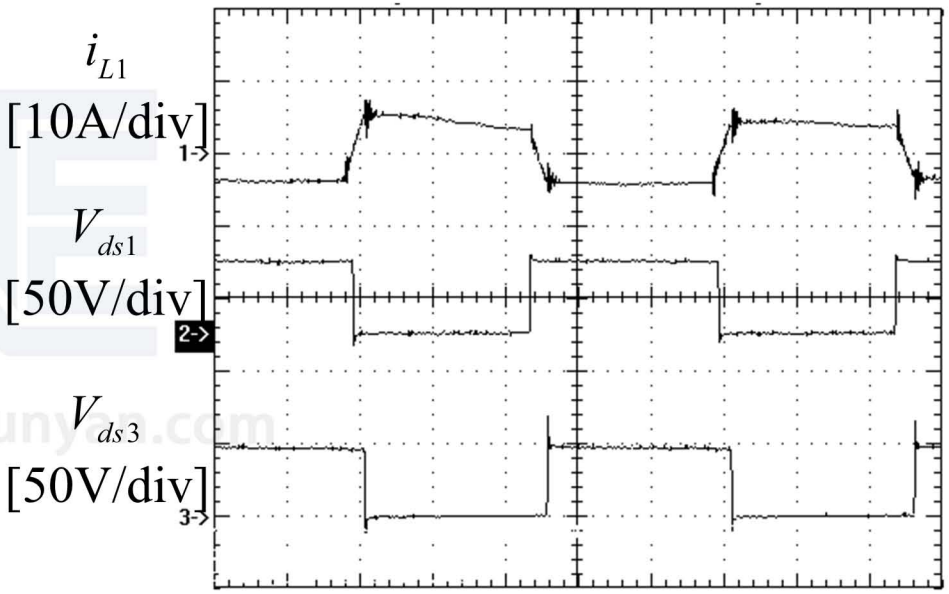
PS control: L_1=4.4μH,

Experiment (2/5)

Output voltage : 24V, output power :100W



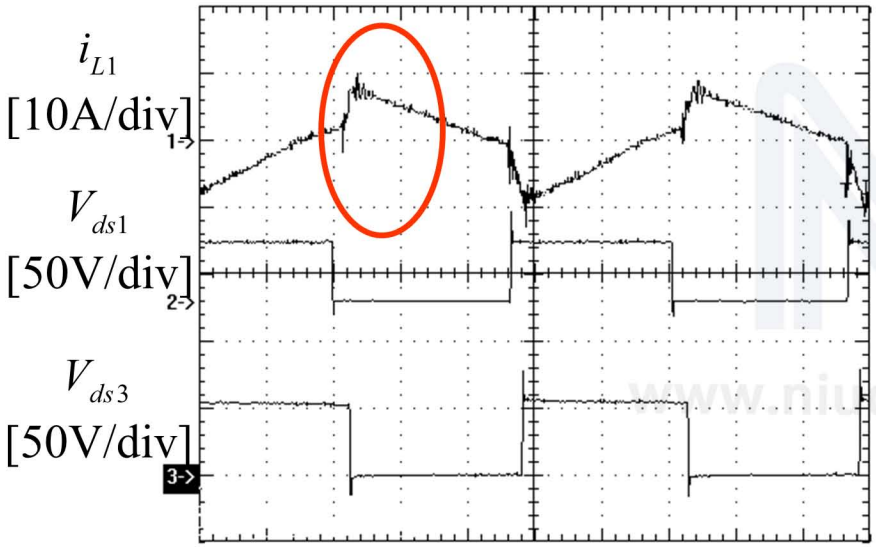
PS control



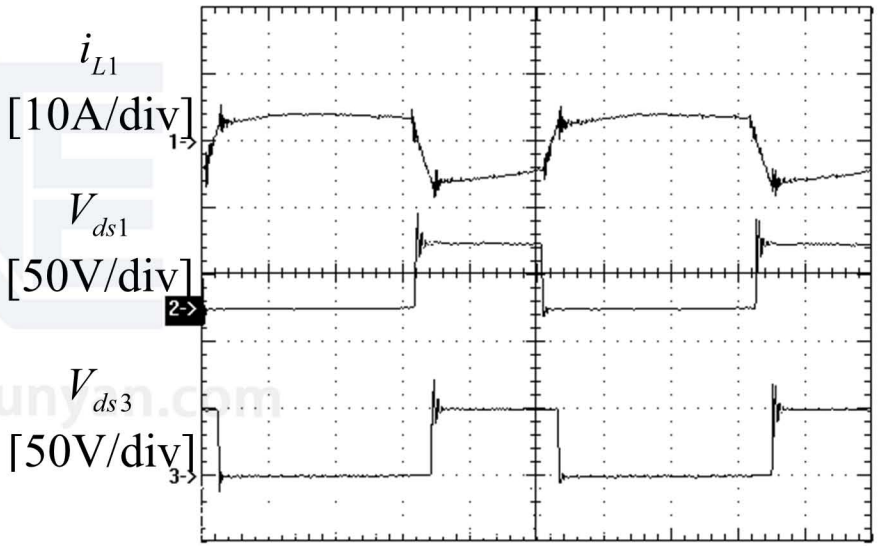
PPS control

Experiment (3/5)

Output voltage : 30V, output power :100W



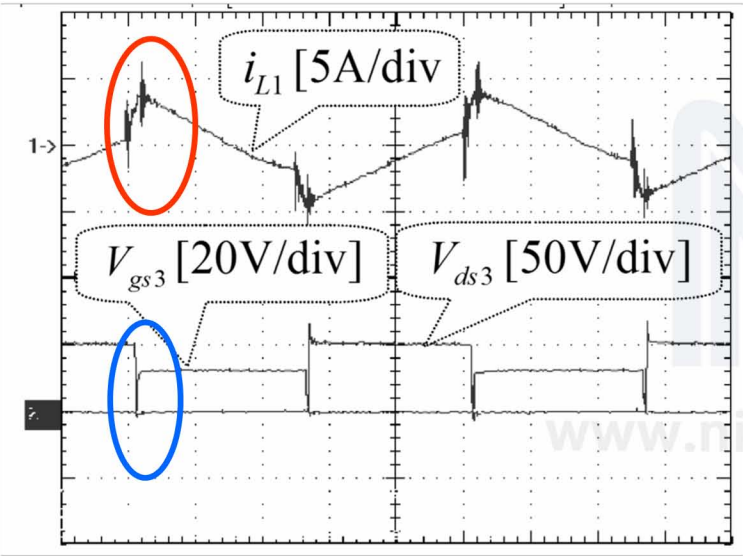
PS control



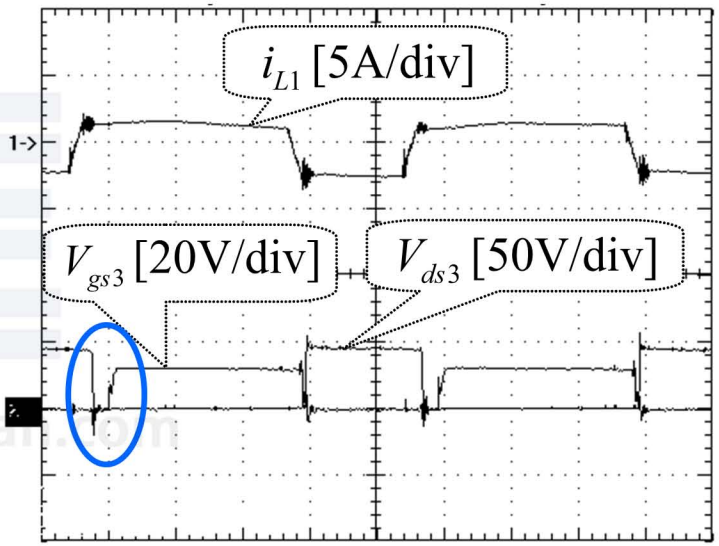
PPS control

Experiment (4/5)

Output voltage : 30V, output power :30W



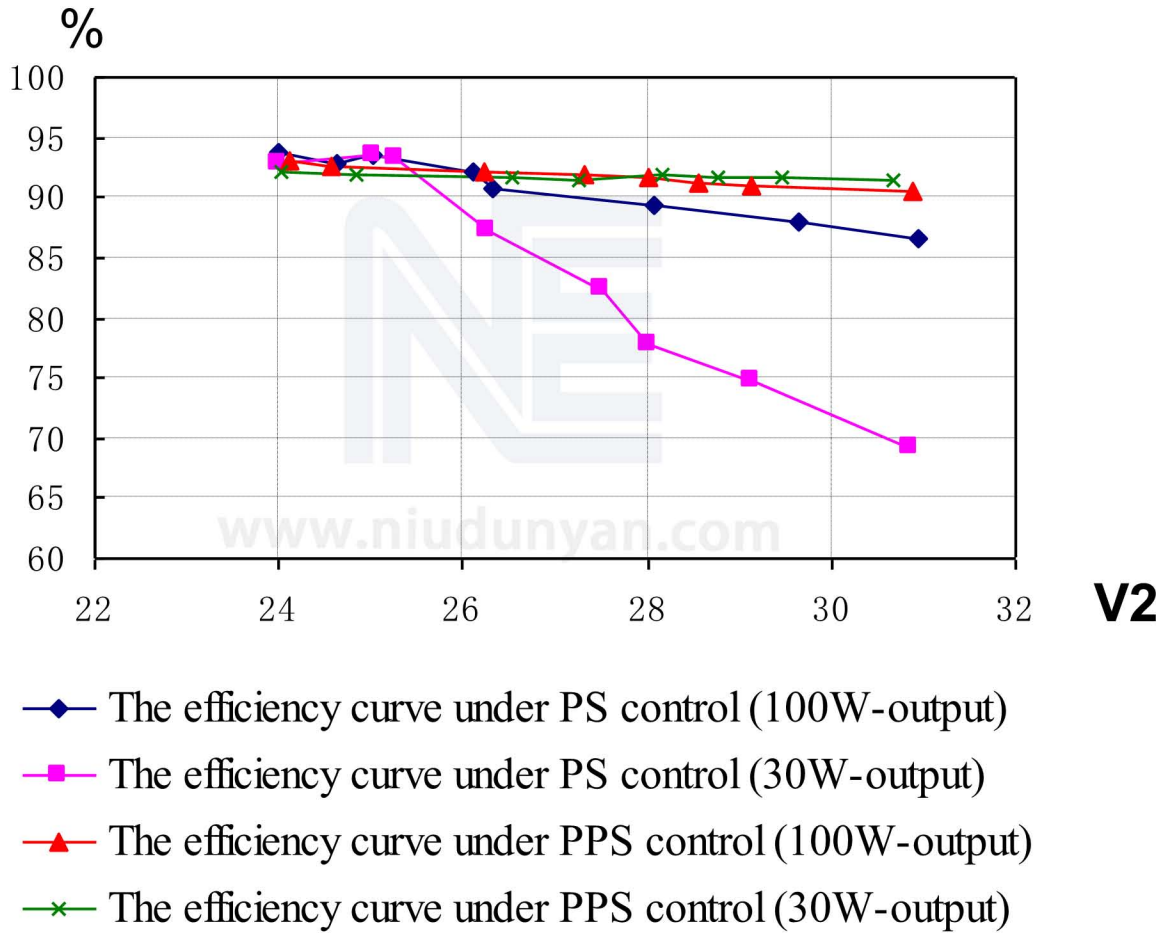
PS control



PPS control

Experiment (5/5)

Efficiency comparison between PS and PPS



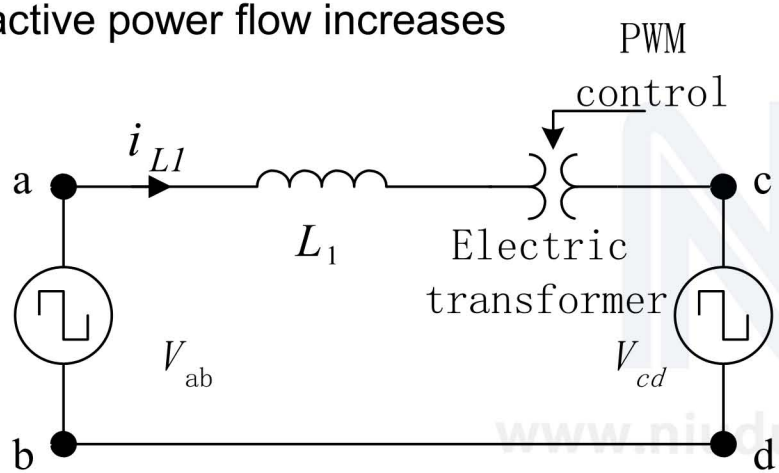
Discussion

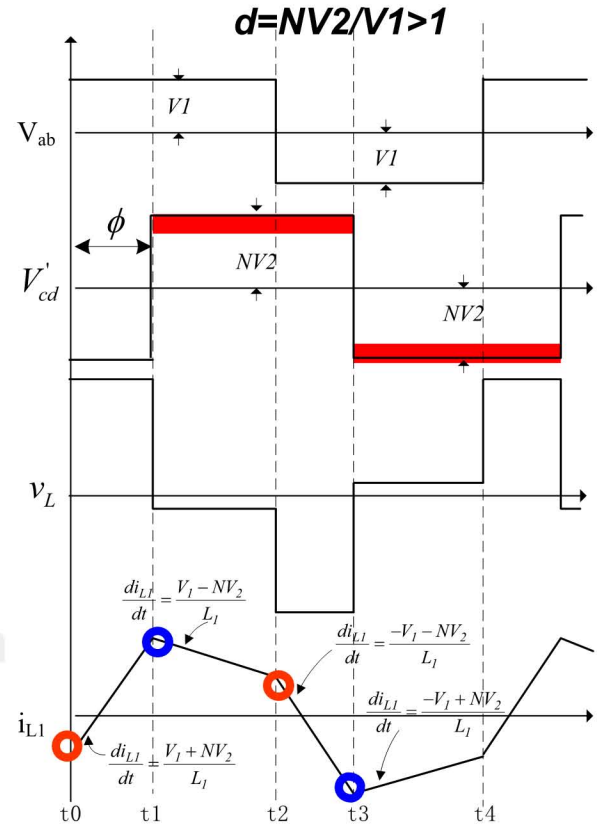
- With PPS control, inductor current peak is reduced
- Both switching loss and conduction loss is reduced
- Current stress of the switches are reduced
- A larger ZVS range is obtained

Concept of PPS control

- High current stresses and narrow ZVS range in unmatched input and output

Reason of the problem: the amplitude of input voltage is not matched with that of output voltage. Reactive power flow increases



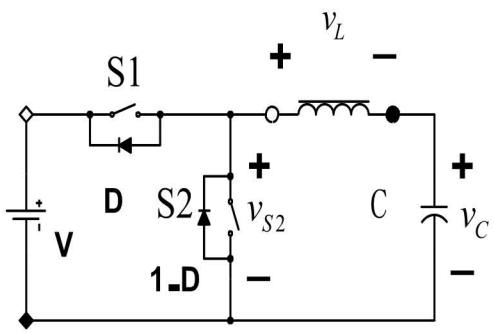


Waveforms of PS control

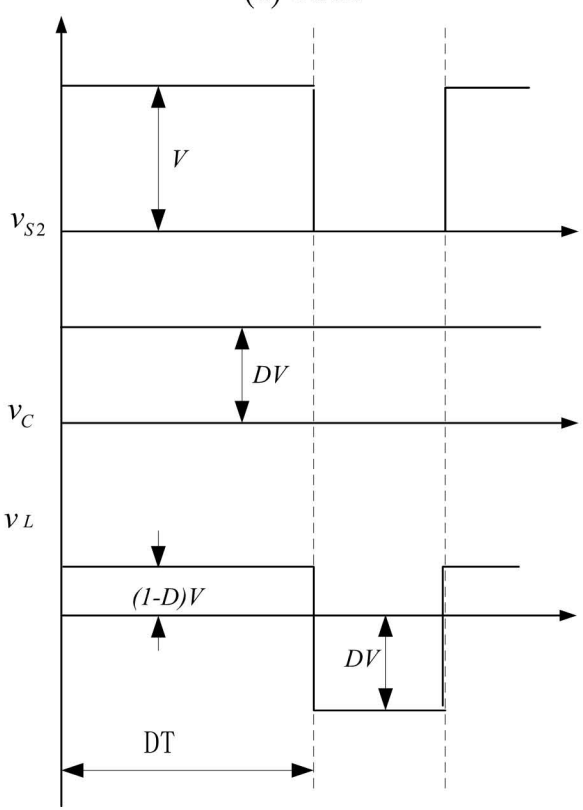
PPS control:

- Duty cycle is varied so that both positive and negative amplitudes of the equivalent input voltage (V_{ab}) can always be equal to those of the equivalent output voltage (V_{cd})

Switch cell under duty cycle control



(a) buck



- In the steady state, output DC voltage of buck converter $v_c = DV$
- Inductor voltage is square with amplitudes depending on duty cycle

$$v_L = v_{S2} - v_C$$

v_L positive amplitude $\quad v_{L+pk} = f(D,V) = (1-D)V$

v_L negative amplitude $\quad v_{L-pk} = g(D,V) = -DV$

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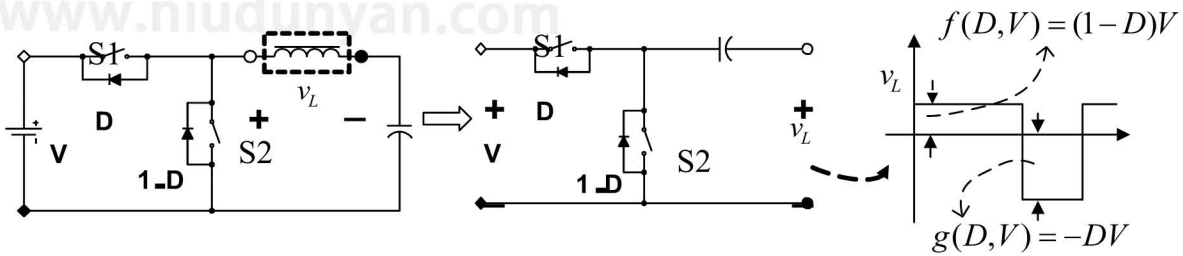
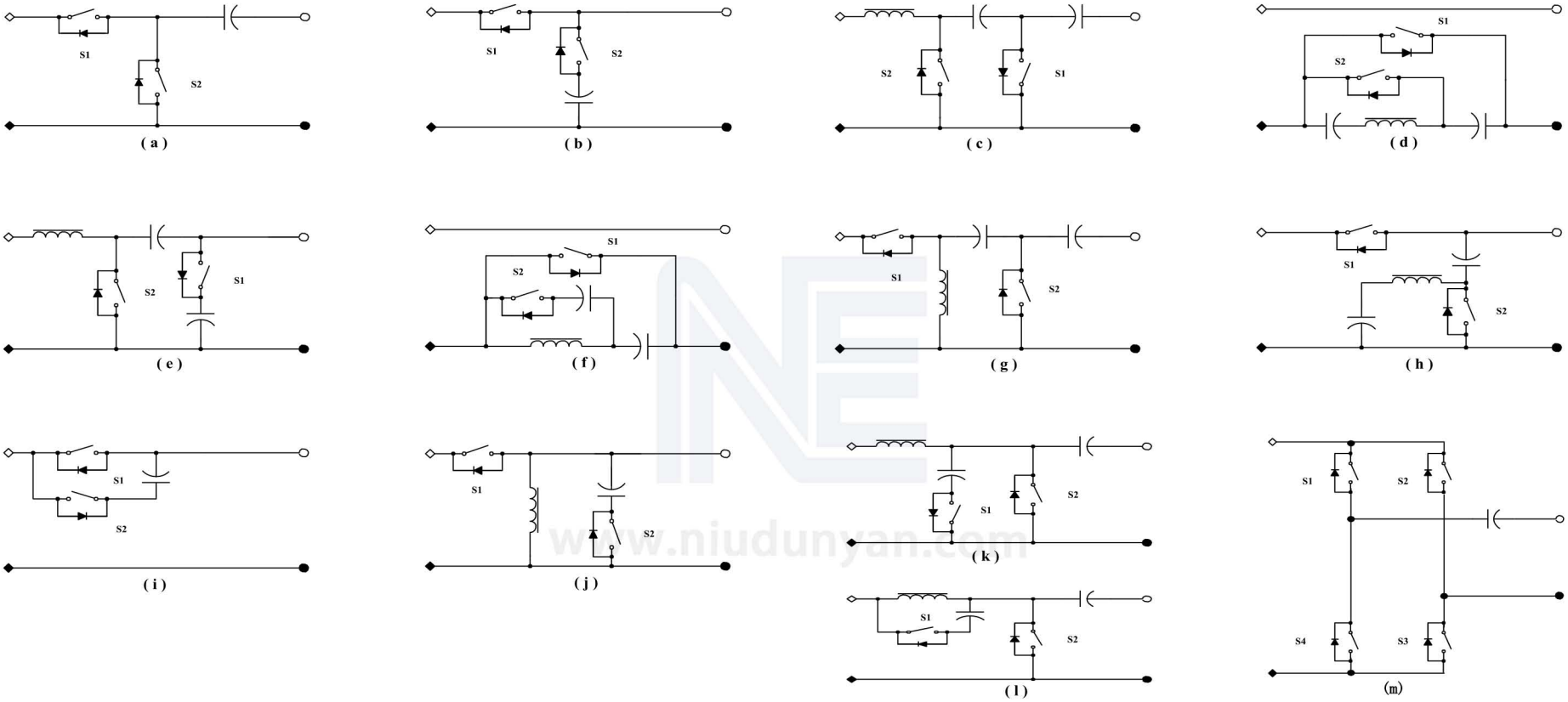


- With duty cycle control, the switch cell output amplitude can be adjusted
- Averaged value of the switch cell output is equal to 0

$$\langle v_L \rangle_T = \frac{1}{T}\int_0^T v_L(t)dt = Df(D,V) + (1-D)g(D,V) = 0$$

Switch Cells



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Classification of switch cells

- Group A switch cell (a), (m)

$$v_{L+pk} = f(D,V) = k_a(1-D)V \qquad v_{L-pk} = g(\mathrm{D},V) = k_a DV$$

- Group B switch cell (b), (c), (d), (f), (g), (h), (i), (j)

$$v_{L+pk} = f(D,V) = k_b V \qquad v_{L-pk} = g(D,V) = k_b DV/(1-D)$$

- Group C switch cell (e), (k), (l)

$$v_{L+pk} = f(D,V) = k_c(1-D)V/D \qquad v_{L-pk} = g(D,V) = k_c V$$

ka=kb=kc=1 except switch cell (m)
*ka=2 f*or switch cell (m),

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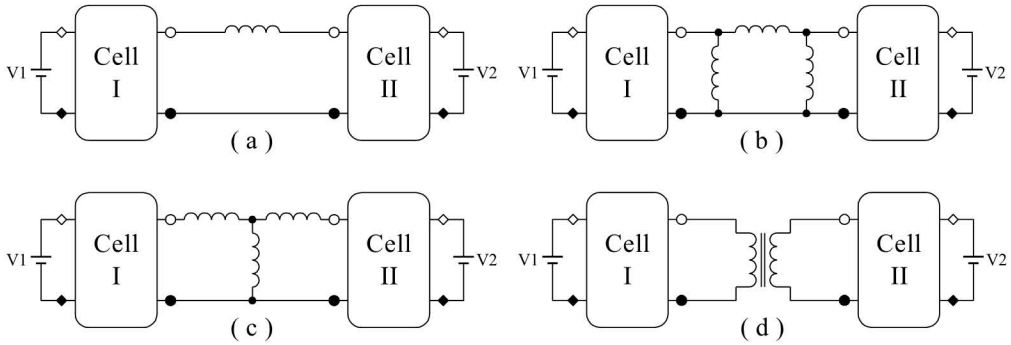
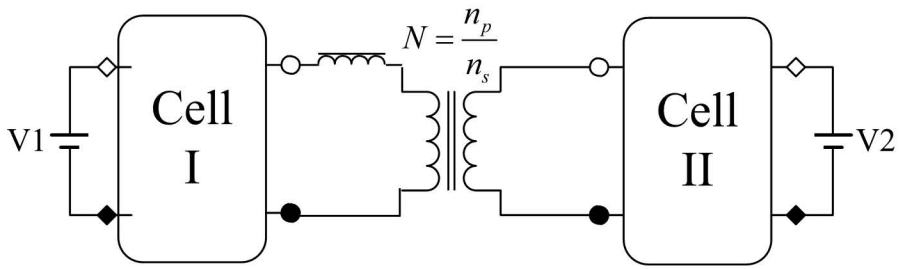
Build bi-dc/dc converter with two switch cells



Requirement to PPS control



For switch cell *I*, positive amplitude $f_{\mathrm{I}}(\mathrm{D},\mathrm{V}_1)$, negative amplitude $g_{\mathrm{I}}(\mathrm{D},V_1)$

For switch cell *II*, positive amplitude $f_{\mathrm{II}}(\mathrm{D},\mathrm{V}_2)$, negative amplitude $g_{\mathrm{II}}(\mathrm{D},V_2)$

Since averaged value of the switch cell is equal to zero, following equations are obtained

$$\begin{cases} Df_{\mathrm{I}}(\mathrm{D},V_1)-(1-D)g_{\mathrm{I}}(\mathrm{D},V_1)=0 \\ Df_{\mathrm{II}}(\mathrm{D},V_2)-(1-D)g_{\mathrm{II}}(\mathrm{D},V_2)=0 \end{cases} \Rightarrow \frac{f_{\mathrm{I}}(\mathrm{D},V_1)}{f_{\mathrm{II}}(\mathrm{D},V_2)}=\frac{g_{\mathrm{I}}(\mathrm{D},V_1)}{g_{\mathrm{II}}(\mathrm{D},V_2)}$$

PPS requires that the positive amplitude of the square sources in two sides are matched, therefore

$$f_{\mathrm{I}}(\mathrm{D},\mathrm{V}_1)=Nf_{\mathrm{II}}(\mathrm{D},\mathrm{V}_2)$$

By using zero averaged value of the switch cell output condition, $g_{\mathrm{I}}(\mathrm{D},\mathrm{V}_1)=Ng_{\mathrm{II}}(\mathrm{D},\mathrm{V}_2)$

- If the positive amplitude of the square sources in two sides are matched, then the negative amplitude of these two square sources are automatically matched

Derivation of duty cycle for PPS

Assumption: switch cell *I* is from Group A

$$f_{\mathrm{I}}\left(\mathrm{D},\mathrm{V}_1\right)=k_a(1-D)V_1$$

Assumption: switch cell *II* is from Group C

$$f_{\mathrm{II}}\left(\mathrm{D},\mathrm{V}_2\right)=k_c(1-D)V_2/D$$

PPS requires that the positive amplitude of both square sources are matched, therefore

$$f_{\mathrm{I}}\left(\mathrm{D},\mathrm{V}_1\right)=Nf_{\mathrm{II}}\left(\mathrm{D},\mathrm{V}_2\right)$$

Then $k_a(1-D)V_1=Nk_c(1-D)V_2/D$ $\Rightarrow$ $D=N\dfrac{k_cV_2}{k_aV_1}$

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Duty cycle

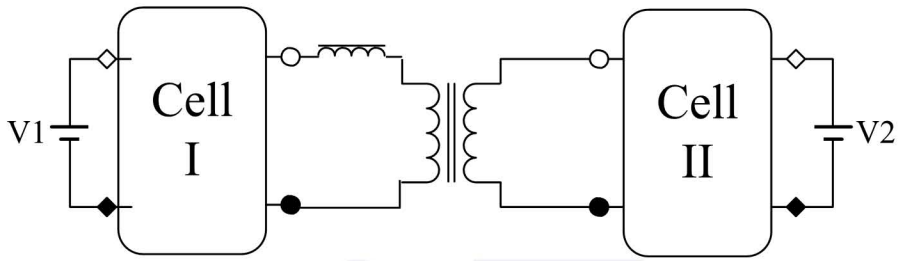
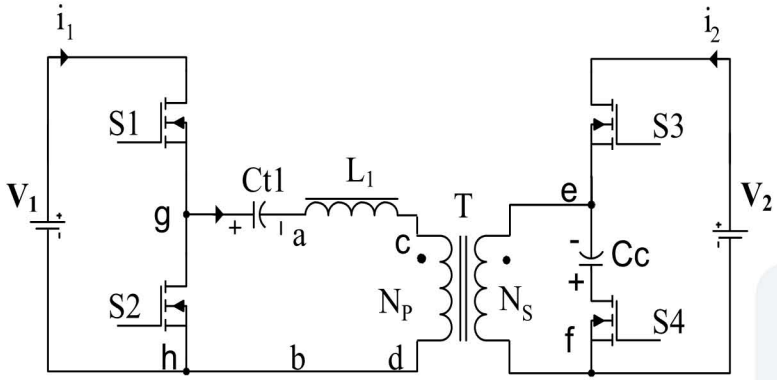


TABLE Value of duty ratio D

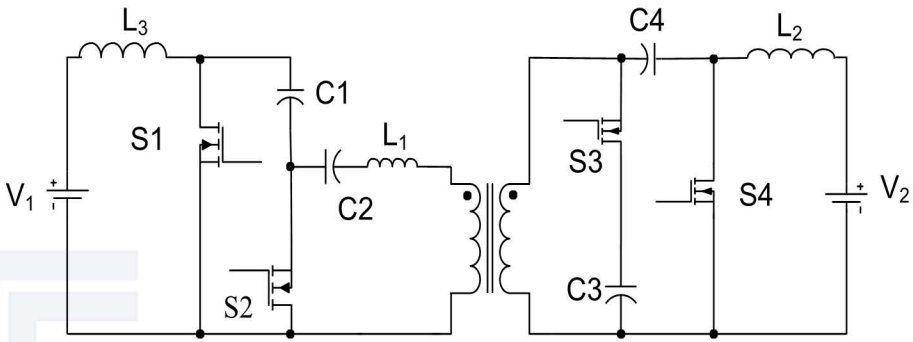
Switch Cell II / D / Switch Cell I	A	B	C
A	No	$\frac{k_aV_2-Nk_bV_1}{k_aV_2}$	$\frac{Nk_cV_2}{k_aV_1}$
B	$\frac{Nk_aV_2-k_bV_1}{Nk_aV_2}$	No	$\frac{Nk_cV_2}{k_bV_1+Nk_cV_2}$
C	$\frac{k_cV_1}{Nk_aV_2}$	$\frac{k_cV_2}{Nk_bV_1+k_cV_2}$	No

- **Two switch cells belonging to different groups can be used to build a PPS controlled bidirectional DC-DC converter**

Examples



switch cell （a) of group A + switch cell (b) of group B



switch cell (c) of group B + switch cell (e) of group C

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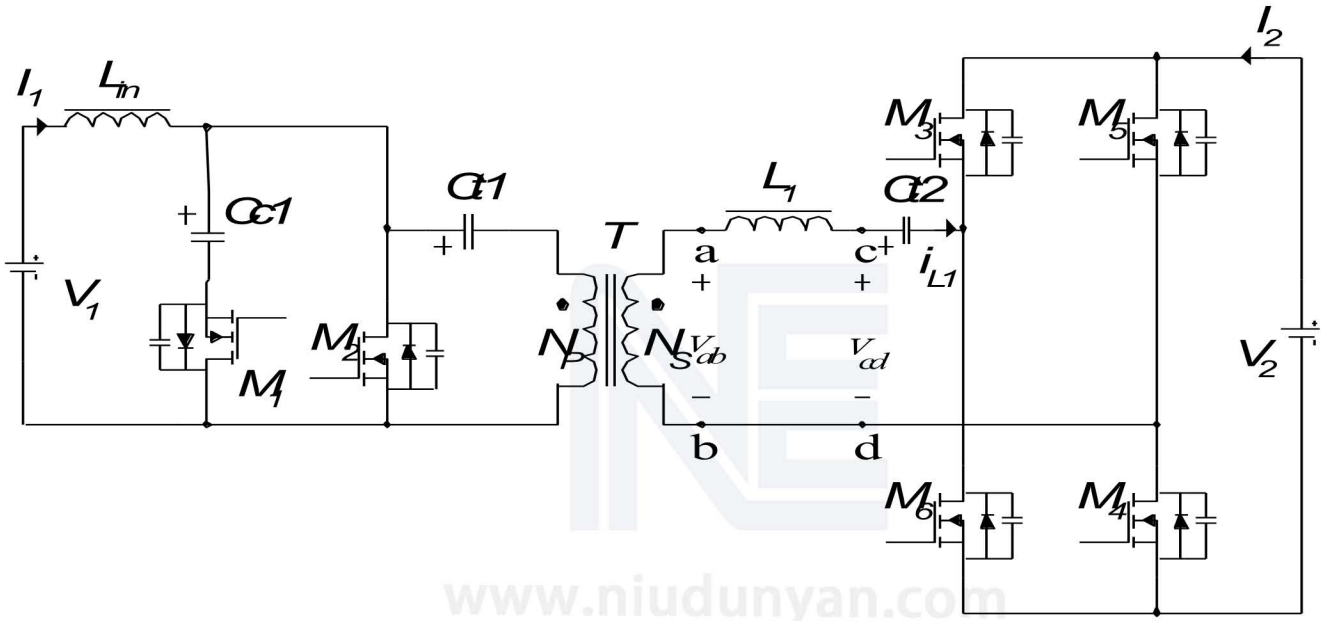
Examples



switch cell (k) of group C + switch cell (m) of group A

Summary

- A technique to synthesize PWM plus phase-shift bi-directional DC-DC converters topologies is presented
- Switch cells are classified into 3 groups. Switch cell in different group can be combined to build a bi-DC/DC converter with PPS control
- With PSS control, inductor current peak is reduced and switch loss is reduced.
- ZVS range is extended

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Chapter 5
DAB Converter with Resonant Tank

Outline

- Problem of DAB converter with phase-shift control
- SRC with cascade buck/boost converter
- DAB with series resonant tank
- DAB with high-order resonant tank: CLLC converter
- Summary

DAB converter with phase-shift control

Advantages

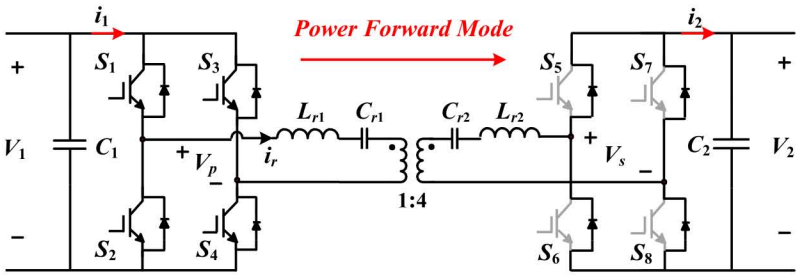
- Bidirectional power flow with buck-boost capability
- Simple to control
- Fixed-frequency operation
- Zero voltage switching(ZVS) for all switches in matched input and output
- Leakage inductances of the transformer is used

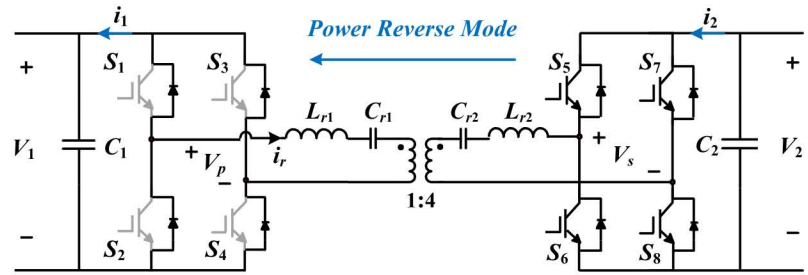
Problems

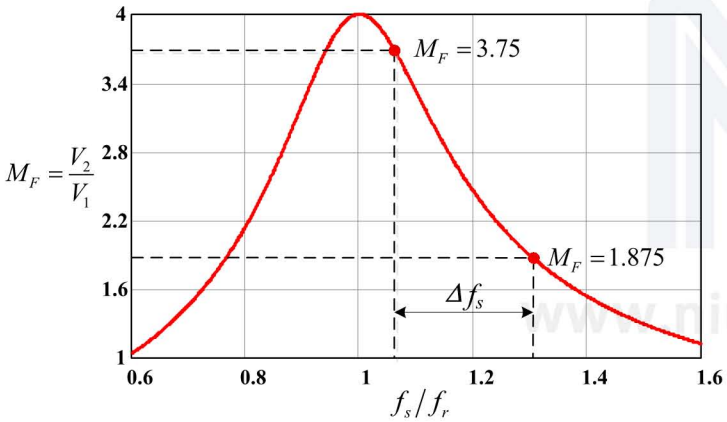
- Higher switch turn-off loss due to turn-off of highest inductor current in a switching period
- Very long current loop through 4 switches and 2 DC side capacitors in the inductor charging state(required to boost voltage)
- When d deviates from 1, inductor current change from trapezoidal to triangle alike waveform
- When d deviates from 1, higher RMS current in the inductor tank and higher loss in the inductor, and higher turn-off switch loss
- ZVS condition become difficult to realize when d deviates from 1 in light load
- 8 switch turn-on and turn-off actions in a switch period(tentative to be ZVS-on and ZVS off)

SRC with uncontrolled rectifier

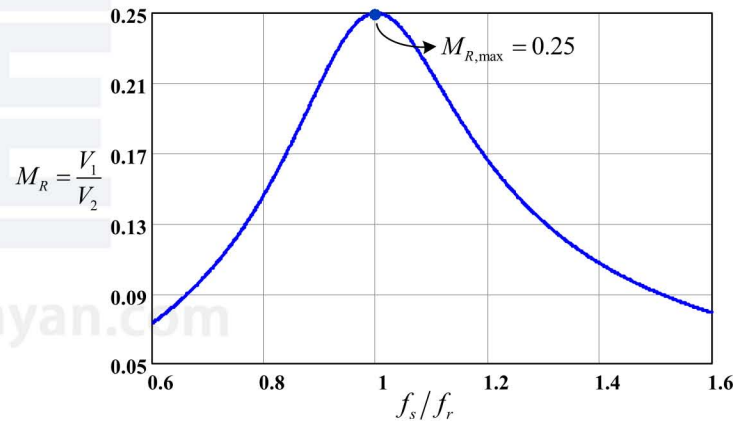
- SRC has high efficiency and high power density with operating near the resonant frequency







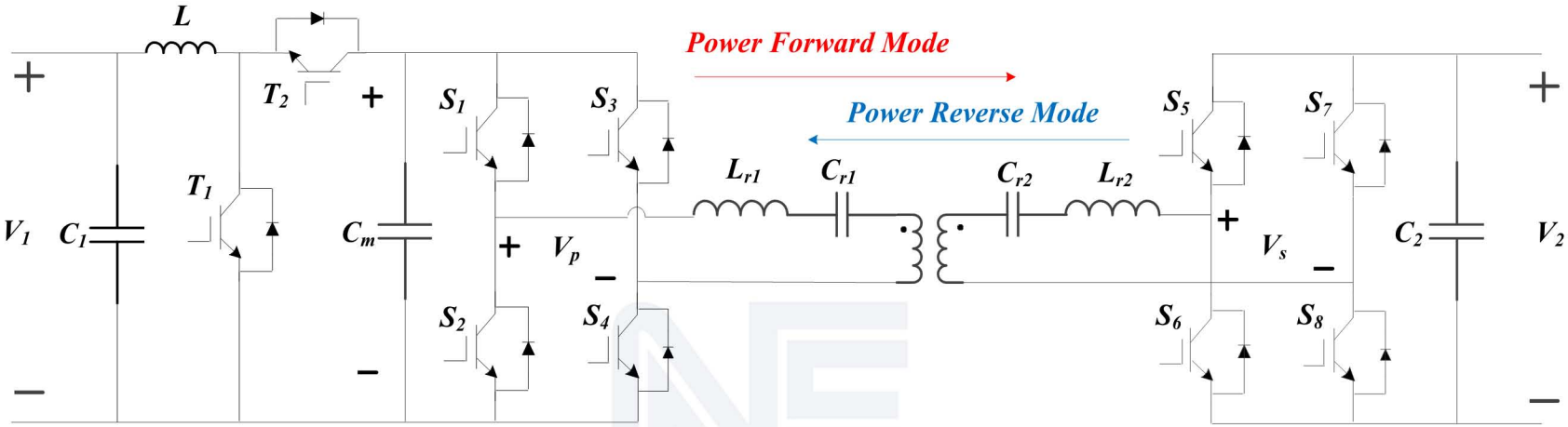
- Gain vs. frequency at forward mode



- Gain vs. frequency at backward mode

SRC has only buck ability

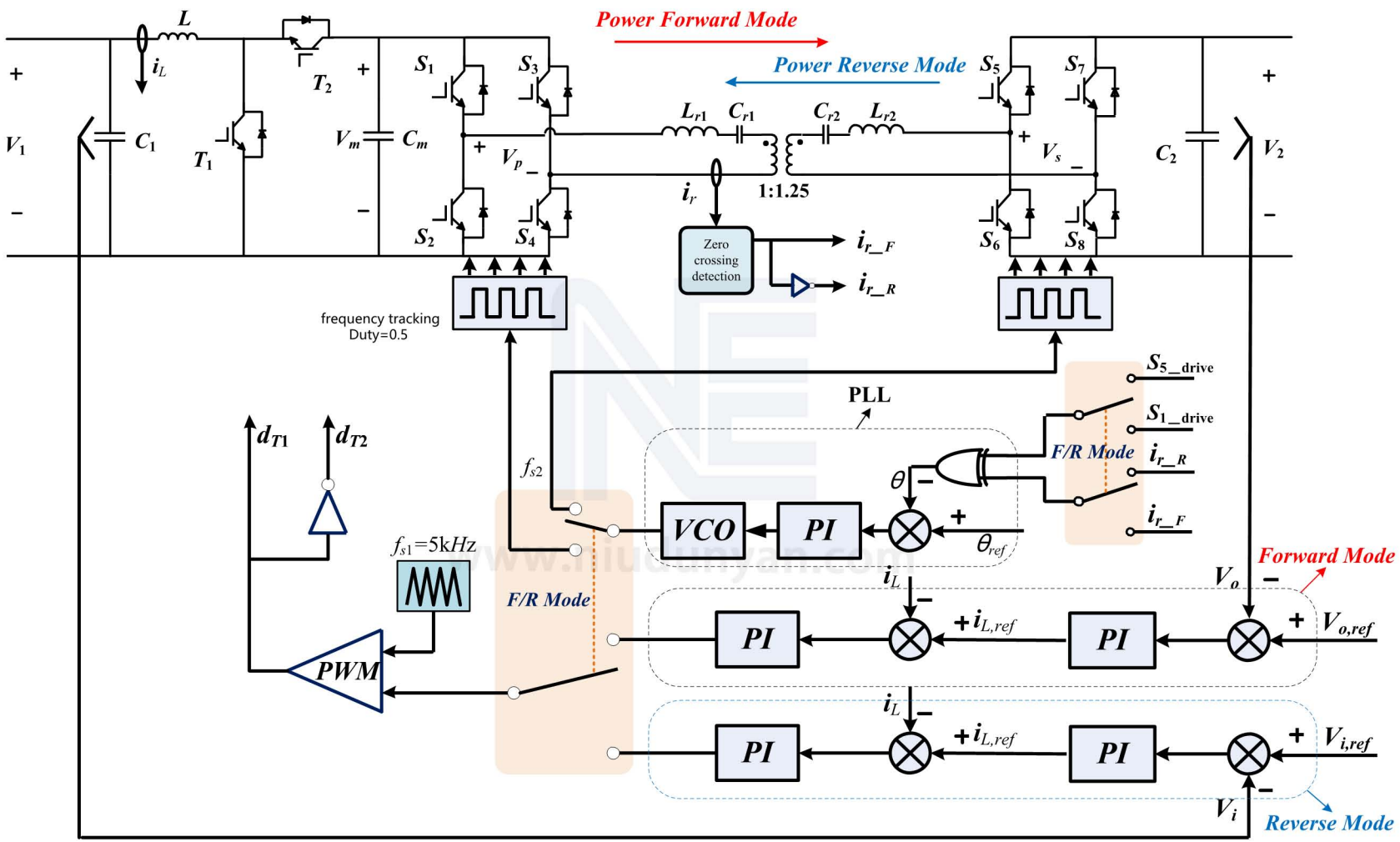
SRC with front-end buck/boost converter



- First stage: Boost/Buck converter with duty cycle control
- Second stage: SRC with variable frequency control to keep almost unit power factor
- Wide gain range in both directions
- ZVS is realized for the 2nd stage and smaller isolation transformer
- First stage is hard switching

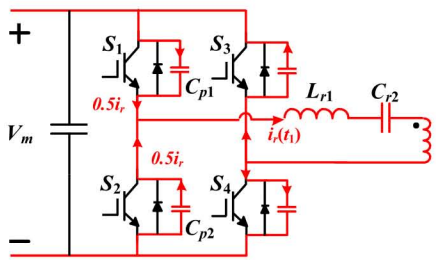
@F. Krismer, J. Biela, J. W. Kolar, *IEEE IAS*, 2005
@Qicheng Huang, Dehong Xu etal,IEEE ECCE, 2014

Control of SRC with front-end buck/boost converter

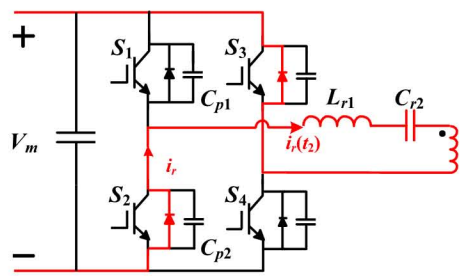


- PLL keeps the power factor angle θ tracking its reference $\theta_{ref.}$
- Input or output voltage/current are adjusted through duty cycle control of Buck/Boost converter

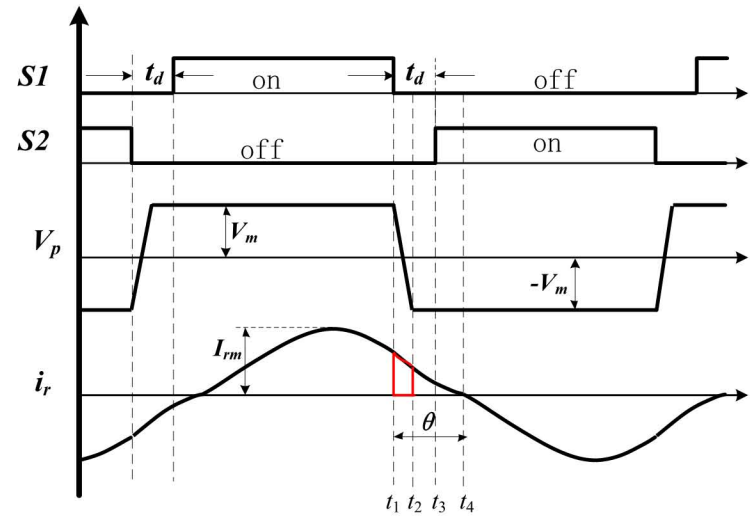
Design of power factor angle to realize ZVS



$[t_1, t_2]$, cap discharging



$[t_2, t_3]$, S2 and S3 diode conducting



To realize ZVS turn-on of S2, S3, following inequality needs to satisfied

$$\int_{\theta/\omega_s - t_d}^{\theta/\omega_s} \frac{1}{2} I_{rm} \sin(\omega_s t)\, dt \geq C_p V_m$$

$$\theta > \frac{2C_p V_m}{I_{rm} t_d} + \pi f_s t_d$$

$$I_{rm} = \frac{4V_m}{\pi} / (N^2 R_{eq}) \qquad R_{eq} = \frac{8}{\pi^2} \frac{V_2^2}{P_o}$$

$$\theta > \frac{4N^2 C_p V_2^2}{\pi P_o t_d} + \pi f_s t_d$$

Current lag time is required to longer than dead time td so that antiparallel diode of the switch keeps conducting before the switch turn-on gate signal

$$\theta \geq 2\pi f_s t_d$$

Combining two inequality, we get current lag angle to satisfy ZVS condition

$$\theta \geq \max\left\{ \frac{4N^2 C_p V_2^2}{\pi P_o t_d} + \pi f_s t_d, 2\pi f_s t_d \right\}$$

Parameters of the Prototype

5kW SRC with front-end buck/boost converter

Parameter	Value	Parameter	Value
Rated power P_o	5kW	L	1.1mH
Input V_1	200~400V	$L_{r1}=L_{r2}$	192μH
Output V_2	500V	$C_{r1}=C_{r2}$	0.33μF
Switching frequency for buck/boost coverter f_{s1}	5kHz	C_1	220μF
Resonant frequency f_r	20kHz	C_m	440μF
N_p:N_s	1:1.25	C_2	200μF
SRC sw. freq. lower limit $f_{s2_down,limit}$	20kHz	C_p	180pF
SRC sw. freq. upper limit $f_{s2_up,limit}$	30kHz	Q	1.5
IGBT	Infineon K40H1203	Controller	DSP

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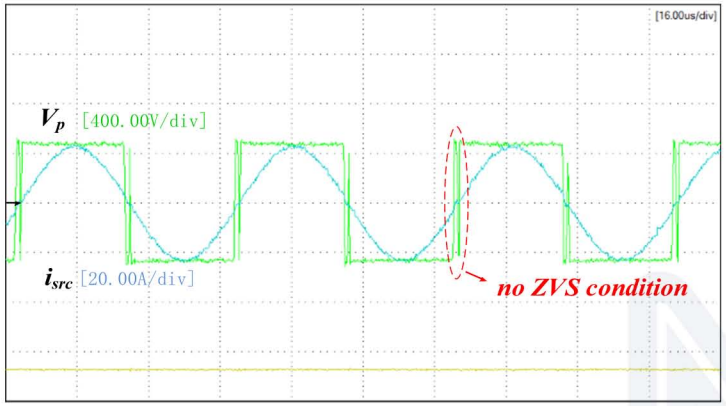
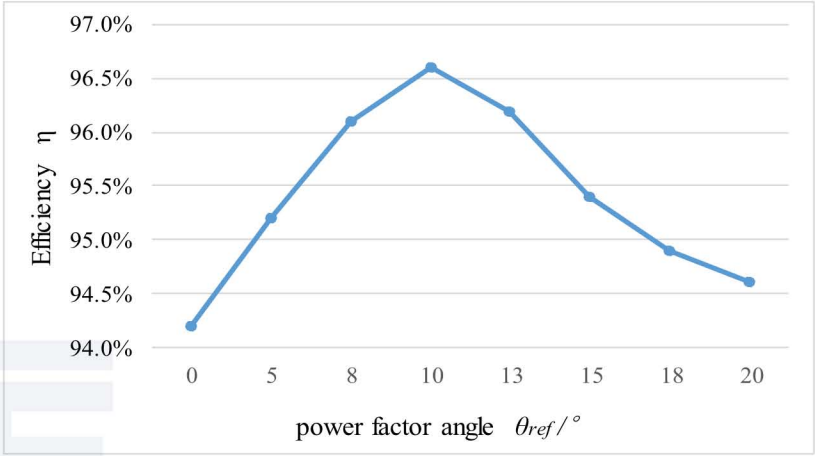
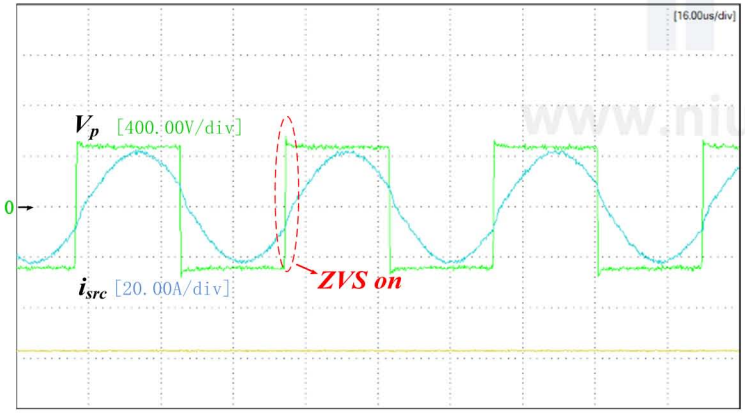
Experiment results with different θ_{ref}



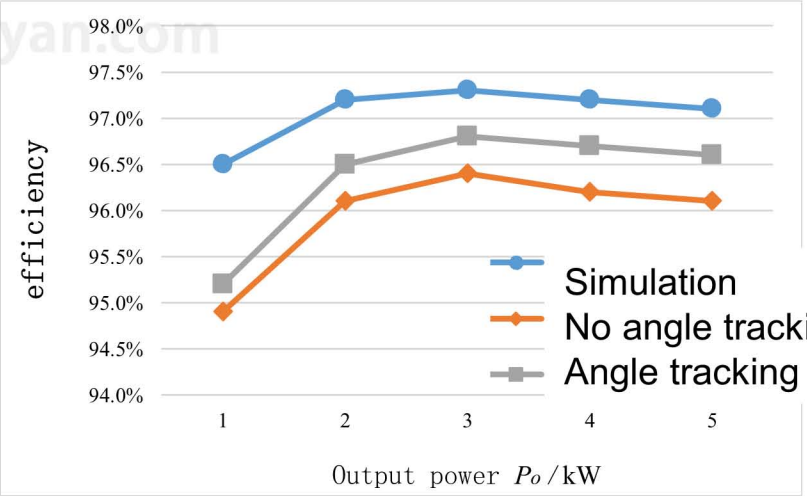
● θ_{ref} =5° (Forward Mode)



Measured efficiency under different θ_{ref}
(P_o = 5kW, Power Forward Mode)



● θ_{ref} =10° (Forward Mode)



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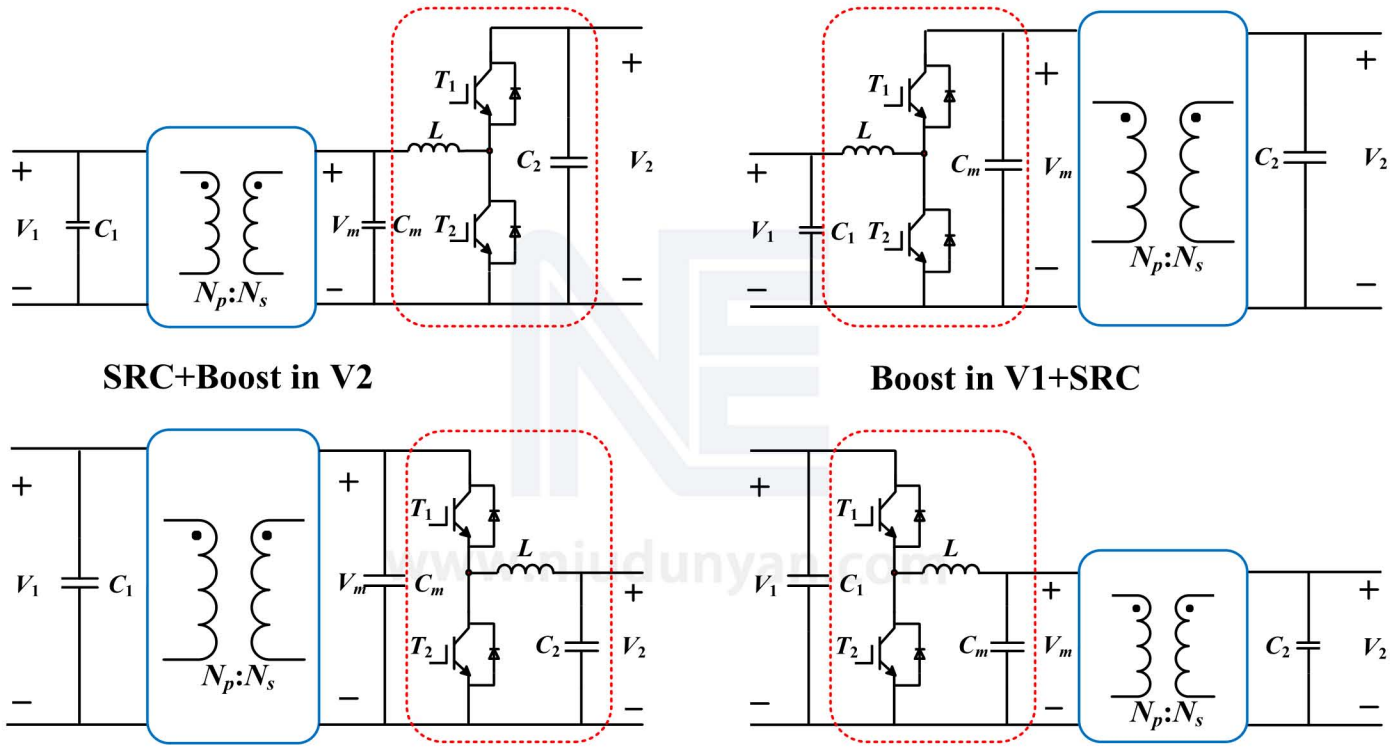
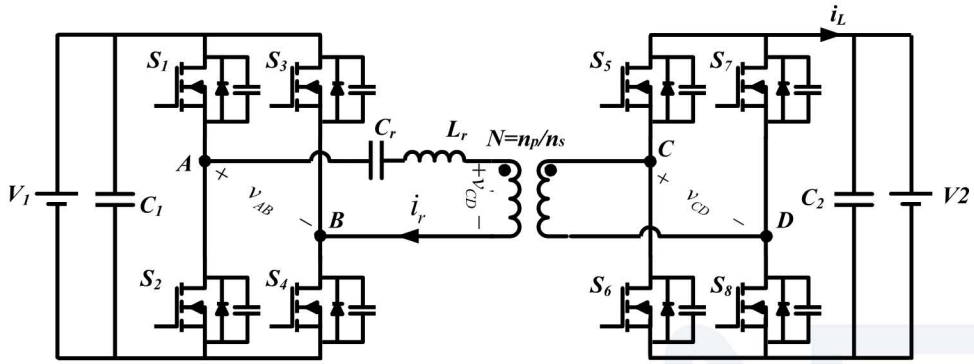
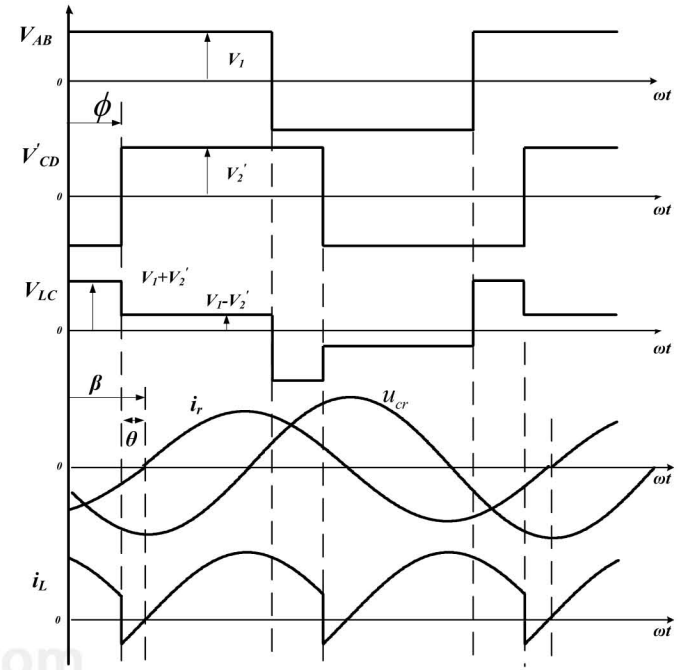
SRC with cascaded buck/boost converter



- SRC is preferred to operate at unit power factor
- Selection of topology depends on the voltage level and variation of input and output voltages

DAB with Series Resonant Tank(DABSRT)





Power vs. Phase shift

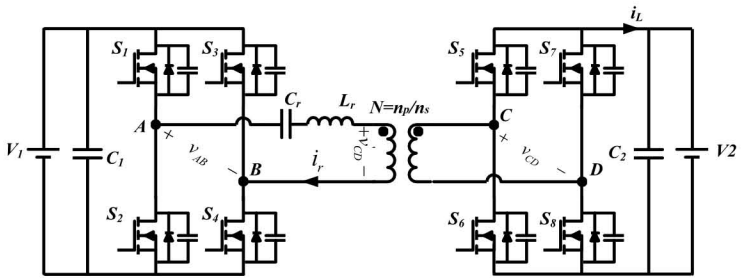
$$P_{o,pu} = \frac{8d}{\pi^2 Q(f_n - 1/f_n)} \sin\phi$$

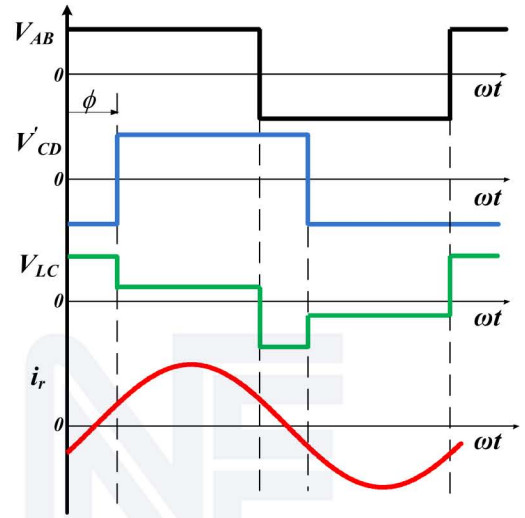
$$d = \frac{NV_2}{V_1}, Q = \frac{\omega_r L_s}{R_{eq}}, f_n = \frac{f_s}{f_r}, R_{eq} = N^2 \frac{V_o^2}{P_o}$$

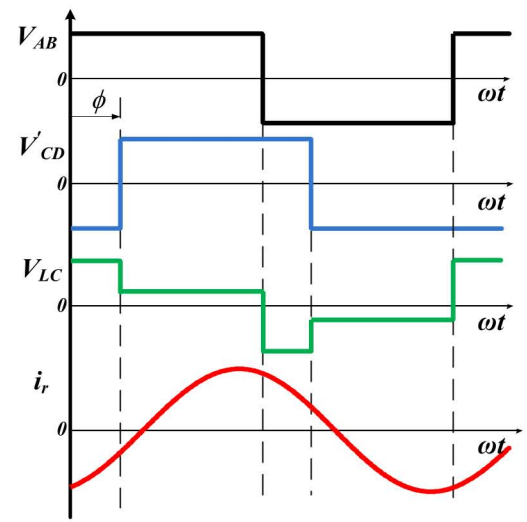
- Combining phase-shift control with frequency control
- Shape the tank waveform into sinusoidal
- ZVS obtained with wide input/output voltage variation
- No transformer saturation due to series capacitor
- Variable switching frequency to minimize power factor angle to maximize the converter efficiency

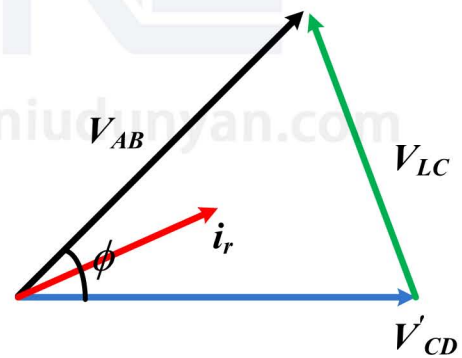
@Xiaodong Li, Ashoka K. S. Bhat, IEEE trans. PE, 2010

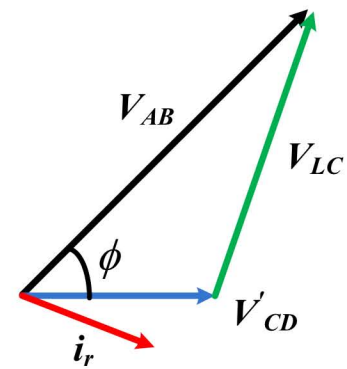
Soft-switching condition











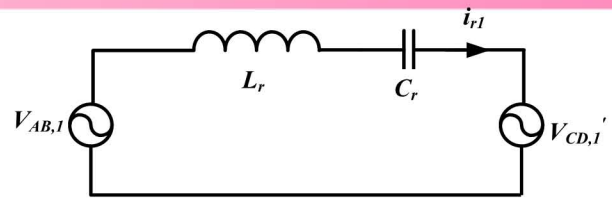
- ZVS for both primary and secondary converter
- ZVS for both primary and ZCS for secondary converter

Soft switching condition is decided by phasor i_r positon with respect to phasor V_{AB} and V_{CD}'

@M. Yaqoob, K. H. Loo, IEEE trans. PE, 2017

ZVS for both primary and secondary

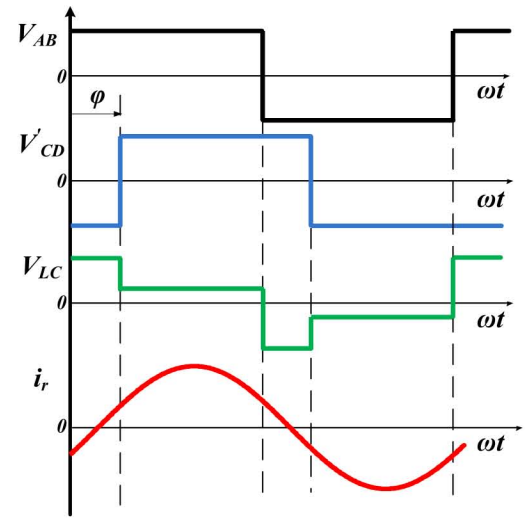
Assumption: fundamental harmonic component analysis method is used



$$V_{AB,1}(t) = \frac{4V_1}{\pi}\sin\omega_s t \qquad V_{CD,1}'(t) = \frac{4dV_1}{\pi}\sin(\omega_s t - \phi)$$

Fundamental component of *ir* $\quad i_{r1}(t) = \frac{4V_1}{\pi X}\left[d\cos(\omega_s t - \phi) - \cos\omega_s t\right]$

where $\quad d = \frac{NV_2}{V_1}, X = \omega L_r - \frac{1}{\omega C_r}$



- For ZVS of primary converter

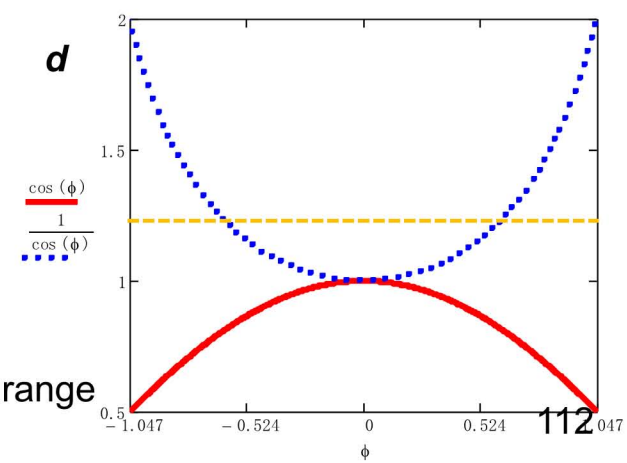
$$i_r(0) = \frac{4V_1}{\pi X}(d\cos\phi - 1) < 0 \quad \Rightarrow \quad d < \frac{1}{\cos\phi}$$

- For ZVS of secondary converter

$$i_r\left(\frac{\phi}{\omega_s}\right) = \frac{4V_p}{\pi X}(d - \cos\phi) > 0 \quad \Rightarrow \quad \cos\varphi < d$$

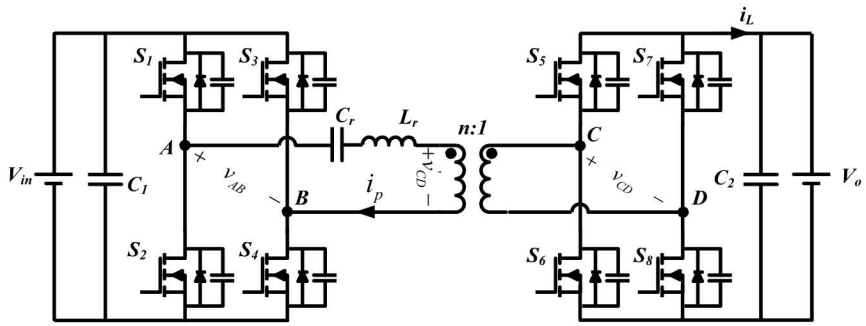
To realize ZVS for both primary and secondary converters

$$\cos\phi < d < \frac{1}{\cos\phi}$$

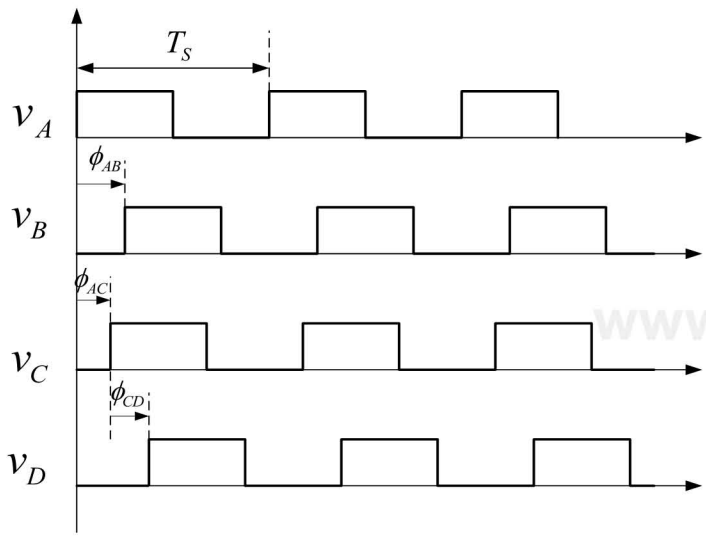


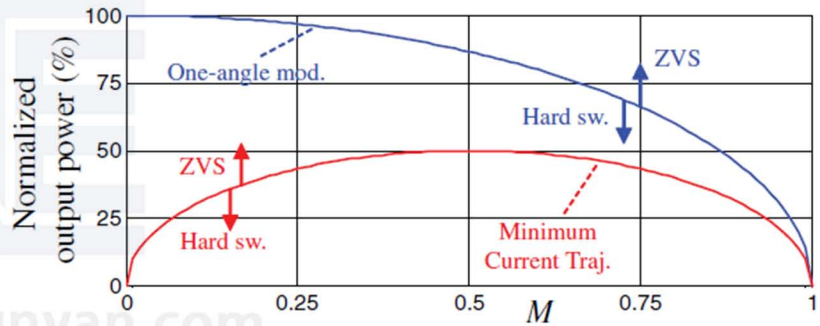
- Phase shift needs to increase to realize ZVS in a large gain range

DABSRT with 3D phase-angle control



$$P_o = P_{o,\max} \sin(\frac{\phi_{AB}}{2}) \sin(\frac{\phi_{CD}}{2}) \sin(\phi_{AC} + \frac{\phi_{CD} - \phi_{AB}}{2})$$



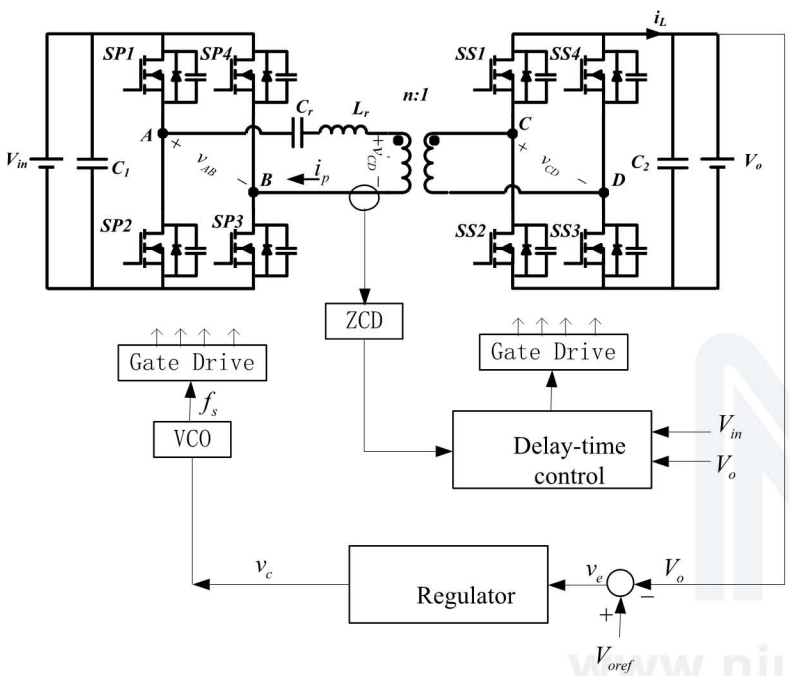


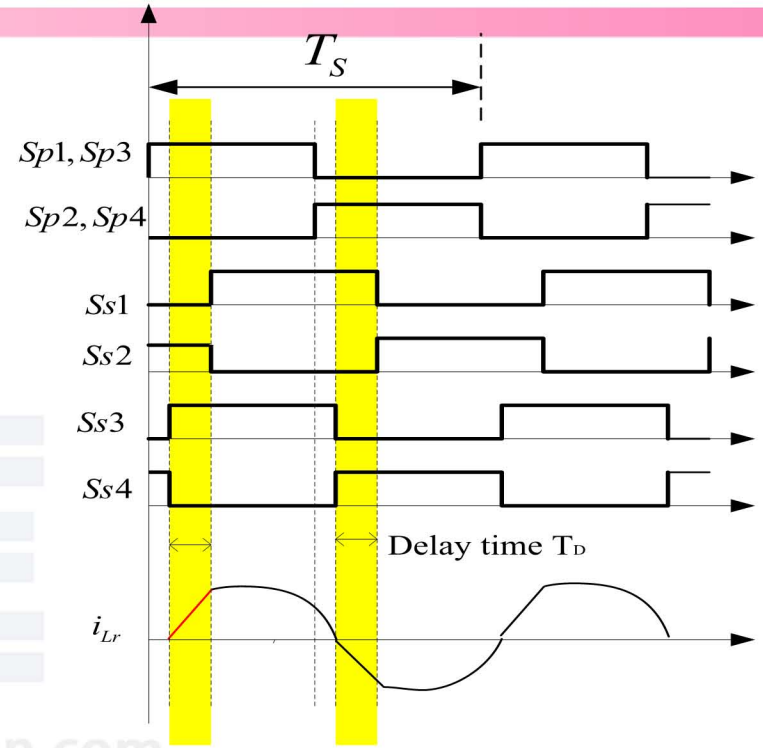
3D phase control vs. one angle control for ZVS boundary for the input bridge in M<1 case

- More freedoms to reduce circulating current in the resonant tank
- Soft switching range in light load is extended
- Improve efficiency at light load

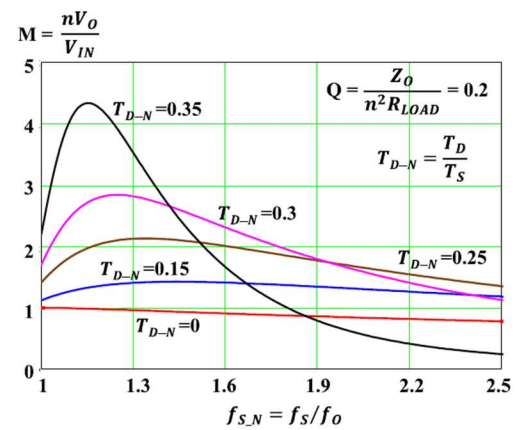
Luca Corradini, Dragan Maksimovic, *etal, IEEE trans PE, 2012*

DABSRT with frequency and delay-time control





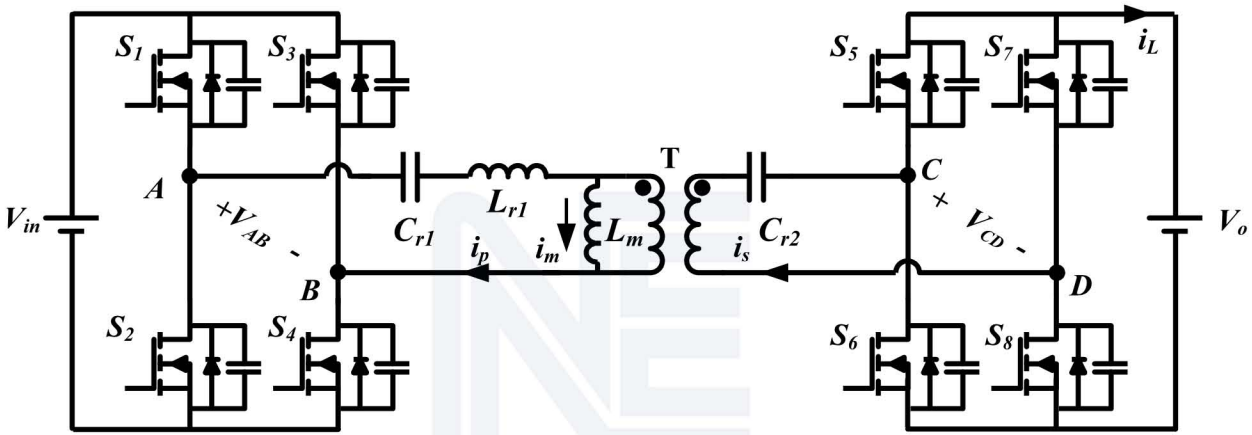
- Buck-boost function
- Reduced current loop during boost stage
- Combining variable-frequency and delay-time control: Variable frequency control in the primary and delay-time control in the secondary-side
- Compressed switching-frequency-range
- ZVS is realized



@Gang Liu, Yungtaek Jang, Milan M. Jovanovic, and Jian Qiu Zhang, IEEE trans. PE, 2017
@Y. Jang, M. M. Jovanovi´c, J. M. Ruiz, and G. Liu,. *IEEE APEC*.2015

DAB with High Order Resonant Tank(DABHORT)

CLLC resonant Converter



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- Extra C is added to LLC converter
- In forward mode, the secondary become rectifier
- In backward mode, the primary side is rectifier
- Heritage the partial feature of LLC converter
- Design of CLLC tank is difficult to cover wide range variation of the gain

@Wei Chen, Ping Rong, and Zhengyu Lu, IEEE Trans IE, 2010

Summary

- SRC with cascaded buck/boost converter optimize the total system with paying circuit complexity
- DAB with Series resonance tank introduces frequency freedom to original phase shift control. With current shaping and combination of frequency and phase shift control, it is helpful to further extend soft switching range, reduce circulation current. However its control becomes complex. Besides it still exist a long current loop in boost stage which is inherited from traditional DAB
- DABSRT with frequency and delay-time control reduces the current loop during boost stage which cuts down circulation current loss

Tutorial Summary

- Although concept of DAB with phase-shift control is very simple, realization has met difficult. Its challenge comes from efficiency decline due to unmatched input and output condition
- PWM+phase-shift(PPS), trapezoidal modulation etc. occur to try to optimizing the inductor current profile
- DAB with resonant tank is used to shape the tank current profile into sinusoidal and leverage both phase-shift(duty cycle control) and frequency control
- Further studies are needed about control and design of DAB converters

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Thanks for your attention

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