

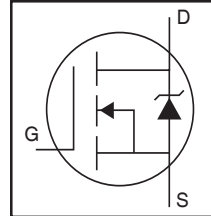
# IRFR4510PbF

# IRFU4510PbF

HEXFET® Power MOSFET

### Applications

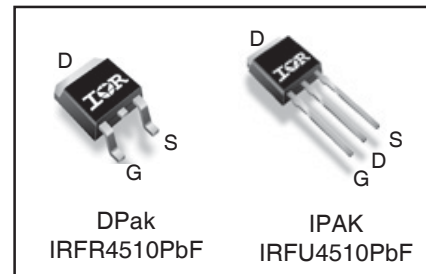
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits



<b>V<sub>DSS</sub></b>	<b>100V</b>
<b>R<sub>DS(on)</sub> typ. max.</b>	<b>11.1mΩ</b>
	<b>13.9mΩ</b>
<b>I<sub>D</sub> (Silicon Limited)</b>	<b>63A</b>
<b>I<sub>D</sub> (Package Limited)</b>	<b>56A</b>

### Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

### Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	63	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Silicon Limited)	45	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V (Package Limited)	56	
I <sub>DM</sub>	Pulsed Drain Current ①	252	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Maximum Power Dissipation	143	W
	Linear Derating Factor	0.95	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	V
T <sub>J</sub> T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

### Avalanche Characteristics

E <sub>AS</sub> (Thermally limited)	Single Pulse Avalanche Energy ②	127	mJ
I <sub>AR</sub>	Avalanche Current ①	See Fig. 14, 15, 22a, 22b	A
E <sub>AR</sub>	Repetitive Avalanche Energy ①		mJ

### Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case ③	---	1.05	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (PCB Mount) ⑦	---	50	
R <sub>θJA</sub>	Junction-to-Ambient	---	110	

### ORDERING INFORMATION:

See detailed ordering and shipping information on the last page of this data sheet.

Notes ① through ⑧ are on page 11

www.irf.com

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

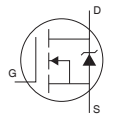
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	100	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.10	—	V/°C	Reference to 25°C, I <sub>D</sub> = 5mA <sup>①</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	11.1	13.9	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 38A <sup>④</sup>
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0	3.0	4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 100μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	20	μA	V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 100V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V
R <sub>G(int)</sub>	Internal Gate Resistance	—	0.61	—	Ω	

**Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	62	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 38A
Q <sub>g</sub>	Total Gate Charge	—	54	81	nC	I <sub>D</sub> = 38A
Q <sub>gs</sub>	Gate-to-Source Charge	—	14	—		V <sub>DS</sub> = 50V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	15	—		V <sub>GS</sub> = 10V <sup>④</sup>
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> - Q <sub>gd</sub> )	—	39	—		I <sub>D</sub> = 38A, V <sub>DS</sub> = 0V, V <sub>GS</sub> = 10V
t <sub>di(on)</sub>	Turn-On Delay Time	—	18	—	ns	V <sub>DD</sub> = 65V
t <sub>r</sub>	Rise Time	—	42	—		I <sub>D</sub> = 38A
t <sub>di(off)</sub>	Turn-Off Delay Time	—	42	—		R <sub>G</sub> = 7.5Ω
t <sub>f</sub>	Fall Time	—	34	—		V <sub>GS</sub> = 10V <sup>④</sup>
C <sub>iss</sub>	Input Capacitance	—	3031	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	213	—		V <sub>DS</sub> = 50V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	104	—		f = 1.0MHz
C <sub>oss</sub> eff. (ER)	Effective Output Capacitance (Energy Related)	—	255	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V <sup>⑥</sup>
C <sub>oss</sub> eff. (TR)	Effective Output Capacitance (Time Related)	—	478	—		V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 80V <sup>⑤</sup>

**Diode Characteristics**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	56	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①</sup>	—	—	252		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 38A, V <sub>GS</sub> = 0V <sup>④</sup>
dv/dt	Peak Diode Recovery	—	7.0	—	V/ns	T <sub>J</sub> = 175°C, I <sub>S</sub> = 38A, V <sub>DS</sub> = 100V <sup>③</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	34	—	ns	T <sub>J</sub> = 25°C V <sub>R</sub> = 86V
		—	39	—		T <sub>J</sub> = 125°C I <sub>F</sub> = 38A
Q <sub>rr</sub>	Reverse Recovery Charge	—	47	—	nC	T <sub>J</sub> = 25°C di/dt = 100A/μs <sup>④</sup>
		—	61	—		T <sub>J</sub> = 125°C
I <sub>RRM</sub>	Reverse Recovery Current	—	2.4	—	A	T <sub>J</sub> = 25°C
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				



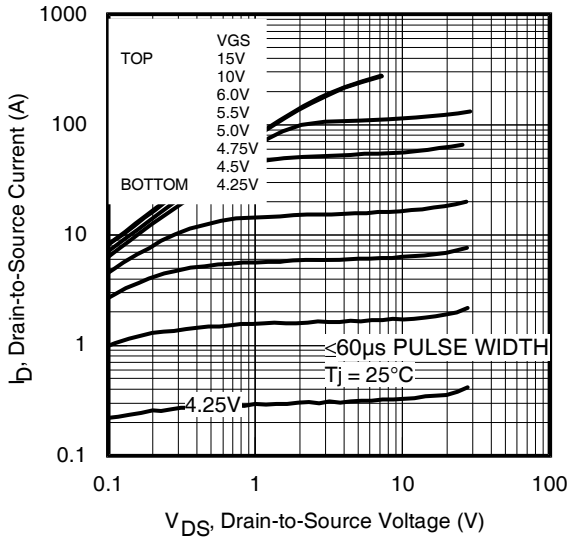


Fig 1. Typical Output Characteristics

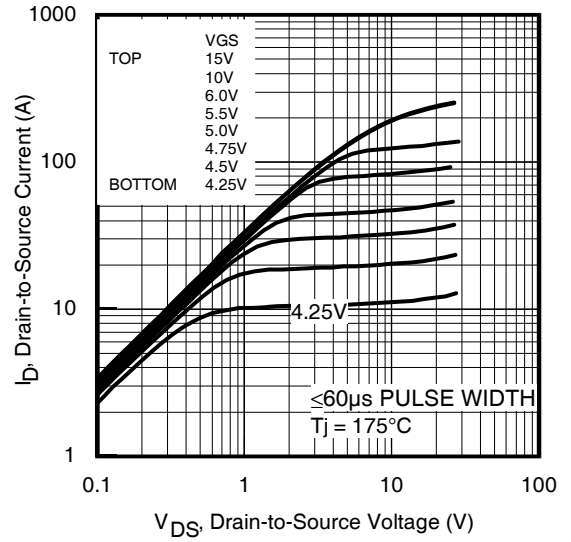


Fig 2. Typical Output Characteristics

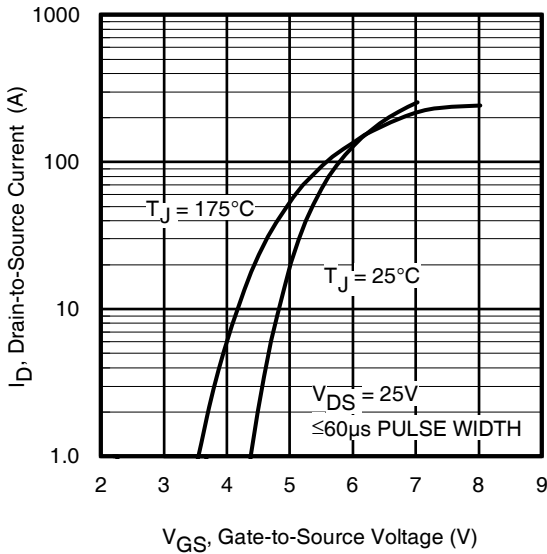


Fig 3. Typical Transfer Characteristics

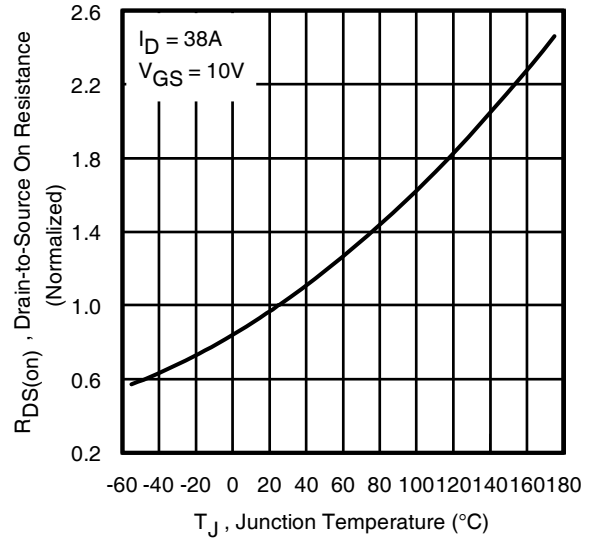


Fig 4. Normalized On-Resistance vs. Temperature

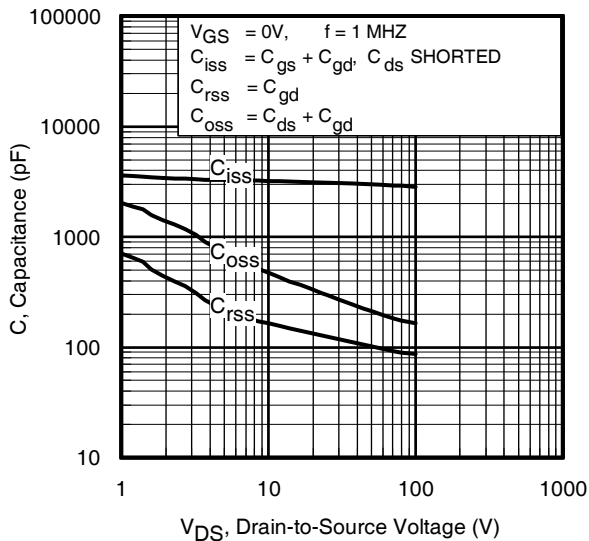


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

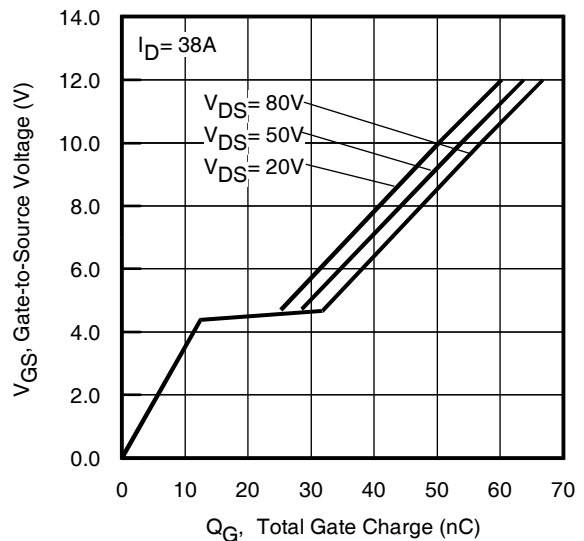
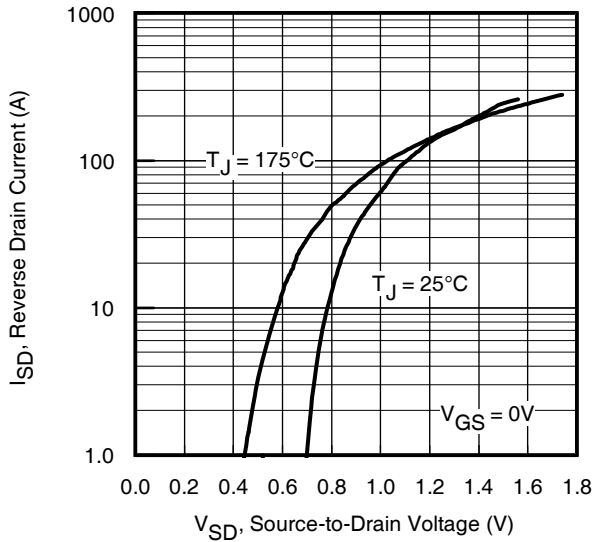
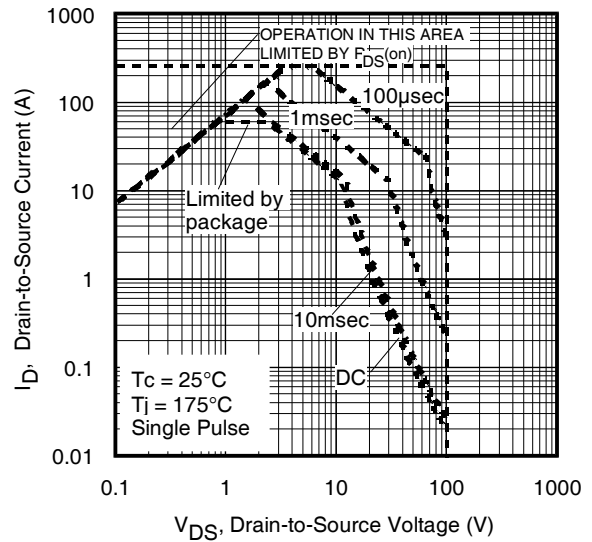


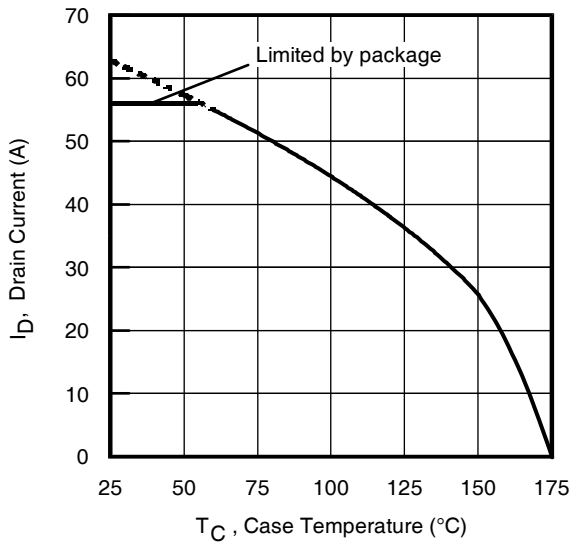
Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage



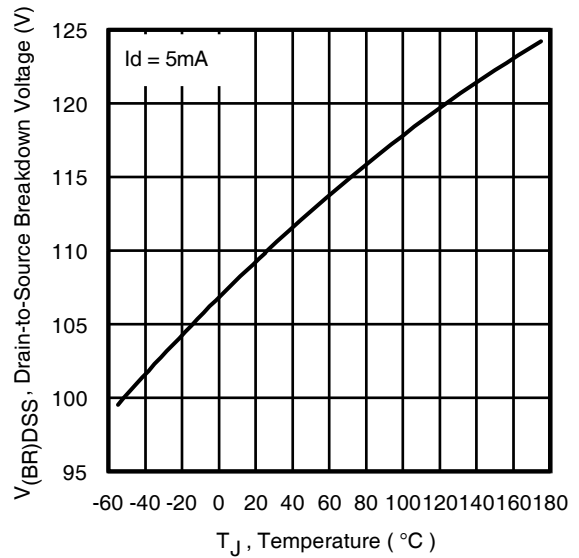
**Fig 7.** Typical Source-Drain Diode Forward Voltage



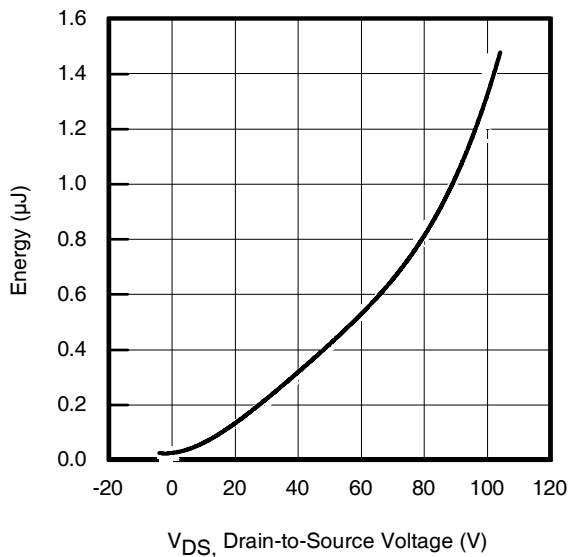
**Fig 8.** Maximum Safe Operating Area



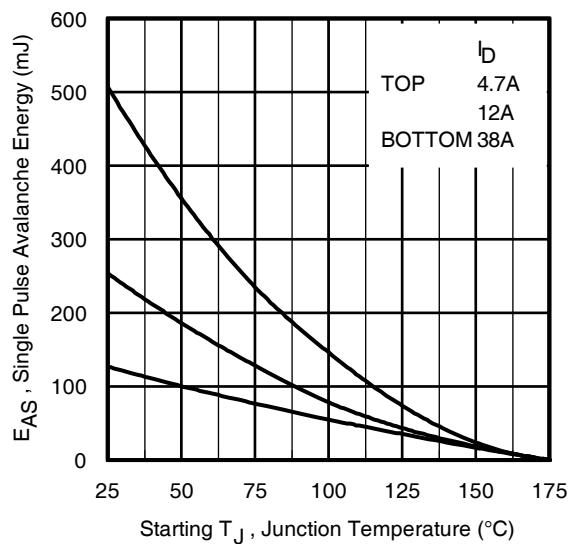
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Drain-to-Source Breakdown Voltage



**Fig 11.** Typical  $C_{OSS}$  Stored Energy



**Fig 12.** Maximum Avalanche Energy vs. Drain Current

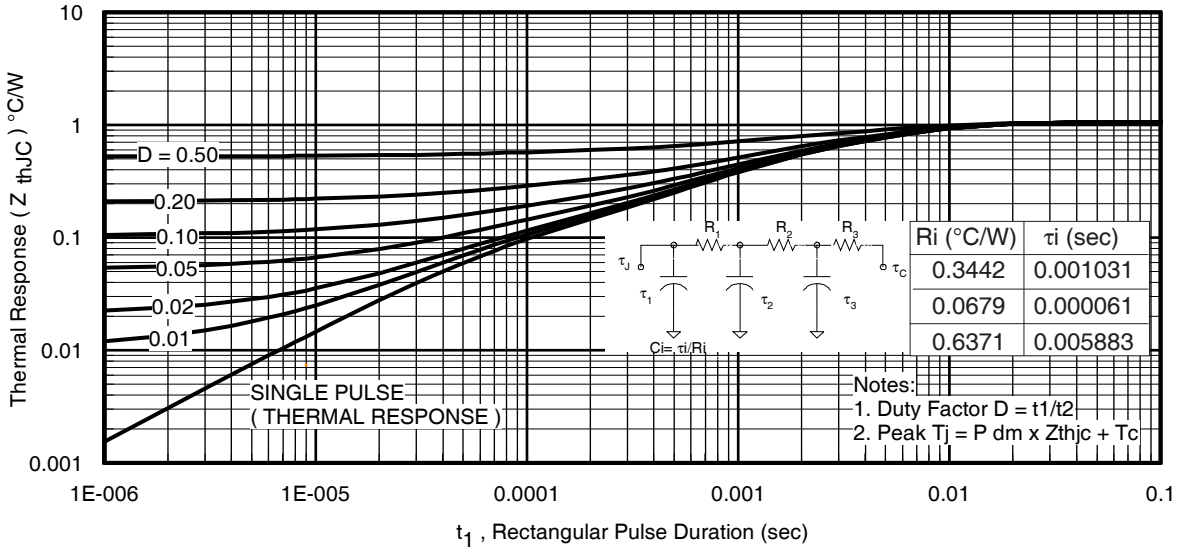


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

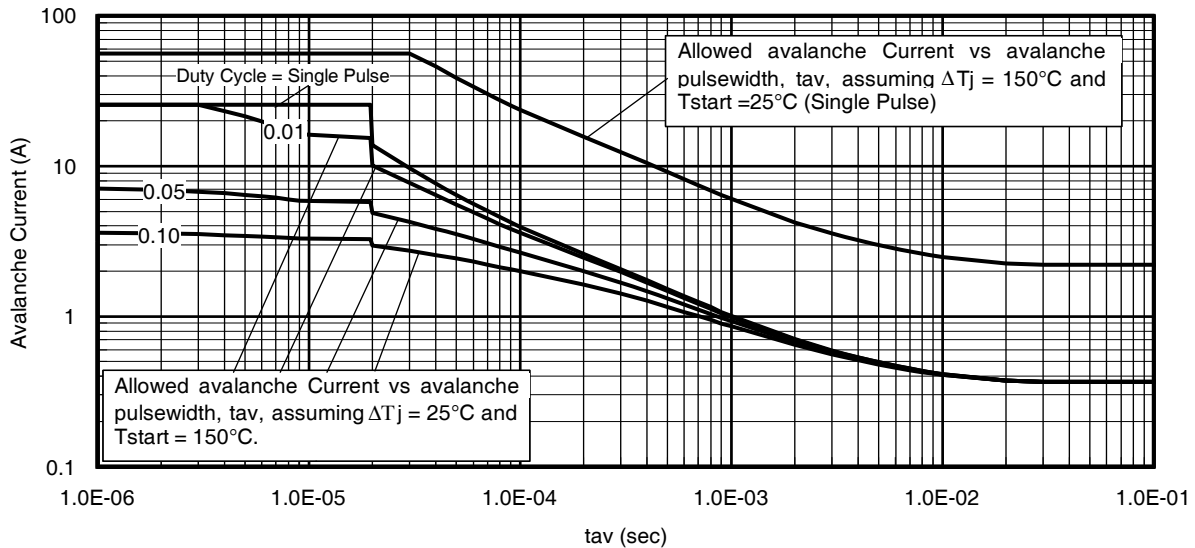


Fig 14. Typical Avalanche Current vs. Pulsewidth

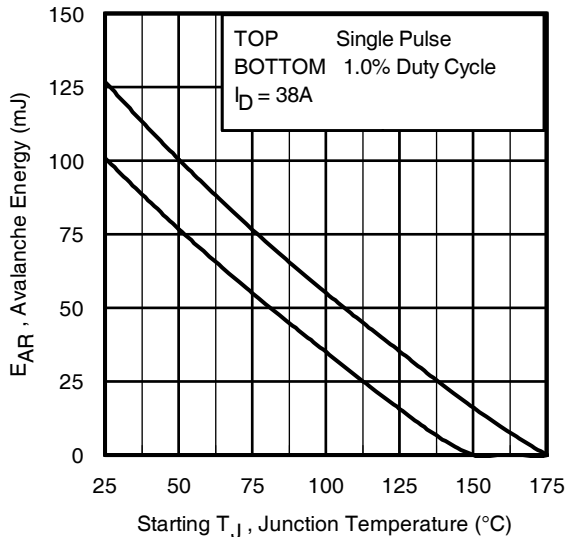


Fig 15. Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves, Figures 14, 15:**  
(For further info, see AN-1005 at [www.irf.com](http://www.irf.com))

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16a, 16b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 14, 15).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

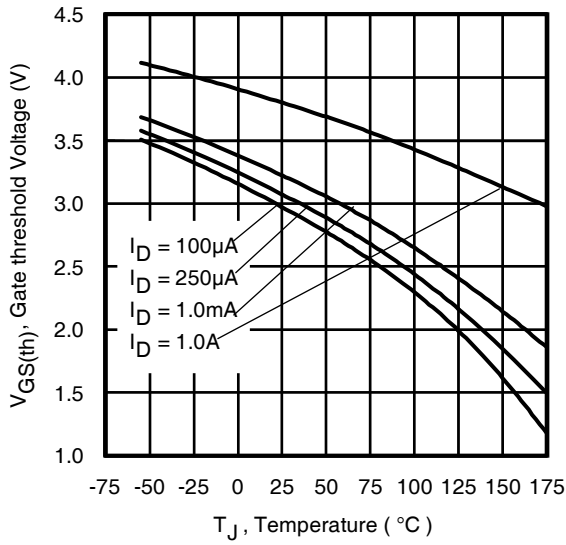


Fig 16. Threshold Voltage vs. Temperature

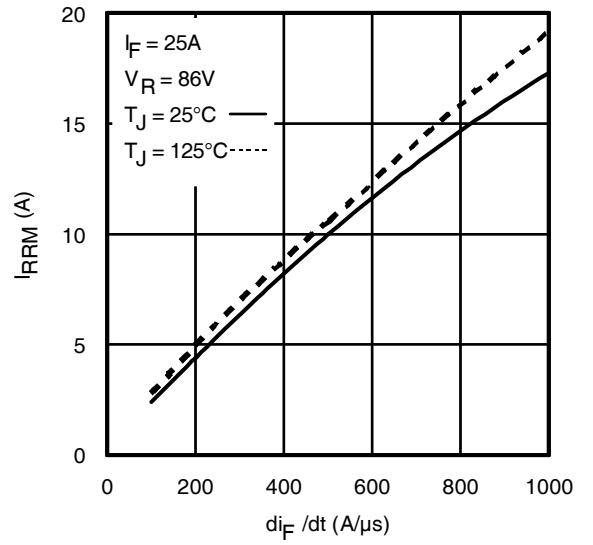


Fig. 17 - Typical Recovery Current vs. di/dt

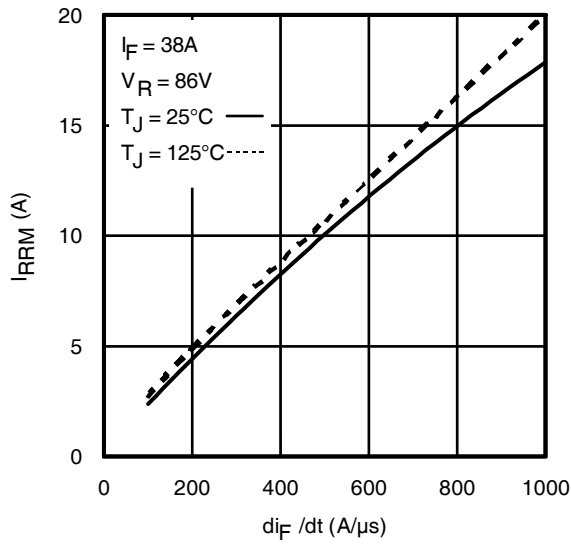


Fig. 18 - Typical Recovery Current vs. di/dt

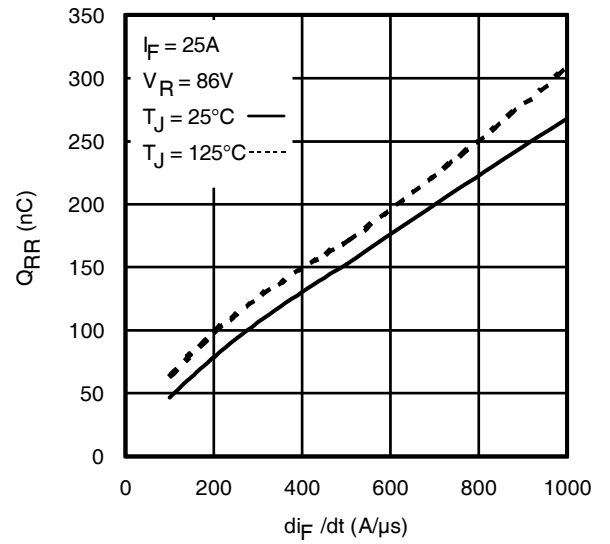


Fig. 19 - Typical Stored Charge vs. di/dt

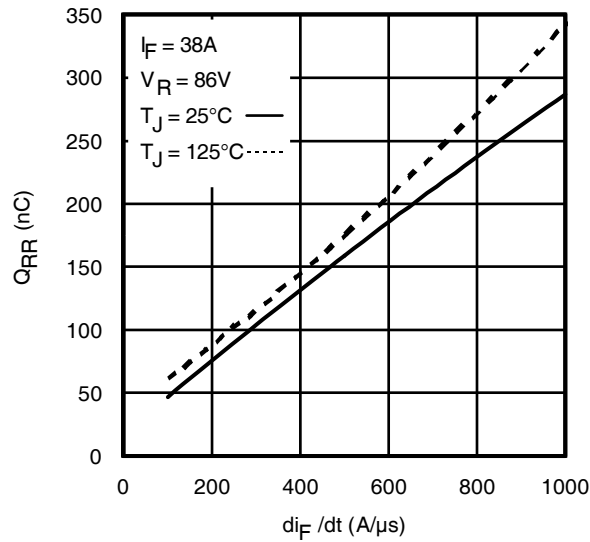
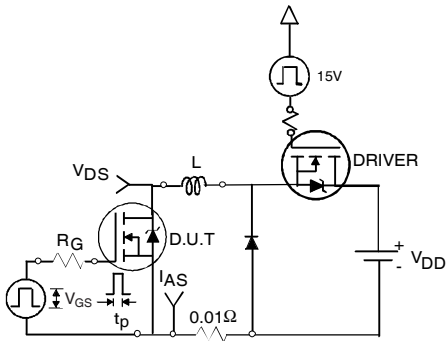


Fig. 20 - Typical Stored Charge vs. di/dt



\*  $V_{GS} = 5V$  for Logic Level Devices

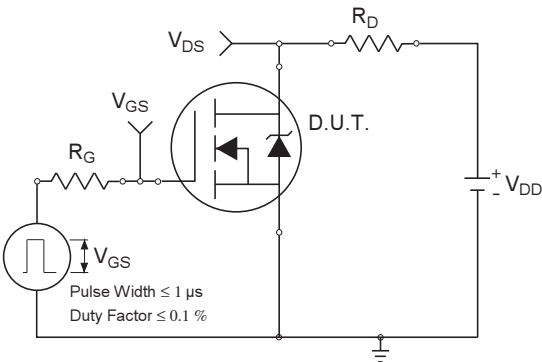
**Fig 21. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



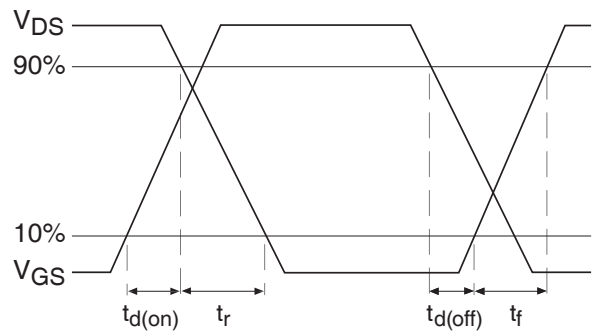
**Fig 22a. Unclamped Inductive Test Circuit**



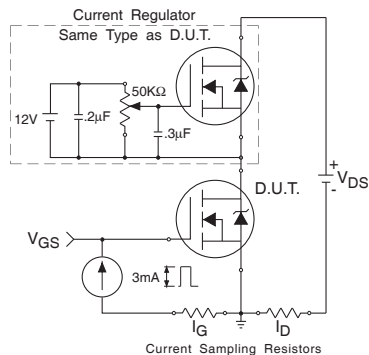
**Fig 22b. Unclamped Inductive Waveforms**



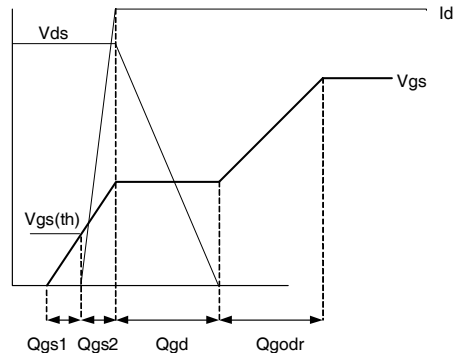
**Fig 23a. Switching Time Test Circuit**



**Fig 23b. Switching Time Waveforms**



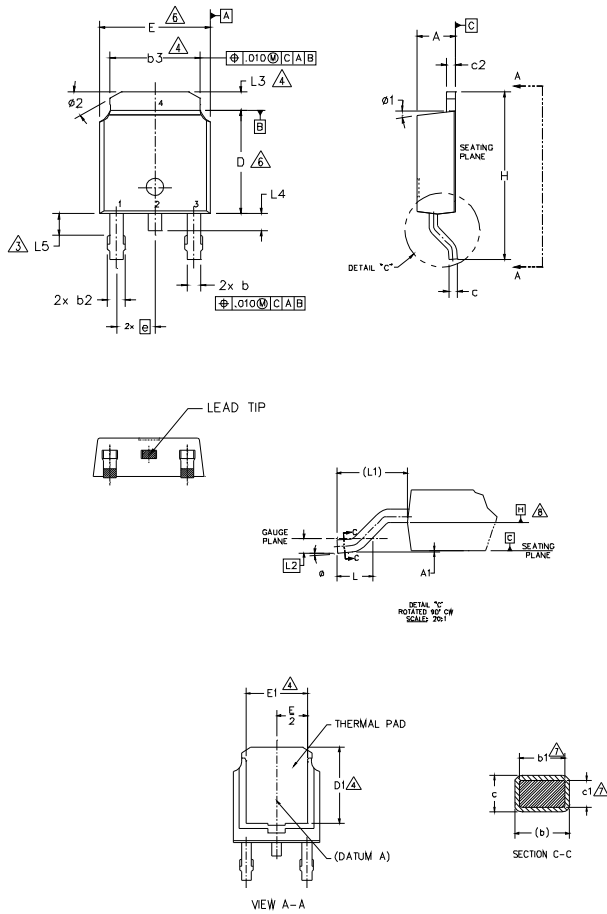
**Fig 24a. Gate Charge Test Circuit**



**Fig 24b. Gate Charge Waveform**

### D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
  - 2.- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS]
  - △ LEAD DIMENSION UNCONTROLLED IN L5.
  - △ DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
  - 5.- SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
  - △ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
  - △ DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
  - △ DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
  - 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1	-	0.13	-	.005	
b	0.64	0.89	.025	.035	
b1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
c	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
E	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
e	2.29 BSC		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 BSC		.108 REF.		
L2	0.51 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
φ	0"	10"	0"	10"	
φ1	0"	15"	0"	15"	
φ2	25"	35"	25"	35"	

**LEAD ASSIGNMENTS**

**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

**IGBT & CoPAK**

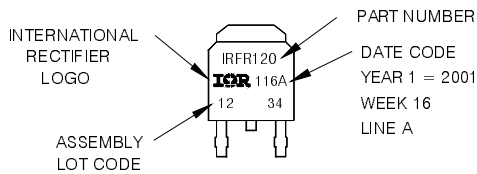
- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

### D-Pak (TO-252AA) Part Marking Information

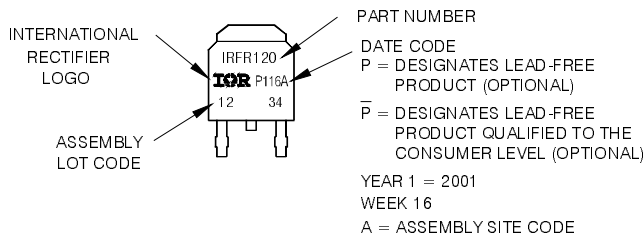
EXAMPLE: THIS IS AN IRFR120  
WITH ASSEMBLY  
LOT CODE 1234  
ASSEMBLED ON WW 16, 2001  
IN THE ASSEMBLY LINE 'A'

Note: 'P' in assembly line position  
indicates 'Lead-Free'

'P' in assembly line position indicates  
'Lead-Free' qualification to the consumer-level



OR



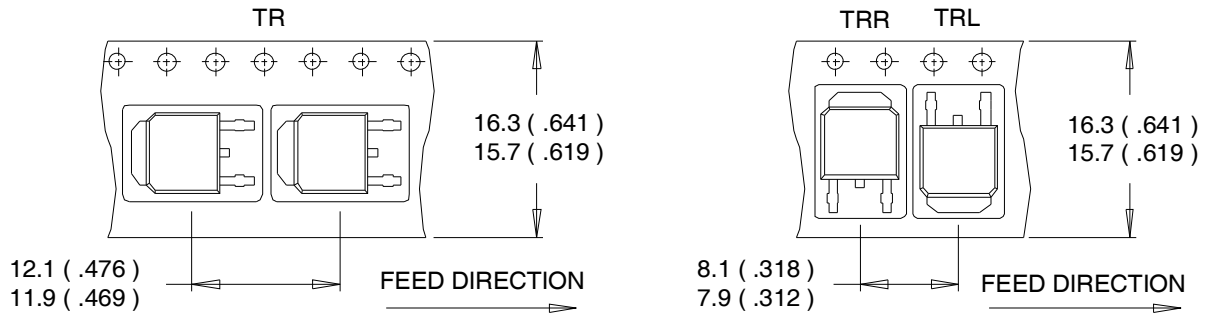
Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>





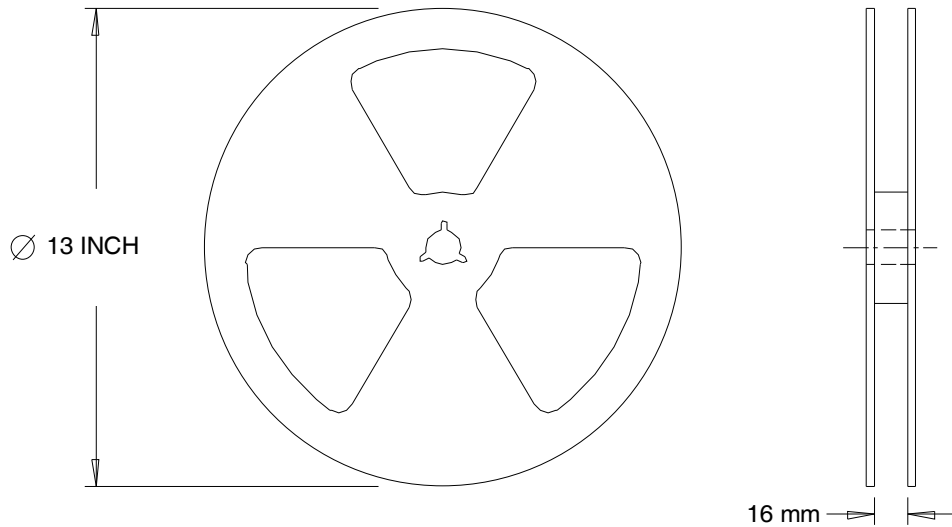
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Orderable part number	Package Type	Standard Pack		Note
		Form	Quantity	
IRFR4510PbF	D-PAK	Tube/Bulk	75	
IRFR4510TRPbF	D-PAK	Tape and Reel	2000	
IRFU4510PbF	I-PAK	Tube/Bulk	75	

### Qualification Information<sup>†</sup>

Qualification level	Industrial <sup>††</sup>	
	(per JEDEC JESD47F <sup>†††</sup> guidelines)	
	Comments: This family of products has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture Sensitivity Level	D-PAK	MSL1 (per JEDEC J-STD-020D <sup>†††</sup> )
	I-PAK	Not applicable
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site <http://www.irf.com/product-info/reliability>

†† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information: <http://www.irf.com/whoto-call/salesrep/>

††† Applicable version of JEDEC standard at the time of product release.

#### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.18\text{mH}$   
 $R_G = 50\Omega$ ,  $I_{AS} = 38\text{A}$ ,  $V_{GS} = 10\text{V}$ . Part not recommended for use above this value.
- ③  $I_{SD} \leq 38\text{A}$ ,  $di/dt \leq 2031\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥  $C_{OSS}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧  $R_{\theta}$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .

Data and specifications subject to change without notice

International  
**IR** Rectifier

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