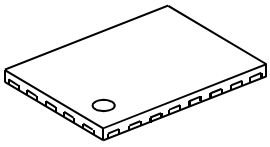
Quad Channel Combination Regulator

■ FEATURES

- Operating temperature range -40 to 125°C
- Including four regulators;
  Ch.1: Wide input range 1.2A buck converter.
  Ch.2: Low voltage 0.6A synchronous buck converter.
  Ch.3: Selectable regulator.
  Low voltage 0.6A synchronous buck converter
  / Low voltage 0.3A LDO
  Ch.4: Low voltage 0.3A LDO
  e.g.) Ta=85 °C, fosc=2MHz
  DC-DC Ch.1: 12V → 3.3V/1000mA
  (Included supply for Ch.2, 3, 4)
  Ch.2: 3.3V → 1.8V/500mA
  Ch.3: 3.3V → 1.2V/500mA
  LDO Ch.4: 3.3V → 2.8V/200mA
- Wide operating input voltage range
  3.9V(UVLO ON: 3.35V) to 40V (Ch.1)
  2.4V to 5.5V (Ch.2, Ch.3, Ch.4)
- Free power-on sequence
  - Individual Power-Good Function
    (High precision -7%, + 15%)
  - Individual Standby Function
- Protection function
  - UVLO (Under Voltage Lockout)
  - Over current protection function for more safety operation
    (Hiccup or Latch)
  - Thermal shutdown
- Oscillating frequency 280kHz to 2.4MHz
- External clock synchronization
- Anti-phase operation between Ch.1 and Ch.2 / 3
- Current mode control buck converters
- Built-in compensation circuit
- Soft start function

■ PACKAGE

EQFN26-HH



3.4mm x 2.6mm

■ GENERAL DESCRIPTION

The NJW4750 is quad channel combination regulator including one wide input range buck converter and three secondary synchronous buck converter / LDO. Ch.3 can be selectable to the synchronous buck converter mode or LDO mode. Therefore, the NJW4750 expands the choices when building power supply block suitable for various applications.

The NJW4750 is operated anti-phase operation between Ch.1 and Ch.2 / 3 in order to reduce EMI noise.

Every regulator has individual enable pin and power-good pin. Therefore, flexible power-on sequence configuration is available.

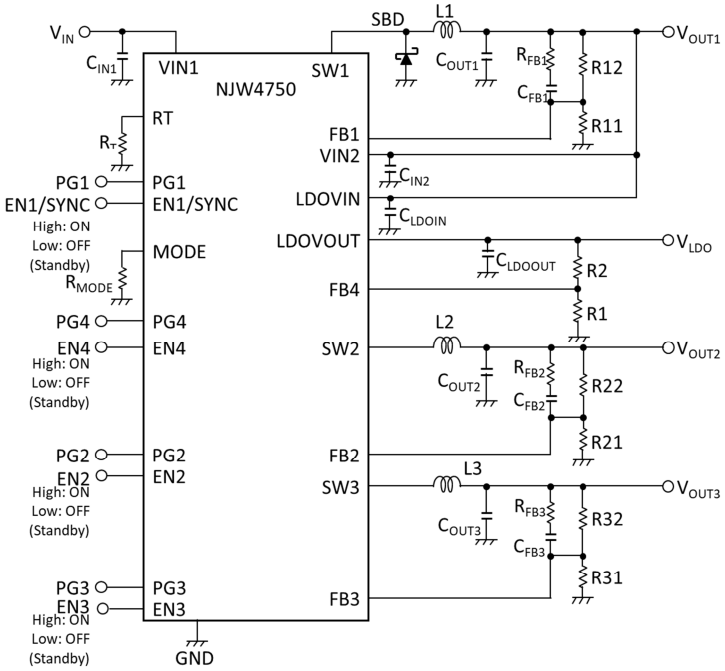
The NJW4750 has two types of over-current protection according to application demand.
Furthermore, it adopts a new overcurrent detection method which is more safety and contributes to miniaturization of the inductor.

Small package: 3.4mm × 2.6mm QFN is adopted suitable for small application such as camera module.

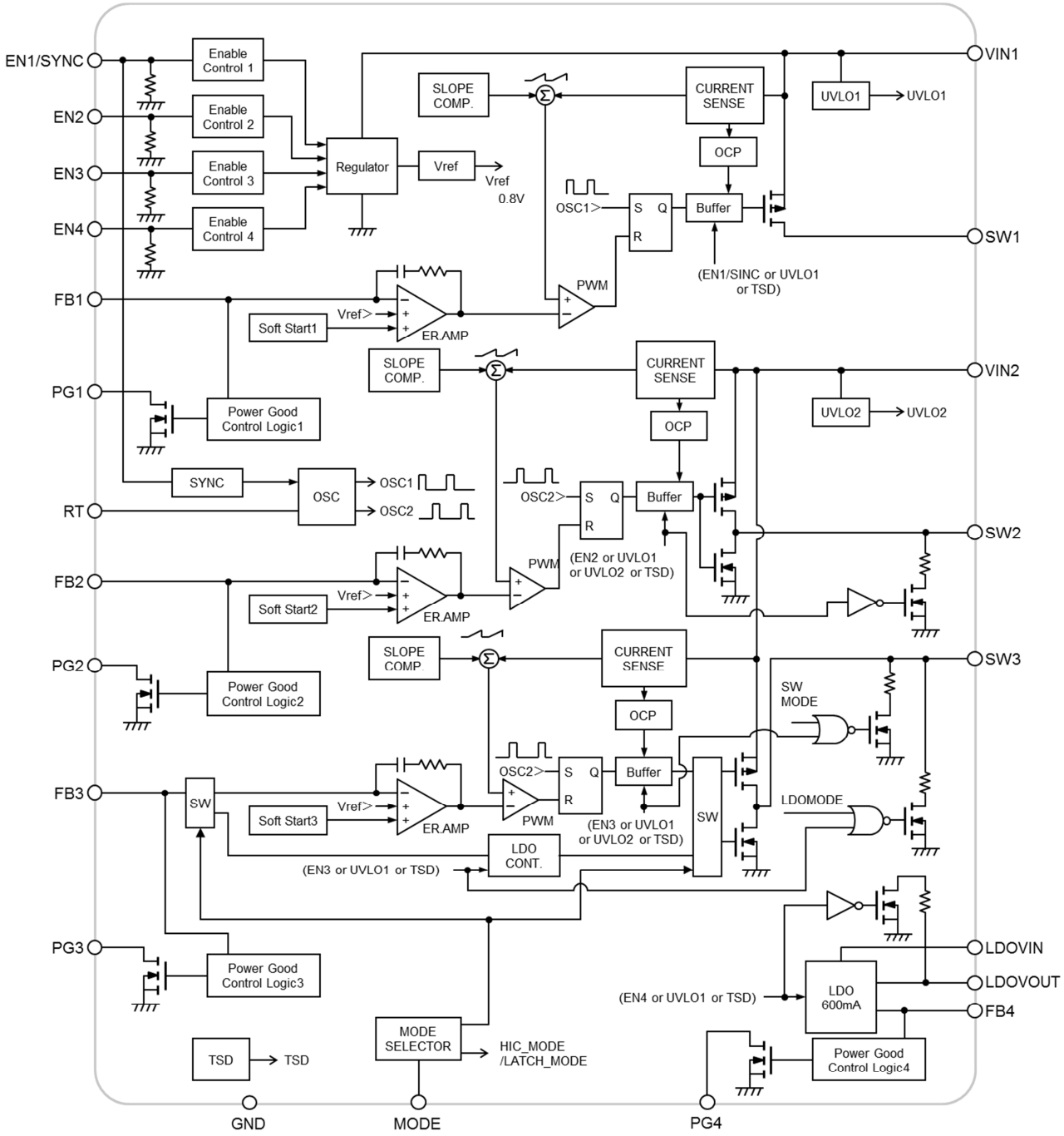
■ TARGET APPLICATION

- Camera Module
- Photoelectric sensor
- Small Application and other.

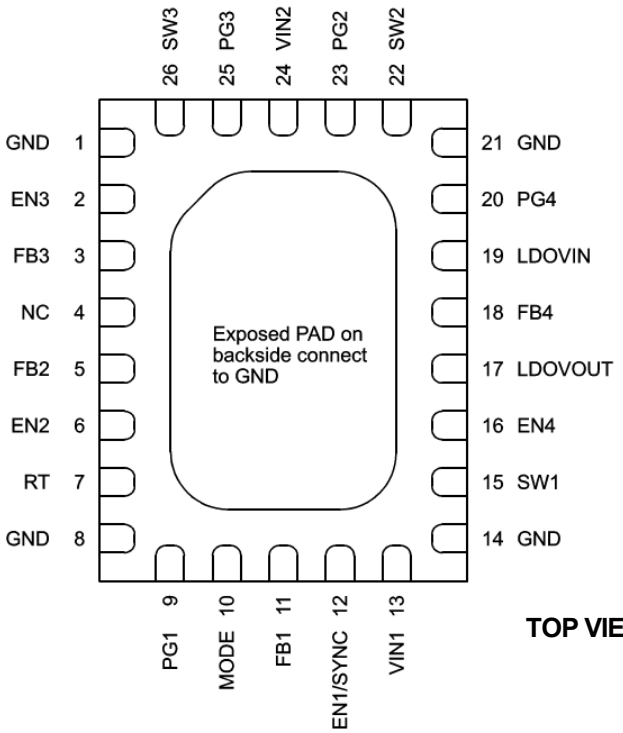
■ APPLICATION



■ BLOCK DIAGRAM



■ PIN CONFIGURATION



TOP VIEW

PIN NO.	SYMBOL	DESCRIPTION	PIN NO.	SYMBOL	DESCRIPTION
1	GND	Ground	14	GND	Ground
2	EN3	Ch.3 Enable input	15	SW1	Ch.1 Output
3	FB3	Ch.3 Voltage feedback input	16	EN4	Ch.4 Enable input
4	NC	NC	17	LDOVOUT	Ch.4 Output
5	FB2	Ch.2 Voltage feedback input	18	FB4	Ch.4 Voltage feedback input
6	EN2	Ch.2 Enable input	19	LDOVIN	Ch.4 Power supply input
7	RT	Oscillation frequency setting	20	PG4	Ch.4 Power-good output
8	GND	Ground	21	GND	Ground
9	PG1	Ch.1 Power-good output	22	SW2	Ch.2 Output
10	MODE	Ch.3 Mode select / OCP setting	23	PG2	Ch.2 Power-good output
11	FB1	Ch.1 Voltage feedback input	24	VIN2	Ch.2, Ch.3 Power supply input
12	EN1/SYNC	Ch.1 Enable input /External CLK input	25	PG3	Ch.3 Power-good output
13	VIN1	Ch.1 Power supply input	26	SW3	Ch.3 Output

■ PRODUCT NAME INFORMATION

NJW4750 MHH -T1 (TE1)

- NJW4750: Part Number
- MHH: Package (MHH: EQFN26-HH)
- T1: Grade
- (TE1): Taping Form

■ ORDERING INFORMATION

PRODUCT NAME	PACKAGE	RoHS	HALOGEN FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW4750MHH-T1(TE1)	EQFN26-HH	yes	yes	Sn2Bi	4750T	18	1500

■ ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MAXIMUM RATING	UNIT
Supply Voltage	V_{VIN1}	-0.3 to +45	V
	V_{VIN2}, V_{LDOVIN}	-0.3 to +7	V
Voltage between pins VIN1 - SW1	$V_{VIN1-SW1}$	+45	V
SW2/SW3 pin Voltage	V_{SW2} V_{SW3}	+7	V
EN/SYNC pin Voltage	$V_{EN1/SYNC}$	-0.3 to +45	V
EN pin Voltage	V_{EN2}, V_{EN3}	-0.3 to +7	V
	V_{EN4}	-0.3 to +45	V
FB pin Voltage	V_{FB1}, V_{FB2}, V_{FB3}, V_{FB4}	-0.3 to +7	V
PG pin Voltage	V_{PG1}, V_{PG2}, V_{PG3}, V_{PG4}	-0.3 to +7	V
Power Dissipation(Ta=25°C)	P_D	EQFN26-HH 850 (1) 2500 (2)	mW
Junction Temperature	Tj	-40 to +150	°C
Operating Temperature	T_{opr}	-40 to +125	°C
Storage Temperature	T_{stg}	-50 to +150	°C

(1): Mounted on glass epoxy board.
(101.5×114.5×1.6mm:based on EIA/JEDEC standard,2layers, with Exposed Pad)
(2): Mounted on glass epoxy board.
(101.5×114.5×1.6mm:based on EIA/JEDEC standard,4layers, with Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via holes to a board based on JEDEC standard JESD51-5)

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{VIN1}	3.9 to 40	V
	V_{VIN2}, V_{LDOVIN}	2.4 to 5.5	V
EN/SYNC pin Voltage	$V_{EN1/SYNC}$	0 to 40	V
EN pin Voltage	V_{EN2}, V_{EN3}, V_{EN4}	0 to 5.5	V
PG pin Voltage	V_{PG1}, V_{PG2}, V_{PG3}, V_{PG4}	0 to 5.5	V
Timing Resistor	R_T	1.8 to 27	kΩ
Oscillating Frequency	f_{OSC}	280 to 2400	kHz
External Clock Input	f_{SYNC}	f_{OSC}×0.9 to f_{OSC}×1.7 Upper limit 2800kHz	kHz

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{VIN1}=$V_{EN1/SYNC}$=12V, R_T=6.8kΩ, Ta=25°C)

Ch.1 (Wide input range buck converter)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Under Voltage Lock Out Circuit Block						
ON Threshold Voltage	V_{T_ON1}	V_{VIN1}=L → H	3.60	3.75	3.90	V
		V_{VIN1}=L → H Ta=-40°C to +125°C	3.60	–	3.90	
OFF Threshold Voltage	V_{T_OFF1}	V_{VIN1}=H → L	3.05	3.20	3.35	V
		V_{VIN1}=H → L Ta=-40°C to +125°C	3.05	–	3.35	
Hysteresis Voltage	V_{HYS1}		500	550	–	mV
Soft Start Block						
Soft Start Time	t_{SS1}	V_{FB1}=0.75V	1.0	2.5	4.0	ms
		V_{FB1}=0.75V Ta=-40°C to +125°C	0.5	–	4.5	
Oscillator Block						
Oscillating Frequency 1	f_{OSC11}	R_T=27kΩ	250	280	310	kHz
		R_T=27kΩ Ta=-40°C to +125°C	250	–	310	
Oscillating Frequency 2	f_{OSC12}	R_T=6.8kΩ	900	1000	1100	kHz
		R_T=6.8kΩ Ta=-40°C to +125°C	900	–	1100	
Oscillating Frequency 3	f_{OSC13}	R_T=1.8kΩ	2200	2400	2600	kHz
		R_T=1.8kΩ Ta=-40°C to +125°C	2200	–	2600	
Error Amplifier Block						
Reference Voltage	V_{B1}		-1.0%	0.8	+1.0%	V
		Ta=-40°C to +125°C	-2.0%	–	+2.0%	
Input Bias Current	I_{B1}		-0.1	–	0.1	μA
		Ta=-40°C to +125°C	-0.1	–	0.1	

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{VIN1}=$V_{EN1/SYNC}$=12V, R_T=6.8kΩ, Ta=25°C)

Ch.1（Wide input range buck converter）

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PWM Comparator Block						
Maximum Duty Cycle	$M_{AX}D_{UTY1}$	V_{FB1}=0.7V	100	–	–	%
		V_{FB1}=0.7V Ta=-40°C to +125°C	100	–	–	
Minimum OFF Time	$t_{OFF1\text{-}min}$		–	55	–	ns
Minimum ON Time	$t_{ON1\text{-}min}$		–	60	–	ns
Over Current Protection Circuit Block						
Cool Down Time	t_{COOL1}	R_{MODE}=36kΩ or 10 kΩ	–	75	–	ms
Output Block						
Output ON Resistance	R_{ON1}	I_{SW1}=0.8A	–	0.5	0.8	Ω
Switching Current Limit	I_{LIM1}		1.4	1.7	2.0	A
Switching Leak Current	I_{LEAK1}	$V_{EN1/SYNC}$=0V, V_{VIN1}=40V V_{SW1}=0V Ta=-40°C to +125°C	–	–	4	μA
Enable Control / Sync Block (EN1/SYNC)						
High Threshold Voltage	$V_{THH\_EN1/SYNC}$	$V_{EN1/SYNC}$=L → H	1.6	–	40.0	V
		$V_{EN1/SYNC}$=L → H Ta=-40°C to +125°C	1.6	–	40.0	
Low Threshold Voltage	$V_{THL\_EN1/SYNC}$	$V_{EN1/SYNC}$=H → L	0	–	0.4	V
		$V_{EN1/SYNC}$=H → L Ta=-40°C to +125°C	0	–	0.4	
Input Bias Current	$I_{EN1/SYNC}$	$V_{EN1/SYNC}$=5V	–	1	3	μA
		$V_{EN1/SYNC}$=5V Ta=-40°C to +125°C	–	–	5	

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{VIN1}=$V_{EN1/SYNC}$=12V, R_T=6.8kΩ, Ta=25°C)

Ch.1 (Wide input range buck converter)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Good Block（PG1）						
High Level Detection Reference Voltage	V_{THH_PG1}	Rising	0.836	–	0.924	V
		Rising, Ta=-40°C to +125°C	0.836	–	0.924	
Low Level Detection Reference Voltage	V_{THL_PG1}	Rising	0.745	–	0.775	V
		Rising, Ta=-40°C to +125°C	0.745	–	0.775	
Hysteresis Voltage	V_{HYS_PG1}		–	16	–	mV
Power Good ON Resistance	R_{ON_PG1}	I_{PG1}=10mA	–	100	–	Ω
Leak Current at OFF State	I_{LEAK_PG1}	V_{PG1}=5.5V	–	–	0.1	μA
		V_{PG1}=5.5V Ta=-40°C to +125°C	–	–	0.1	

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{VIN1}=12V, V_{VIN2}=V_{EN2}=3.3V, R_T=6.8kΩ, Ta=25°C)

Ch.2 (Low voltage synchronous buck converter)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Under Voltage Lock Out Circuit Block						
ON Threshold Voltage	V_{T_ON2}	V_{VIN2}=L → H	2.10	2.25	2.40	V
		V_{VIN2}=L → H Ta=-40°C to +125°C	2.10	–	2.40	
OFF Threshold Voltage	V_{T_OFF2}	V_{VIN2}=H → L	2.00	2.15	2.30	V
		V_{VIN2}=H → L Ta=-40°C to +125°C	2.00	–	2.30	
Hysteresis Voltage	V_{HYS2}		50	100	–	mV
Soft Start Block						
Soft Start Time	t_{SS2}	V_{FB2}=0.75V	1.0	2.5	4.0	ms
		V_{FB2}=0.75V Ta=-40°C to +125°C	0.5	–	4.5	
Oscillator Block						
Oscillating Frequency 1	f_{OSC21}	R_T=27kΩ	250	280	310	kHz
		R_T=27kΩ Ta=-40°C to +125°C	250	–	310	
Oscillating Frequency 2	f_{OSC22}	R_T=6.8kΩ	900	1000	1100	kHz
		R_T=6.8kΩ Ta=-40°C to +125°C	900	–	1100	
Oscillating Frequency 3	f_{OSC23}	R_T=1.8kΩ	2200	2400	2600	kHz
		R_T=1.8kΩ Ta=-40°C to +125°C	2200	–	2600	
Error Amplifier Block						
Reference Voltage	V_{B2}		-1.0%	0.8	+1.0%	V
		Ta=-40°C to +125°C	-2.0%	–	+2.0%	
Input Bias Current	I_{B2}		-0.1	–	0.1	μA
		Ta=-40°C to +125°C	-0.1	–	0.1	

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{VIN1}=12V, V_{VIN2}=V_{EN2}=3.3V, R_T=6.8kΩ, Ta=25°C)

Ch.2 (Low voltage synchronous buck converter)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PWM Comparator Block						
Maximum Duty Cycle	$M_{AX}D_{UTY2}$	V_{FB2}=0.7V	100	–	–	%
		V_{FB2}=0.7V Ta=-40°C to +125°C	100	–	–	
Minimum OFF Time	$t_{OFF2\text{-}min}$		–	55	–	ns
Minimum ON Time	$t_{ON2\text{-}min}$		–	80	–	ns
Over Current Protection Circuit Block						
Cool Down Time	t_{COOL2}	R_{MODE}=36kΩ or 10 kΩ	–	75	–	ms
Output Block						
Pch Output ON Resistance	R_{ONP2}	$I_{SW2SOURCE}$=0.5A	–	0.5	0.8	Ω
Nch Output ON Resistance	R_{ONN2}	$I_{SW2SINK}$=0.5A	–	0.3	0.5	Ω
Switching Current Limit	I_{LIM2}		0.7	1.0	1.3	A
Switching Leak Current	I_{LEAK2}	V_{EN2}=0V, V_{VIN2}=5.5V V_{SW2}=0V Ta=-40°C to +125°C	–	–	4	μA
Enable Control Block (EN2)						
High Threshold Voltage	V_{THH_EN2}	V_{EN2}=L → H	1.0	–	5.5	V
		V_{EN2}=L → H Ta=-40°C to +125°C	1.0	–	5.5	
Low Threshold Voltage	V_{THL_EN2}	V_{EN2}=H → L	0	–	0.4	V
		V_{EN2}=H → L Ta=-40°C to +125°C	0	–	0.4	
Input Bias Current	I_{EN2}	V_{EN2}=3.3V	–	7	14	μA
		V_{EN2}=3.3V Ta=-40°C to +125°C	–	–	14	

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{VIN1}=12V, V_{VIN2}=V_{EN2}=3.3V, R_T=6.8kΩ, Ta=25°C)

Ch.2 (Low voltage synchronous buck converter)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Power Good Block (PG2)						
High Level Detection Reference Voltage	V_{THH_PG2}	Rising	0.836	–	0.924	V
		Rising, Ta=-40°C to +125°C	0.836	–	0.924	
Low Level Detection Reference Voltage	V_{THL_PG2}	Rising	0.745	–	0.775	V
		Rising, Ta=-40°C to +125°C	0.745	–	0.775	
Hysteresis Voltage	V_{HYS_PG2}		–	16	–	mV
Power Good ON Resistance	R_{ON_PG2}	I_{PG2}=10mA	–	100	–	Ω
Leak Current at OFF State	I_{LEAK_PG2}	V_{PG2}=5.5V	–	–	0.1	μA
		V_{PG2}=5.5V Ta=-40°C to +125°C	–	–	0.1	

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{VIN1}=12V, V_{VIN2}=V_{EN3}=3.3V, R_T=6.8kΩ , Ta=25°C)

Ch.3 (Selectable regulator: SW Reg. MODE and LDO MODE can share the same table.)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Enable Control Block（EN3）						
High Threshold Voltage	V_{THH_EN3}	V_{EN3}=L → H	1.0	–	5.5	V
		V_{EN3}=L → H Ta=-40°C to +125°C	1.0	–	5.5	
Low Threshold Voltage	V_{THL_EN3}	V_{EN3}=H → L	0	–	0.4	V
		V_{EN3}=H → L Ta=-40°C to +125°C	0	–	0.4	
Input Bias Current	I_{EN3}	V_{EN3}=3.3V	–	7	14	μA
		V_{EN3}=3.3V Ta=-40°C to +125°C	–	–	14	
Power Good Block (PG3)						
High Level Detection Reference Voltage	V_{THH_PG3}	Rising	0.836	–	0.924	V
		Rising, Ta=-40°C to +125°C	0.836	–	0.924	
Low Level Detection Reference Voltage	V_{THL_PG3}	Rising	0.745	–	0.775	V
		Rising, Ta=-40°C to +125°C	0.745	–	0.775	
Hysteresis Voltage	V_{HYS_PG3}		–	16	–	mV
Power Good ON Resistance	R_{ON_PG3}	I_{PG3}=10mA	–	100	–	Ω
Leak Current at OFF State	I_{LEAK_PG3}	V_{PG3}=5.5V	–	–	0.1	μA
		V_{PG3}=5.5V Ta=-40°C to +125°C	–	–	0.1	

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{VIN1}=12V, V_{VIN2}=V_{EN3}=3.3V, R_T=6.8kΩ, R_{MODE}= 82kΩ or 36kΩ, Ta=25°C)

Ch.3 (Selectable regulator: SW Reg. MODE)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Under Voltage Lock Out Circuit Block						
ON Threshold Voltage	V_{T_ON3}	V_{VIN2}=L → H	2.10	2.25	2.40	V
		V_{VIN2}=L → H Ta=-40°C to +125°C	2.10	–	2.40	
OFF Threshold Voltage	V_{T_OFF3}	V_{VIN2}=H → L	2.00	2.15	2.30	V
		V_{VIN2}=H → L Ta=-40°C to +125°C	2.00	–	2.30	
Hysteresis Voltage	V_{HYS3}		50	100	–	mV
Soft Start Block						
Soft Start Time	t_{SS3}	V_{FB3}=0.75V	1.0	2.5	4.0	ms
		V_{FB3}=0.75V Ta=-40°C to +125°C	0.5	–	4.5	
Oscillator Block						
Oscillating Frequency 1	f_{OSC31}	R_T=27kΩ	250	280	310	kHz
		R_T=27kΩ Ta=-40°C to +125°C	250	–	310	
Oscillating Frequency 2	f_{OSC32}	R_T=6.8kΩ	900	1000	1100	kHz
		R_T=6.8kΩ Ta=-40°C to +125°C	900	–	1100	
Oscillating Frequency 3	f_{OSC33}	R_T=1.8kΩ	2200	2400	2600	kHz
		R_T=1.8kΩ Ta=-40°C to +125°C	2200	–	2600	
Error Amplifier Block						
Reference Voltage	V_{B3}		-1.0%	0.8	+1.0%	V
		Ta=-40°C to +125°C	-2.0%	–	+2.0%	
Input Bias Current	I_{B3}		-0.1	–	0.1	μA
		Ta=-40°C to +125°C	-0.1	–	0.1	

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{VIN1}=12V, V_{VIN2}=V_{EN3}=3.3V, R_T=6.8kΩ, R_{MODE}= 82kΩ or 36kΩ, Ta=25°C)

Ch.3 (Selectable regulator: SW Reg. MODE)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
PWM Comparator Block						
Maximum Duty Cycle	$M_{AX}D_{UTY3}$	V_{FB3}=0.7V	100	–	–	%
		V_{FB3}=0.7V Ta=-40°C to +125°C	100	–	–	
Minimum OFF Time	$t_{OFF3\text{-}min}$		–	55	–	ns
Minimum ON Time	$t_{ON3\text{-}min}$		–	80	–	ns
Over Current Protection Circuit Block						
Cool Down Time	t_{COOL3}	R_{MODE}=36kΩ	–	75	–	ms
Output Block						
Pch Output ON Resistance	R_{ONP3}	$I_{SW3SOURCE}$=0.5A	–	0.5	0.8	Ω
Nch Output ON Resistance	R_{ONN3}	$I_{SW3SINK}$=0.5A	–	0.3	0.5	Ω
Switching Current Limit	I_{LIM3}		0.7	1.0	1.3	A
Switching Leak Current	I_{LEAK3}	V_{EN3}=0V, V_{VIN2}=5.5V V_{SW3}=0V Ta=-40°C to +125°C	–	–	4	μA

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{VIN1}=12V, V_{VIN2} =V_{EN3}=3.3V, R_T=6.8kΩ, R_{MODE}= OPEN or 10kΩ, Ta=25°C)

Ch.3 (Selectable regulator: LDO MODE)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Error Amplifier Block						
Reference Voltage	V_{B3}		-1.0%	0.8	+1.0%	V
		Ta=-40°C to +125°C	-2.0%	–	+2.0%	
Output Current	I_{OUT3}	V_{OUT3}×0.9	300	600	–	mA
		V_{OUT3}×0.9 Ta=-40°C to +125°C	300	–	–	
Load Regulation	ΔV_{OUT3} /I_{OUT3}	I_{OUT3}=1mA to 200mA	–	0.003	0.009	%/mA
		I_{OUT3}=1mA to 200mA Ta=-40°C to +125°C	–	–	0.020	
Ripple Rejection	RR3	ein=50mVrms, f=1kHz V_{OUT3}=2.5V, I_{OUT3}=150mA	–	40	–	dB
Dropout Voltage	ΔV_{IO3}	I_{OUT3}=200mA	–	0.2	0.3	V
		I_{OUT3}=200mA Ta=-40°C to +125°C	–	–	0.4	
Average Temperature Coefficient of Output Voltage	ΔV_{OUT3} /Ta	I_{OUT3}=150mA Ta=-20°C to +75°C	–	±50	–	ppm/°C

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{VIN1}=12V, V_{LDOVIN}=V_{EN4} =3.3V, R_T=6.8kΩ, Ta=25°C)

Ch.4 (Low voltage LDO)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Error Amplifier Block						
Reference Voltage	V_{B4}		-1.0%	0.8	+1.0%	V
		Ta=-40°C to +125°C	-2.0%	–	+2.0%	
Output Current	I_{OUT4}	V_{OUT4}×0.9	300	600	–	mA
		V_{OUT4}×0.9 Ta=-40°C to +125°C	300	–	–	
Load Regulation	ΔV_{OUT4} /I_{OUT4}	I_{OUT4}=1mA to 200mA	–	0.003	0.009	%/mA
		I_{OUT4}=1mA to 200mA Ta=-40°C to +125°C	–	–	0.020	
Ripple Rejection	RR4	ein=50mVrms, f=1kHz V_{OUT4}=2.5V, I_{OUT4}=150mA	–	40	–	dB
Dropout Voltage	ΔV_{IO4}	I_{OUT4}=200mA	–	0.2	0.3	V
		I_{OUT4}=200mA Ta=-40°C to +125°C	–	–	0.4	
Average Temperature Coefficient of Output Voltage	ΔV_{OUT4} /Ta	I_{OUT4}=150mA Ta=-20°C to +75°C	–	±50	–	ppm/°C
Enable Control Block (EN4)						
High Threshold Voltage	V_{THH_EN4}	V_{EN4}=L → H	1.0	–	5.5	V
		V_{EN4}=L → H Ta=-40°C to +125°C	1.0	–	5.5	
Low Threshold Voltage	V_{THL_EN4}	V_{EN4}=H → L	0	–	0.4	V
		V_{EN4}=H → L Ta=-40°C to +125°C	0	–	0.4	
Input Bias Current	I_{EN4}	V_{EN4}=3.3V	–	7	14	μA
		V_{EN4}=3.3V Ta=-40°C to +125°C	–	–	14	
Power Good Block (PG4)						
High Level Detection Reference Voltage	V_{THH_PG4}	Rising	0.836	–	0.924	V
		Rising, Ta=-40°C to +125°C	0.836	–	0.924	
Low Level Detection Reference Voltage	V_{THL_PG4}	Rising	0.745	–	0.775	V
		Rising, Ta=-40°C to +125°C	0.745	–	0.775	
Hysteresis Voltage	V_{HYS_PG4}		–	16	–	mV
Power Good ON Resistance	R_{ON_PG4}	I_{PG4}=10mA	–	100	–	Ω
Leak Current at OFF State	I_{LEAK_PG4}	V_{PG4}=5.5V	–	–	0.1	μA
		V_{PG4}=5.5V Ta=-40°C to +125°C	–	–	0.1	

■ ELECTRICAL CHARACTERISTICS

(Unless otherwise noted, V_{VIN1}=$V_{EN1/SYNC}$=12V, V_{VIN2}=V_{LDOVIN}=V_{EN2}=V_{EN3}=V_{EN4}=3.3V, R_T=6.8kΩ, Ta=25°C)

Common parameter

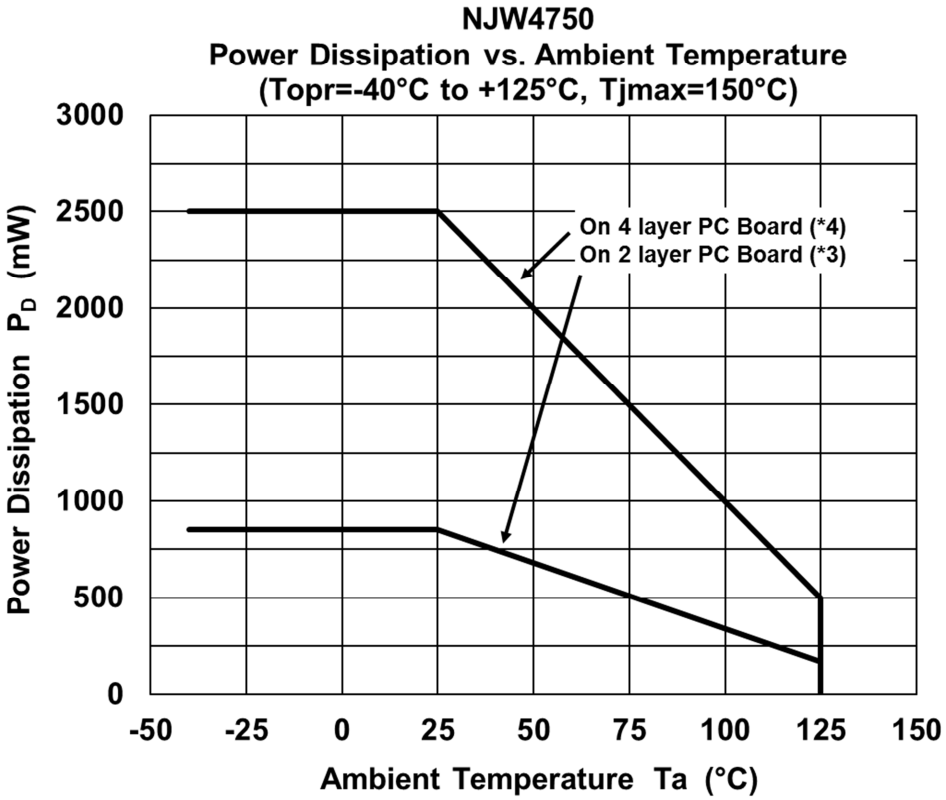
PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
General Characteristic						
Quiescent Current 1 (VIN1)	I_{DD1}	R_L=no load, V_{FB1}=0.9V	–	2.3	3.5	mA
		R_L=no load, V_{FB1}=0.9V Ta=-40°C to +125°C	–	–	3.5	
Quiescent Current 2 (VIN2)	I_{DD2}	R_L=no load V_{FB2}=0.9V, V_{FB3}=0.9V	–	2	3	mA
		R_L=no load V_{FB2}=0.9V, V_{FB3}=0.9V Ta=-40°C to +125°C	–	–	3	
Quiescent Current 3 (LDOVIN)	I_{DDLDO}	R_L=no load, V_{FB4}=0.9V	–	0.1	0.2	mA
		R_L=no load, V_{FB4}=0.9V Ta=-40°C to +125°C	–	–	0.2	
Standby Current 1 (VIN1)	I_{DD_STB1}	$V_{EN1/SYNC}$=0V V_{EN2}=0V V_{EN3}=0V V_{EN4}=0V	–	–	3	μA
		$V_{EN1/SYNC}$=0V V_{EN2}=0V V_{EN3}=0V V_{EN4}=0V Ta=-40°C to +125°C	–	–	6	
Standby Current 2 (VIN2)	I_{DD_STB2}	$V_{EN1/SYNC}$=0V V_{EN2}=0V V_{EN3}=0V V_{EN4}=0V	–	–	2	μA
		$V_{EN1/SYNC}$=0V V_{EN2}=0V V_{EN3}=0V V_{EN4}=0V Ta=-40°C to +125°C	–	–	4	
Standby Current 3 (LDOVIN)	I_{DD_STBLDO}	$V_{EN1/SYNC}$=0V V_{EN2}=0V V_{EN3}=0V V_{EN4}=0V	–	–	15	μA
		$V_{EN1/SYNC}$=0V V_{EN2}=0V V_{EN3}=0V V_{EN4}=0V Ta=-40°C to +125°C	–	–	20	

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-ambient Thermal resistance	θja	146.3(3) 50.5(4)	°C /W
Junction-to-Top of package Characterization parameter	ψjt	6.1(3) 0.8(4)	°C /W

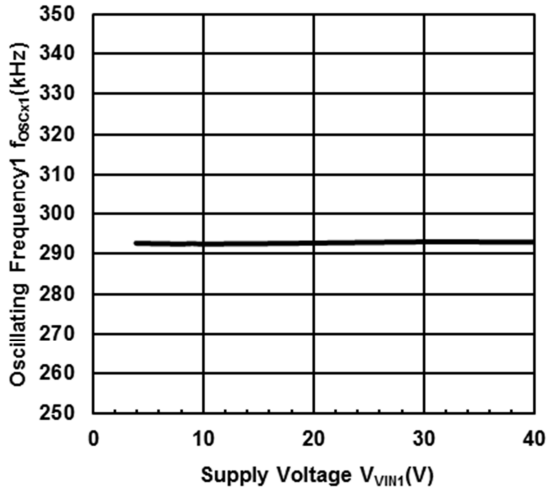
(3): Mounted on glass epoxy board.
(101.5×114.5×1.6mm:based on EIA/JEDEC standard,2layers, with Exposed Pad)
(4): Mounted on glass epoxy board.
(101.5×114.5×1.6mm:based on EIA/JEDEC standard,4layers, with Exposed Pad)
(For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via holes to a board based on JEDEC standard JESD51-5)

■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

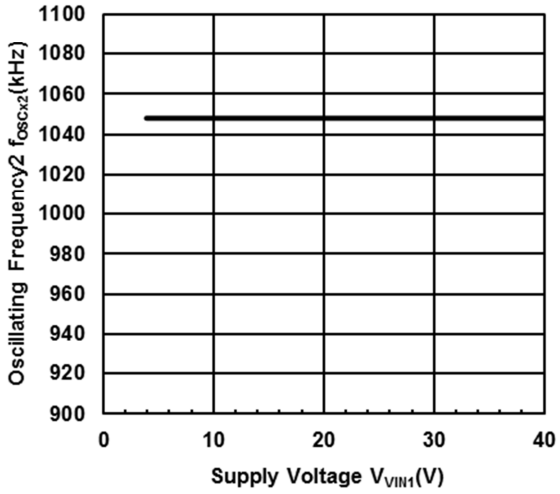


■ TYPICAL CHARACTERISTICS

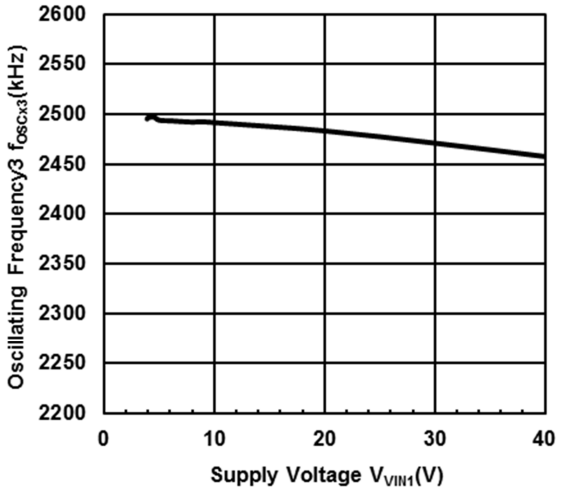
Oscillating Frequency1 vs. Supply Voltage
R_T=27kΩ, Ta=25℃



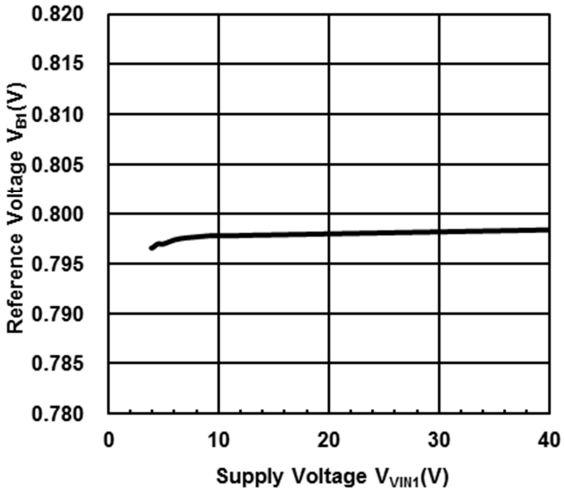
Oscillating Frequency2 vs. Supply Voltage
R_T=6.8kΩ, Ta=25℃



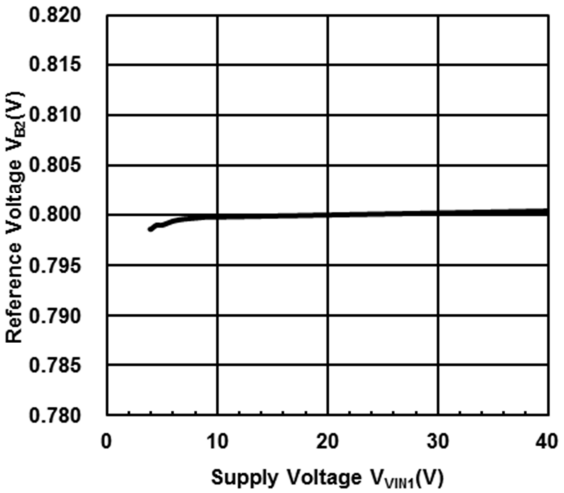
Oscillating Frequency3 vs. Supply Voltage
R_T=1.8kΩ, Ta=25℃



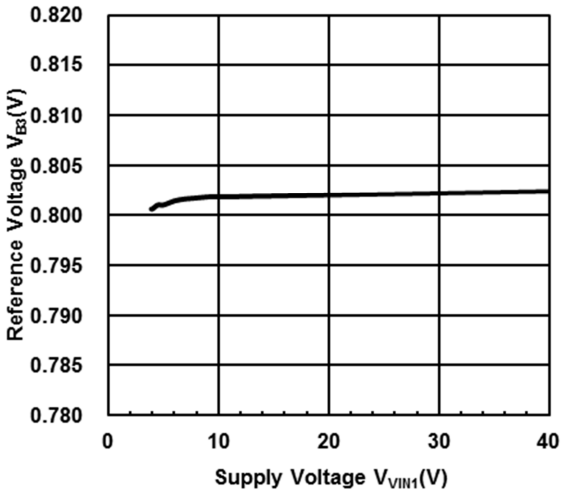
Ch.1 Reference Voltage vs. Supply Voltage
Ta=25℃



Ch.2 Reference Voltage vs. Supply Voltage
Ta=25℃

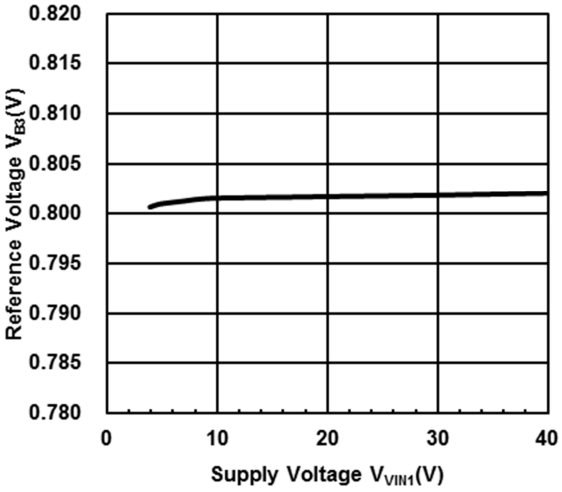


Ch.3 Reference Voltage vs. Supply Voltage
Ta=25℃, R_{MODE}=39kΩ

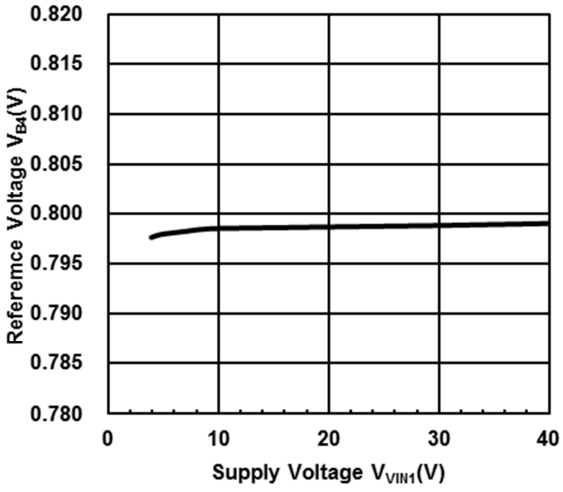


■ TYPICAL CHARACTERISTICS

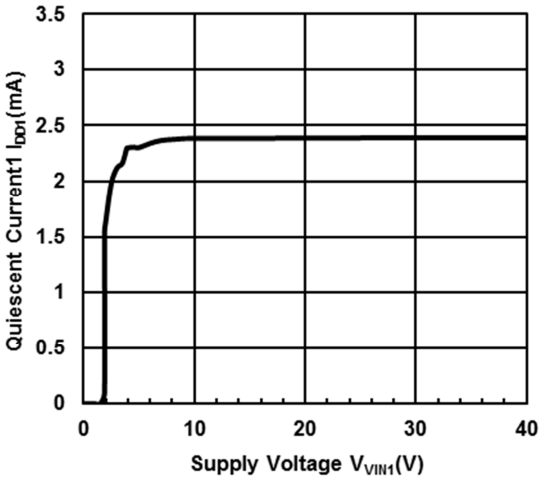
Ch.3 Reference Voltage vs. Supply Voltage
Ta=25℃, R_{MODE}=15kΩ,
V_O=1.8V(R1=36kΩ, R2=47kΩ)



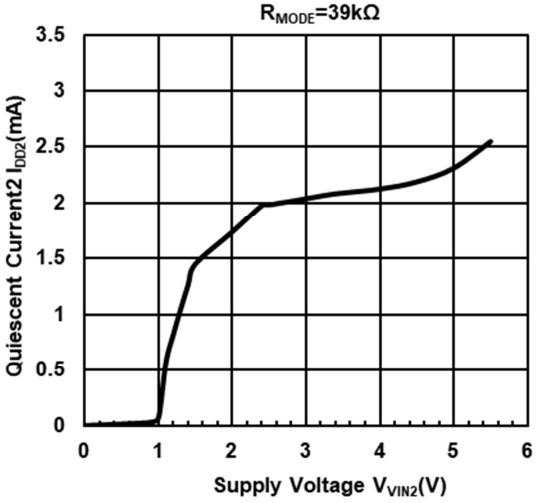
Ch.4 Reference Voltage vs. Supply Voltage
Ta=25℃, V_O=1.8V(R1=36kΩ, R2=47kΩ)



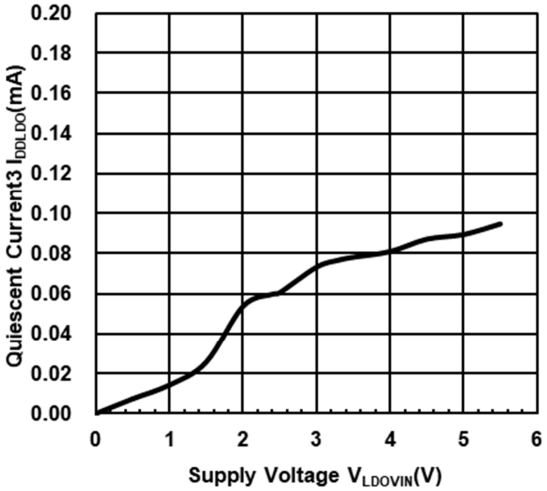
Quiescent Current1 vs. Supply Voltage
R_L=No Load, V_{FB1}=0.9V



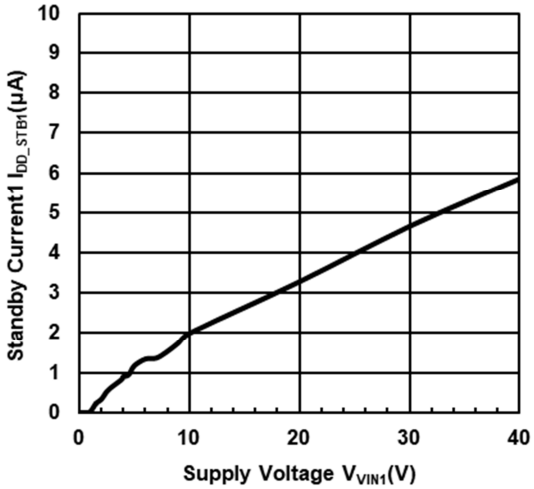
Quiescent Current2 vs. Supply Voltage
R_L=No Load, V_{FB2}=V_{FB3}=0.9V, EN2=EN3=3.3V,
R_{MODE}=39kΩ



Quiescent Current3 vs. Supply Voltage
R_LNo Load, V_{FB4}=0.9V

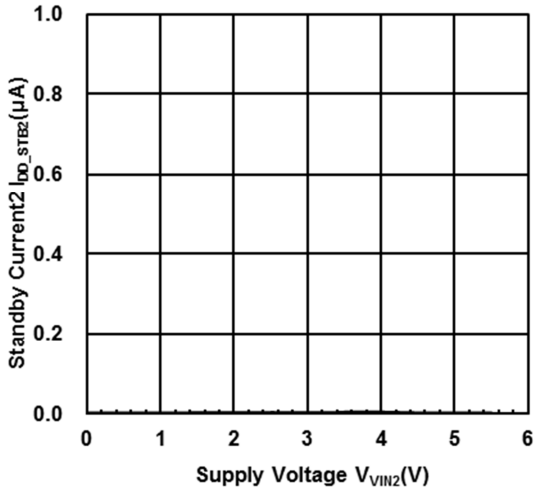


Standby Current1 vs. Supply Voltage
$V_{EN1/SYNC}$=V_{EN2}=V_{EN3}=V_{EN4}=0V

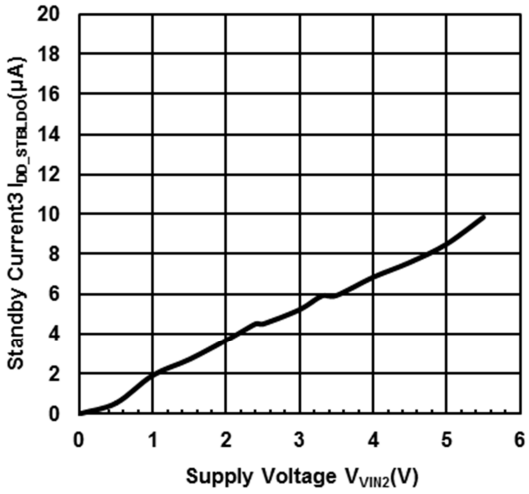


■ TYPICAL CHARACTERISTICS

Standby Current2 vs. Supply Voltage
V_{VIN1}=12V, $V_{EN1/SYNC}$=V_{EN2}=V_{EN3}=V_{EN4}=0V,
R_{MODE}=39kΩ

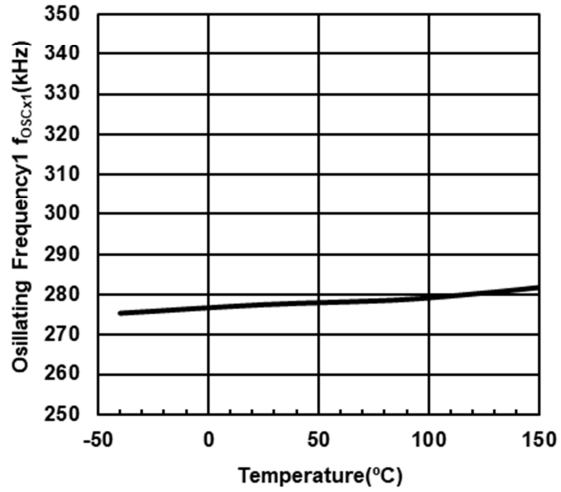


StandbyCurrent3 vs. Supply Voltage
V_{VIN1}=12V, $V_{EN1/SYNC}$=V_{EN2}=V_{EN3}=V_{EN4}=0V

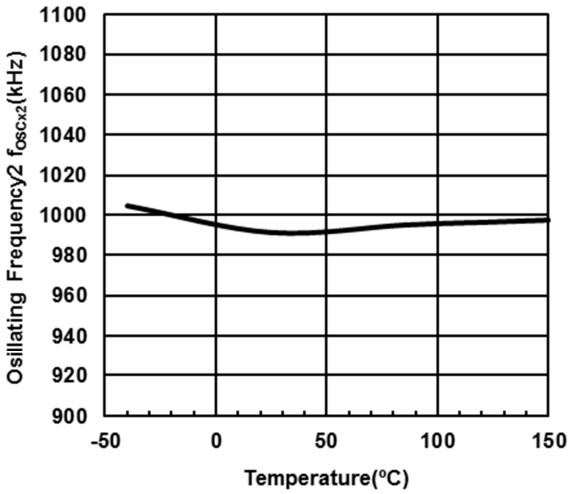


■ TYIPICAL CHARACTERISTICS

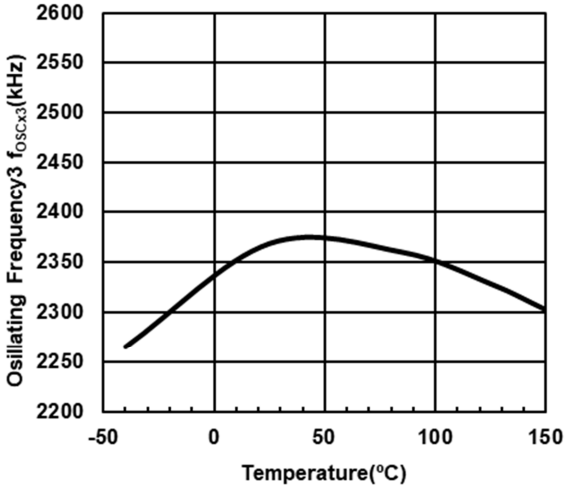
Oscillating Frequency1 vs. Temperature
V_{VIN1}=12V, R_T=27kΩ



Oscillating Frequency2 vs. Temperature
V_{VIN1}=12V, R_T=6.8kΩ

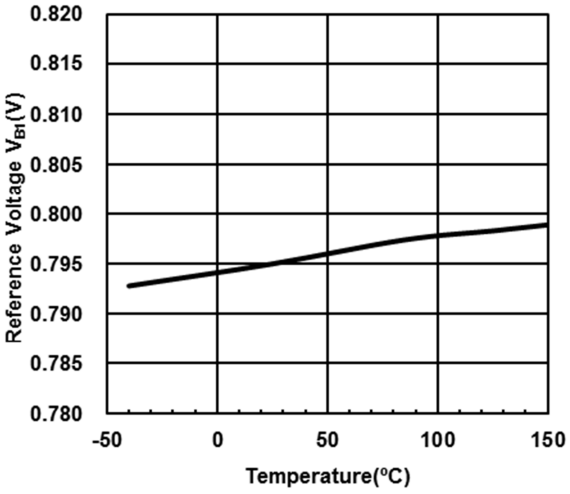


Oscillating Frequency3 vs. Temperature
V_{VIN1}=12V, R_T=1.8kΩ

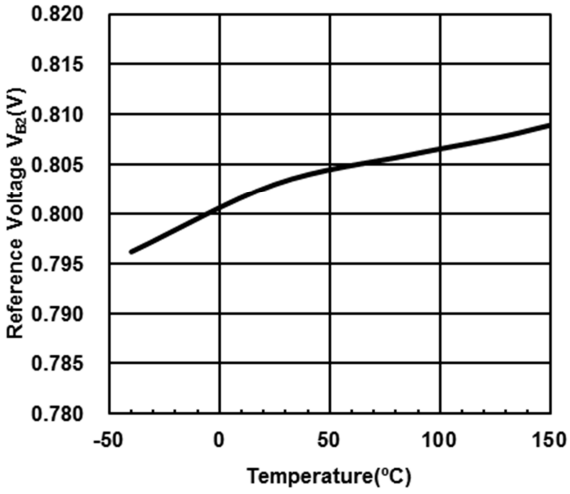


■ TYPICAL CHARACTERISTICS

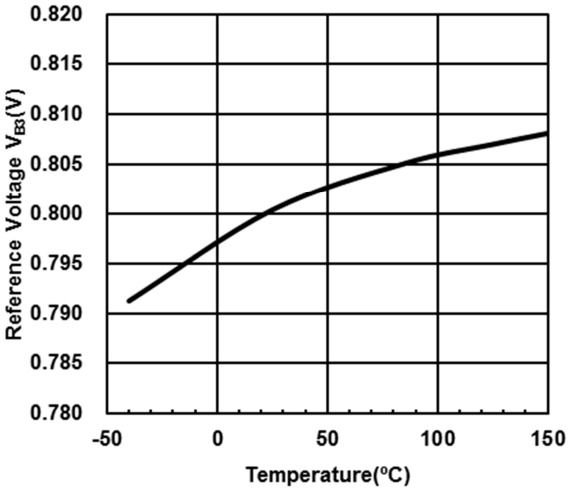
Ch.1 Reference Voltage vs. Temperature
V_{VIN1}=12V



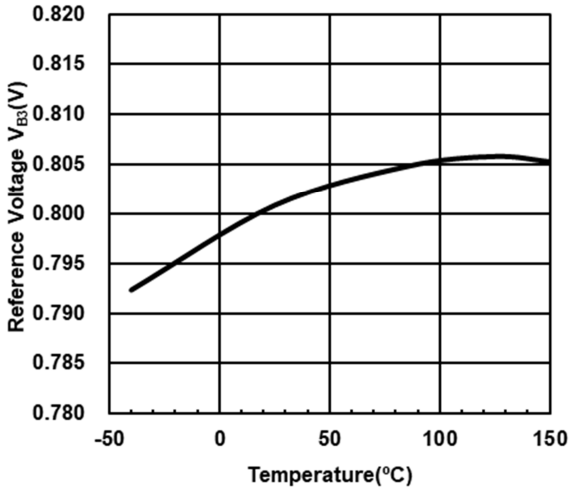
Ch.2 Reference Voltage vs. Temperature
V_{VIN1}=12V



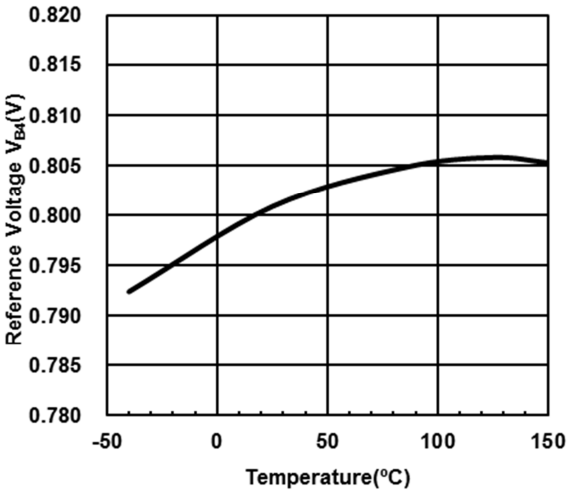
Ch.3 Reference Voltage vs. Temperature
V_{VIN1}=12V, R_{MODE}=39kΩ



Ch.3 Reference Voltage vs. Temperature
V_{VIN1}=12V, R_{MODE}=15kΩ

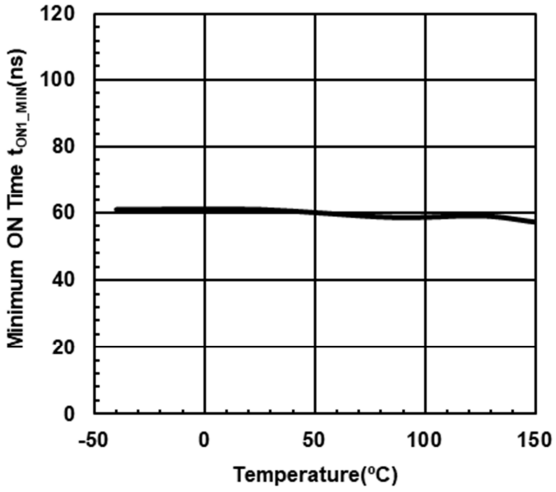


Ch.4 Reference Voltage vs. Temperature
V_{VIN1}=12V

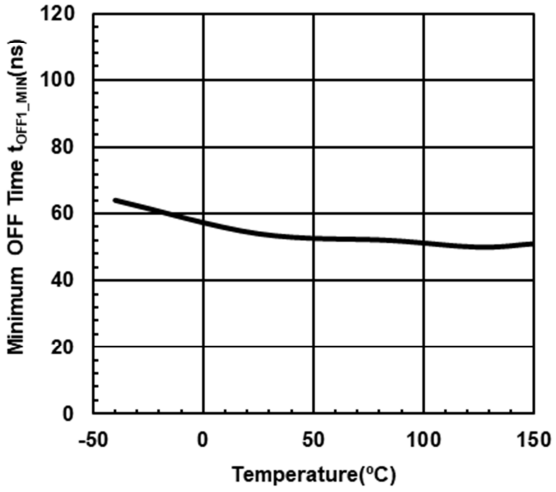


■ TYPICAL CHARACTERITICS

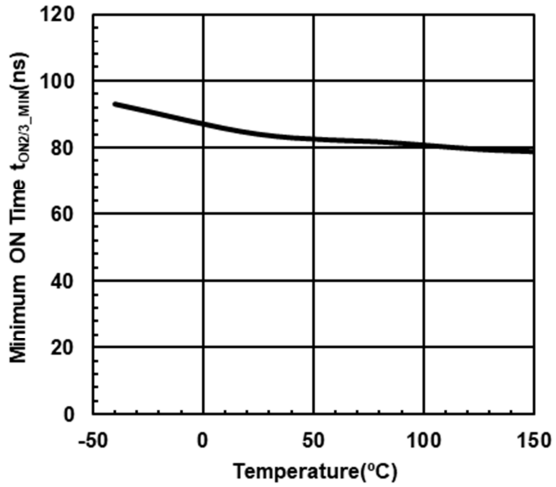
Ch.1 Minimum ON Time vs. Temperature
V_{VIN1}=12V



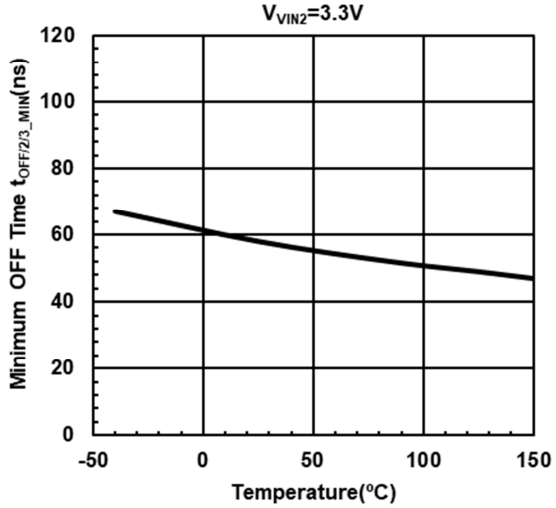
Ch.1 Minimum OFF Time vs. Temperature
V_{VIN1}=12V



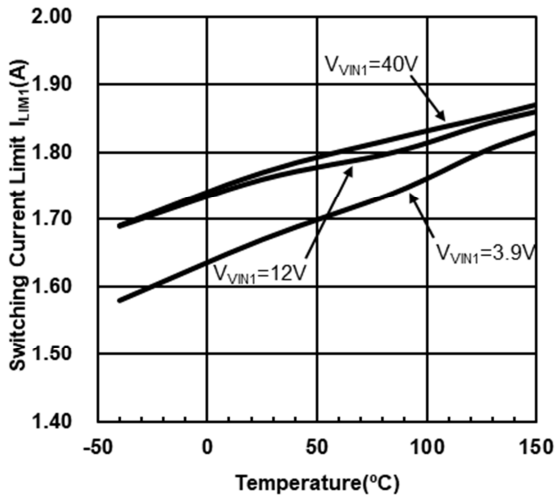
Ch.2/3 Minimum ON Time vs. Temperature
V_{VIN2}=3.3V



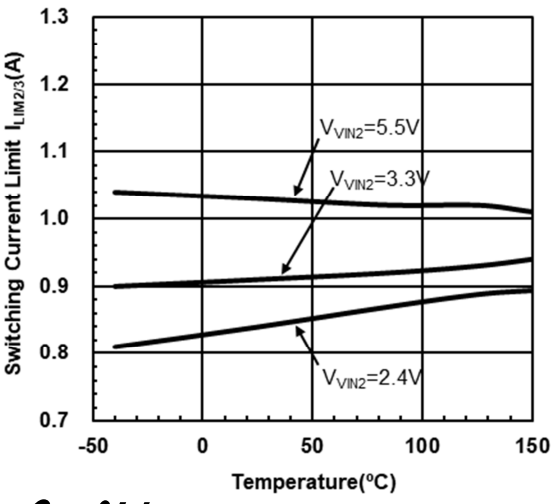
Ch.2/3 Minimum OFF Time vs. Temperature
V_{VIN2}=3.3V



Ch.1 Switching Current Limit vs. Temperature

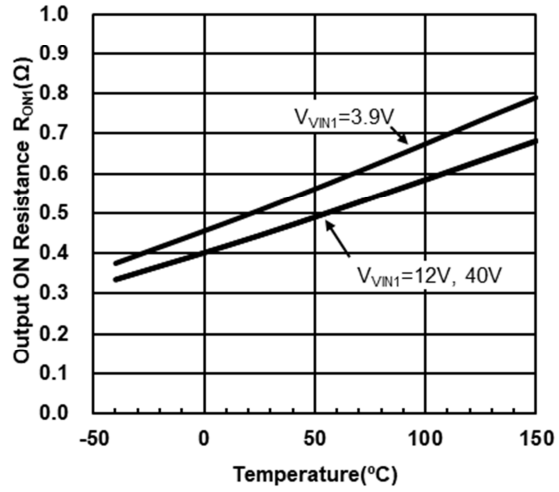


Ch.2/3 Switching Current Limit vs. Temperature

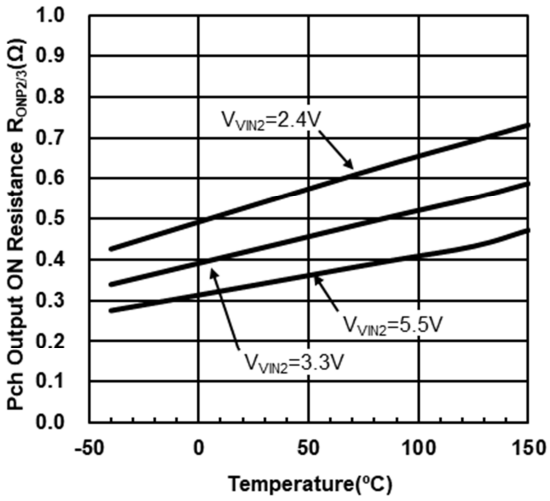


■ TYPICAL CHARACTERISTICS

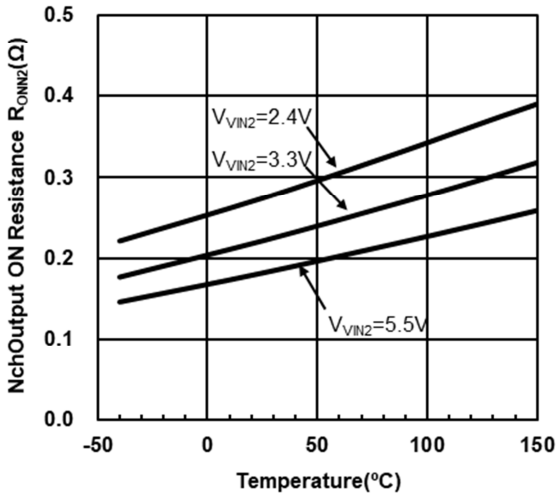
Ch.1 Output ON Resistance vs. Temperature
I_{SW1}=0.8A



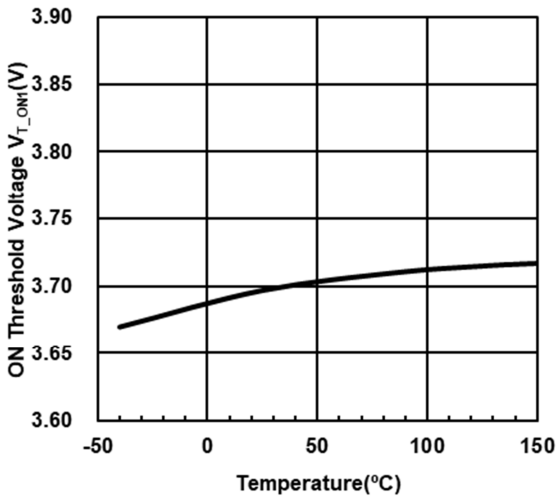
Ch.2/3 Pch Output ON Resistance vs. Temperature
$I_{SW2/3\ SOURCE}$=0.5A



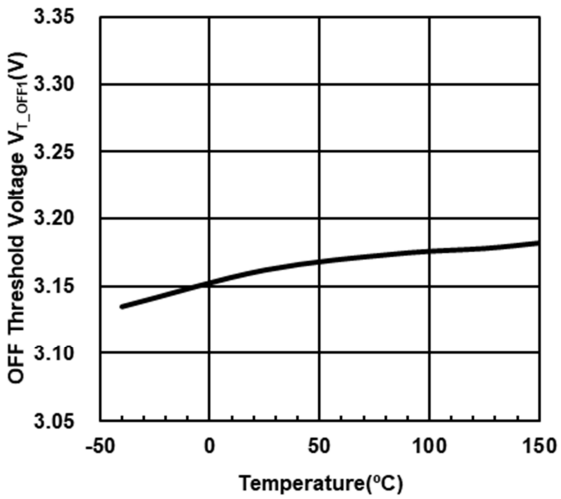
Ch.2/3 Nch Output ON Resistance vs. Temperature
$I_{SW2/3SINK}$=0.5A



Ch.1 ON Threshold Voltage vs. Temperature
V_{VIN1} L → H

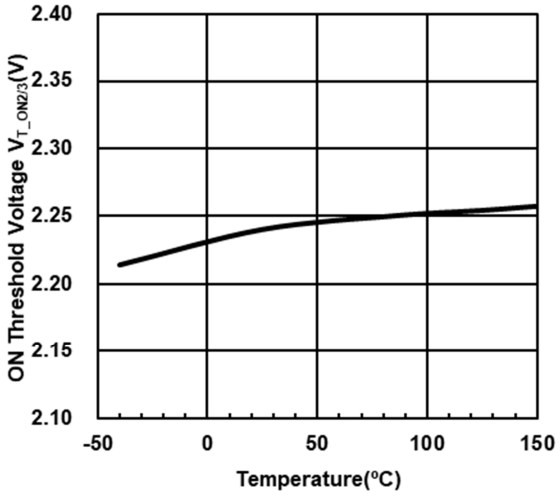


Ch1 OFF Threshold Voltage vs. Temperature
V_{VIN1} H → L

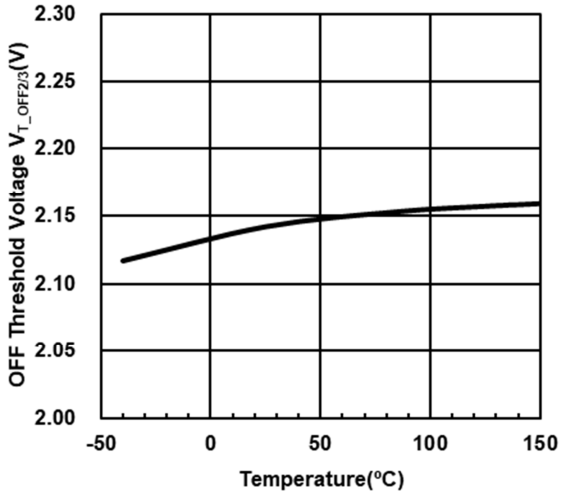


■ TYPICAL CHARACTERISTICS

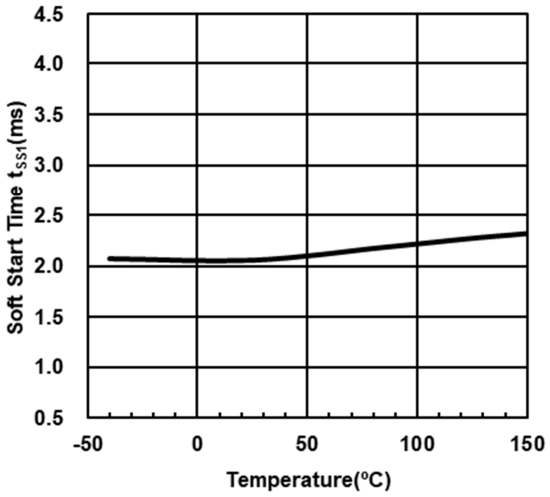
Ch.2/3 ON Threshold Voltage vs. Temperature
V_{VIN2} L → H



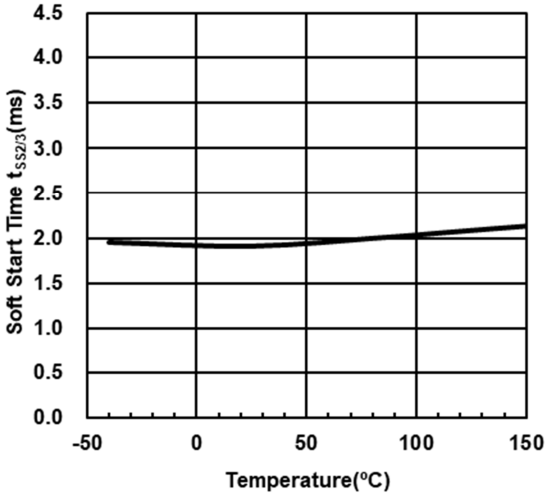
Ch.2/3 OFF Threshold Voltage vs. Temperature
V_{VIN2} H → L



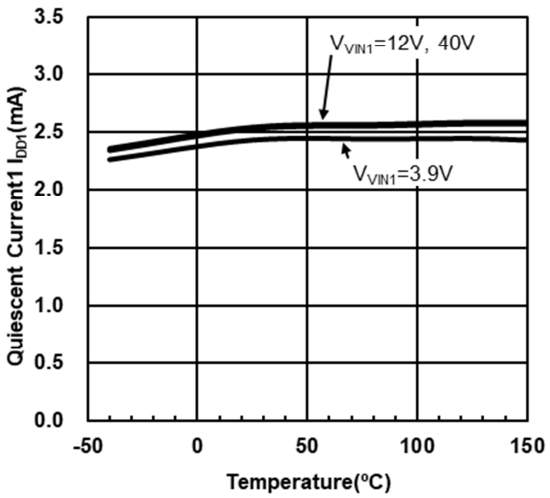
Ch.1 Soft Start Time vs. Temperature
V_{FB1}=0.75V



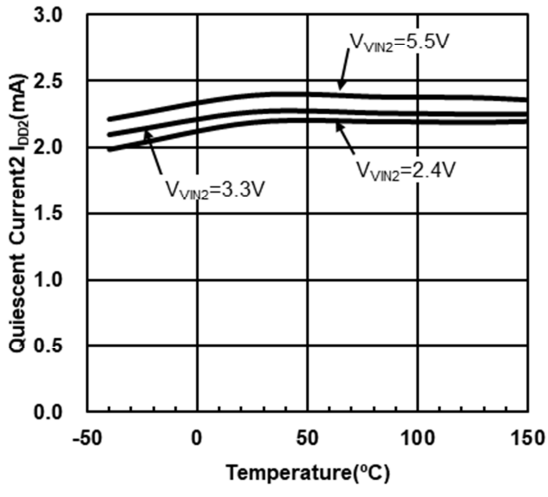
Ch.2/3 Soft Start Time vs. Temperature
V_{FB2}=0.75V



Quiescent Current1 vs Temperature
R_L=No Load, V_{FB1}=0.9V

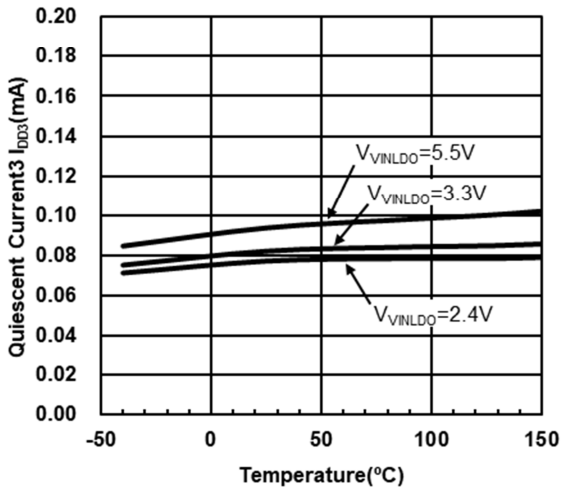


Quiescent Current2 vs. Temperature
R_L=No Load, V_{FB2}=V_{FB3}=0.9V, V_{EN2}=V_{EN3}=3.3V,
R_{MODE}=39kΩ

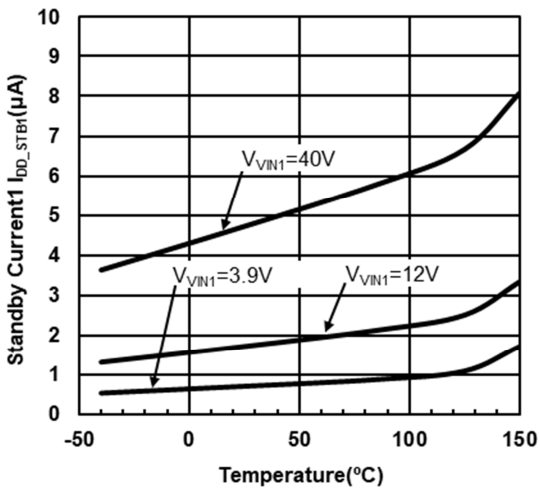


■ TYPICAL CHARACTERISTICS

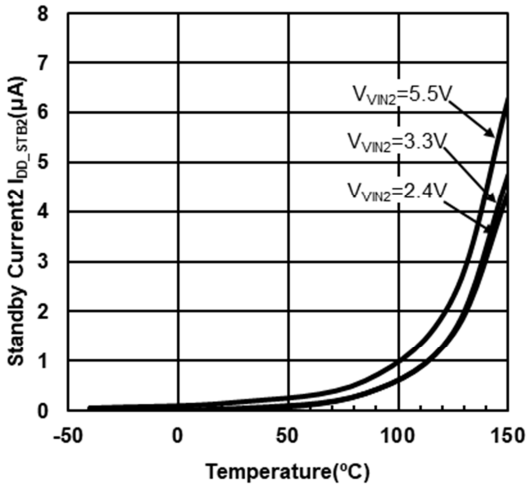
Quiescent Current3 vs. Temperature
R_L=No Load, V_{FB4}=0.9V



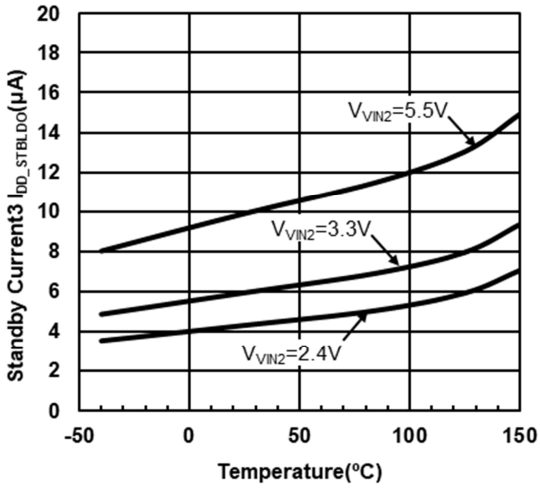
Standby Current1 vs. Temperature
$V_{EN1/SYNC}$=V_{EN2}=V_{EN3}=V_{EN4}=0V



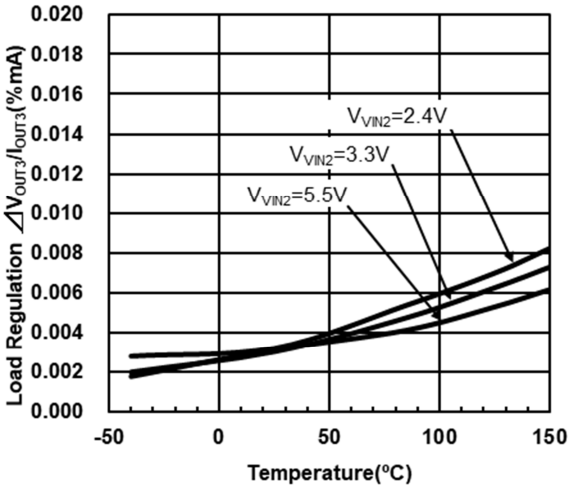
Standby Current2 vs. Temperature
V_{VIN1}=12V, $V_{EN1/SYNC}$=V_{EN2}=V_{EN3}=V_{EN4}=0V



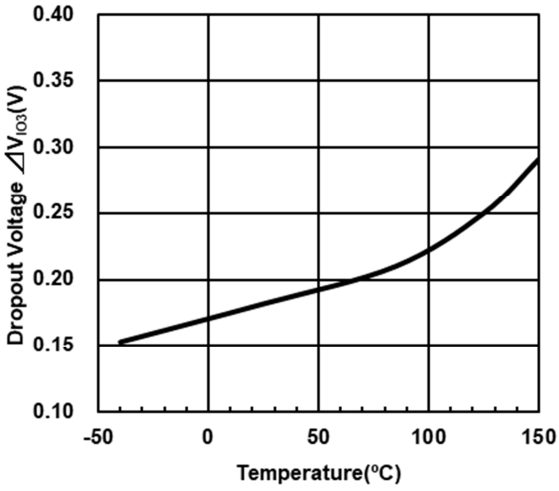
Standby Current3 vs. Temperature
V_{VIN1}=12V, $V_{EN1/SYNC}$=V_{EN2}=V_{EN3}=V_{EN4}=0V



Ch.3 Load Regulation vs. Temperature
I_{OUT3}=1mA to 200mA, R_{MODE}=Open or 15kΩ

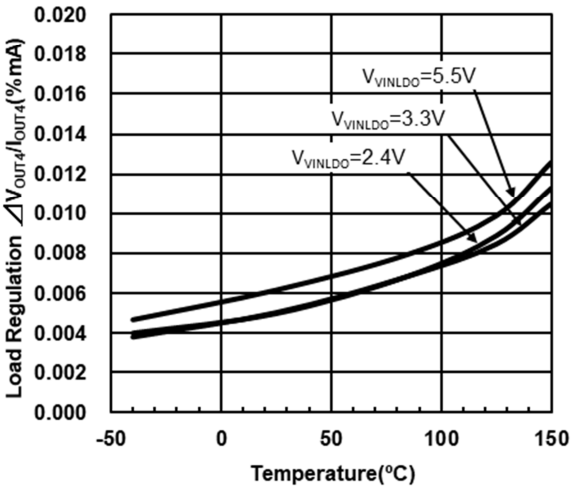


Ch.3 Dropout Voltage vs. Temperature
V_{IN2}=3.3V, I_{OUT3}=200mA

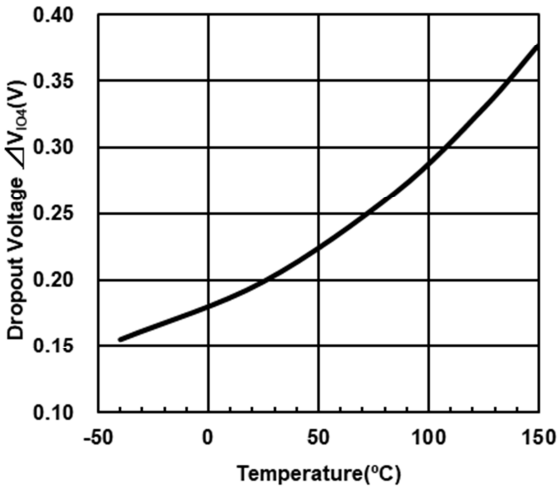


■ TYIPICAL CHARACTERISTICS

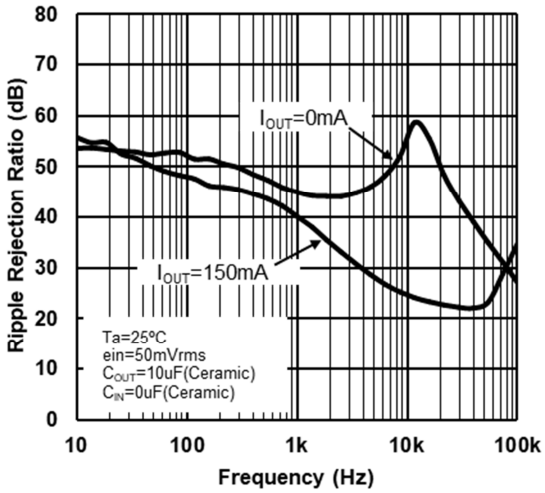
Ch.4 Load Regulation vs. Temperature
I_{OUT4}=1mA to 200mA



Ch.4 Dropout Voltage vs. Temperature
V_{INLDO}=3.3V, I_{OUT4}=200mA



Ch.3,4 RippleRejection vs Frequency
V_{OUT}=2.5V, V_{LDOVIN}=3.3V



■ INTRODUCTION

Please note the following when using NJW 4750.

- The NJW 4750 can operate each Ch. independently.
  However, even if Ch.1 is not used, it is necessary to input a power supply to VIN1 pin.
- Ch.3 (LDOMODE) and Ch.4 need to be start-up after power Ch. becomes active.
  The LDO may not be start-up by the protection function.
  e.g. The case of using Ch.1 as a power supply for Ch.4.
  It becomes the start of Ch.4 after normal start of Ch.1 by connecting PG1 pin of Ch.1 to EN4 pin of Ch.4.

■ PIN DESCRIPTION

PIN NO.	SYMBOL	DESCRIPTION
1	GND	Ground pin.
2	EN3	This pin controls the operation and stop of Ch.3. High Level: operation, Low level or Open level: Standby mode.
3	FB3	This pin detects the output voltage of Ch.3. The output voltage is divided and inputted so that the FB pin voltage becomes 0.8V same as the reference voltage.
4	NC	Non connection.
5	FB2	This pin detects the output voltage of Ch.2. The output voltage is divided and inputted so that the FB pin voltage becomes 0.8V same as the reference voltage.
6	EN2	This pin controls the operation and stop of Ch.2. High Level: operation, Low level or Open level: Standby mode.
7	RT	Oscillation frequency setting pin by Timing Resistor. Oscillating frequency should set between 280kHz and 2.4MHz.
8	GND	Ground pin.
9	PG1	Power-good output of Ch.1 configured with open drain.
10	MODE	This pin is used to determine the operation mode. Connect an open or mode setting resistor.
11	FB1	This pin detects the output voltage of Ch.1. The output voltage is divided and inputted so that the FB pin voltage becomes 0.8V same as the reference voltage.
12	EN1/SYNC	This pin controls the operation and stop of Ch.1. High Level: operation, Low level or Open level: Standby mode. By inputting the clock signal, it operates synchronized with the input signal.
13	VIN1	Power supply input for IC and Ch.1. Since the impedance of the power supply path needs to be lowered connecting a capacitor (C_{IN}) near the IC is required.
14	GND	Ground pin.
15	SW1	Ch.1 Output.
16	EN4	This pin controls the operation and stop of Ch.4. High Level: operation, Low level or Open level: Standby mode.
17	LDOVOUT	Ch.4 Output
18	FB4	This pin detects the output voltage of Ch.4. The output voltage is divided and inputted so that the FB pin voltage becomes 0.8V same as the reference voltage.
19	LDOVIN	Power supply input for Ch.4. Since the impedance of the power supply path needs to be lowered connecting a capacitor (C_{IN}) near the IC is required.
20	PG4	Power-good output of Ch.4 configured with open drain.
21	GND	Ground pin.
22	SW2	Ch.2 Output.
23	PG2	Power-good output of Ch.2 configured with open drain.
24	VIN2	Power supply input for Ch.2 and Ch.3. Since the impedance of the power supply path needs to be lowered connecting a capacitor (C_{IN}) near the IC is required.
25	PG3	Power-good output of Ch.3 configured with open drain.
26	SW3	Ch.3 Output.
Exposed PAD	-	Exposed PAD on backside should be connected to the ground and soldered to PCB.

■ DESCRIPTION OF BLOCK FEATURES

1. Mode setting

   By connecting the resistor between the MODE pin and GND, the operation mode of Ch.3 and protection type of OCP are selected.(Table 1)

   Table 1 The NJW4750 operation mode and setting resistor value.

MODE	Setting resistor R_{MODE} (±5%)		Ch.3	OCP Mode	MODE Pin Output Voltage (±5%)
	Min	Max			
1	open		LDO	Latch	2.5V
2	82kΩ	110kΩ	SW reg.	Latch	1.4V
3	27kΩ	39kΩ	SW reg.	Hiccup(SW) Foldback(LDO)	1.2V
4	6.8kΩ	15kΩ	LDO	Hiccup(SW) Foldback(LDO)	1.0V

   The mode setting can be set only at startup, and the state of the mode can be checked by pin voltage.

2. Basic functions of switching regulator. (Ch.1,2 and Ch.3)

   • Error Amplifier Section (Error AMP)

   0.8V±1% precise reference voltage is connected to the non-inverted input of this section.

   The output voltage can be set by dividing the output of the converter and connecting to the inverted input (FB pin).

   • PWM comparator section (PWM), oscillating circuit Section (OSC)

   Oscillating frequency can be set by inserting resistor between the RT pin and GND.

   Table 2 shows example of oscillating frequency and timing resistor. The resistance is adapted to a series of E24 and a series of E96.

   Please set the oscillating frequency according to Table 2

   Table 2 The NJW4750 oscillating frequency and timing resistor value

Oscillating Frequency (kHz)	Timing Resistor (kΩ)	Oscillating Frequency (kHz)	Timing Resistor (kΩ)
280	27	1200	5.6
380	20	1750	3.9
500	15	2000	3.0
700	10	2250	2.0
1000	6.8	2400	1.8

   NJW4750 is limited in minimum ON time and minimum OFF time, refer to electrical characteristics.

   Maximum duty cycle is 100%.

   When you design the application, please refer to "Application information - Oscillating frequency setting".

■ **DESCRIPTION OF BLOCK FEATURES (Continued)**

• Power MOSFET

The power is stored in the inductor by the switch operation of built-in power MOSFET. The switching current is limited by the overcurrent protection function.

• Power supply, GND pin（VIN、GND）

Current flows into the IC according to drive frequency in a switching element. When impedance of a power supply line is high, power supply will be unstably, and the performance of the IC can't be drawn out sufficiently.
Therefore, since the impedance of the power supply path needs to be lowered connecting a capacitor (C_{IN}) near the IC is required.

3. Additional and protection functions of switching regulator. (Ch.1,2 and Ch.3 are similar)

• Under voltage lockout (UVLO)

The UVLO circuit stops the IC operation in a low power supply voltage case, and when a power supply voltage becomes higher voltage than threshold, then the IC operation starts.
The threshold voltage has a hysteresis voltage width at rising and falling. A flutter of detection and release of UVLO is prevented by it.

• Soft start function

The output voltage of the converter gradually rises to a set value by the soft start function. The soft start time is 4ms (max.). It is defined with the time of the error amplifier reference voltage becoming from 0V to 0.75V.(Fig.1)
Soft start operating condition.

- Ch.1: $V_{VIN1} \geqq V_{T\_ON1}$、$V_{EN1} \geqq V_{THH\_EN1}$
- Ch.2: $V_{VIN1} \geqq V_{T\_ON1}$、$V_{VIN2} \geqq V_{T\_ON2}$、$V_{EN2} \geqq V_{THH\_EN2}$
- Ch.3: $V_{VIN1} \geqq V_{T\_ON1}$、$V_{VIN2} \geqq V_{T\_ON2}$、$V_{EN3} \geqq V_{THH\_EN3}$

Also thermal shutdown must be disabled.

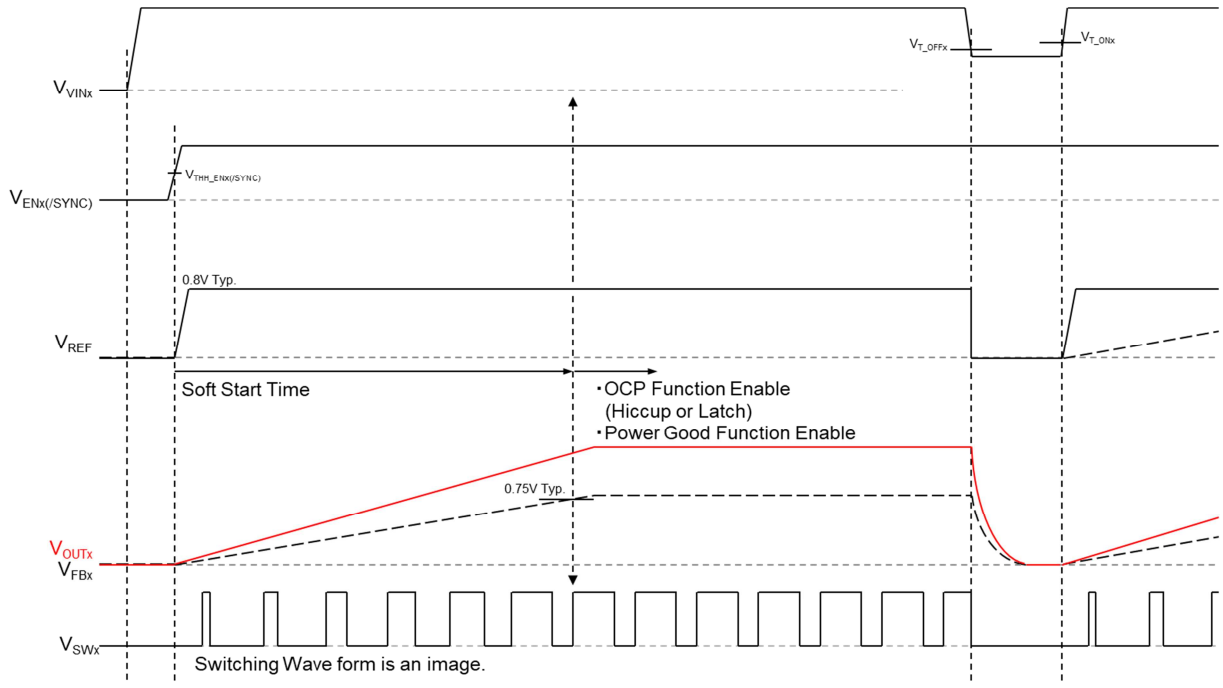


Fig.1 Soft start timing chart

■ DESCRIPTION OF BLOCK FEATURES (Continued)

- Over current protection circuit (OCP) (Ch.1,2 and Ch.3 are similar)
  Switching regulator block of NJW4750 has 2 kinds of overcurrent protection function.
  1. Hiccup (Fig.2):
     Switching operation is reduced and output is restricted. When the load state normally returns, it is reset automatically.
  2. Latch (Fig.3):
     The function as the power supply is suspended.
     Latch is released by setting all EN pin to Low or VIN1 pin to 0 V.

  ※ Hiccup system is each Ch. Independent control. Latch system suspends all output of IC.

  Operating condition of OCP
  In the soft start operating, Hiccup/Latch becomes ineffective.
  The overcurrent protection function operates when one of them of 2 conditions was formed.
  • $V_{FBx} \leq 0.4V$ and 7cycle over current detection continuously.
  • Overcurrent detection continuously of 1/fosc×240 s.

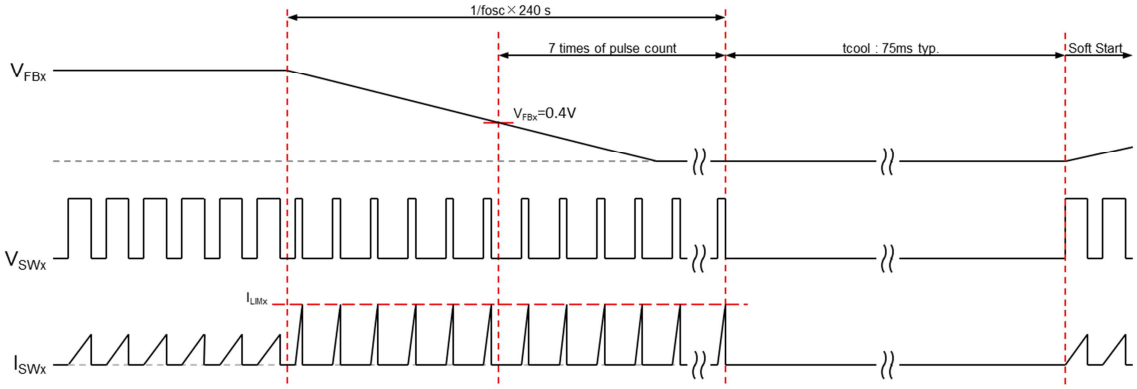


Fig.2 Hiccup mode OCP timing chart

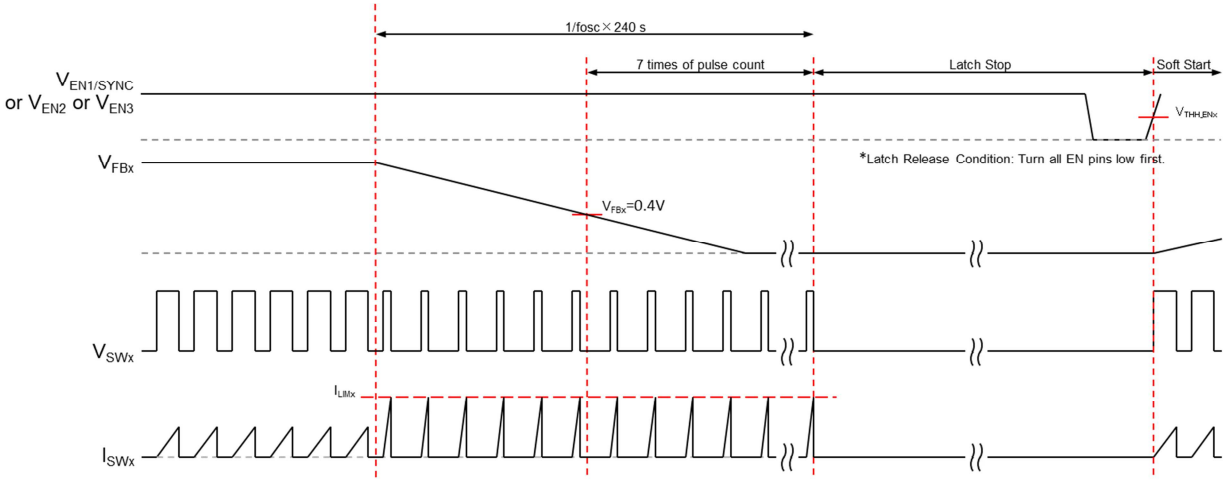


Fig.3 Latch mode OCP timing chart

■ DESCRIPTION OF BLOCK FEATURES (Continued)

• External clock synchronization (Ch.1,2 and Ch.3)

By inputting a square wave to EN1/SYNC pin, the oscillator of NJW4750 can be synchronized to an external frequency.

The input square wave must be on the following specification. (Table 3)

Table 3 The input square wave to EN1/SYNC pin.

	Condition
Input Frequency	f_{OSC}×0.9 to f_{OSC}×1.7 Upper limit 2,800kHz
Duty Cycle	40% to 60%
Voltage Magnitude	1.6V or more (High level) 0.4V or less (Low level)

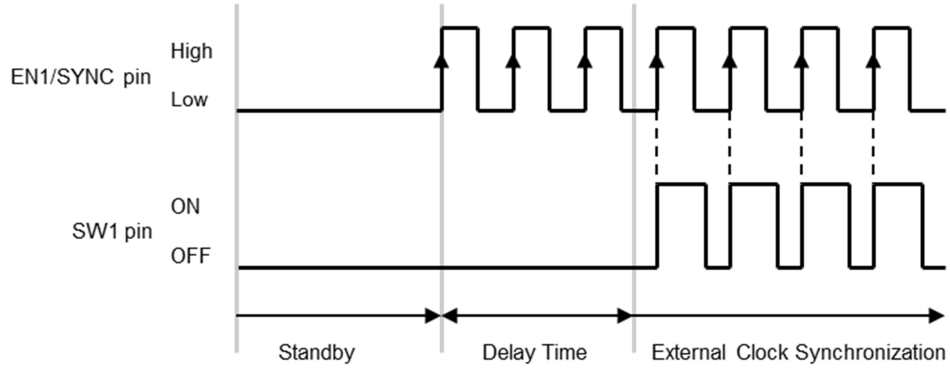


Fig.4 Switching operation by external synchronized clock

■ **DESCRIPTION OF BLOCK FEATURES (Continued)**

4. Basic functions of LDO (Ch.3 LDO MODE and Ch.4)
   • Error amplifier section (Error AMP)
   0.8V±1% precise reference voltage is connected to the non-inverted input of this section.
   The output voltage can be set by dividing the output of the converter and connecting to the inverted input (FB pin).

5. Additional and protection functions of LDO (Ch.3 LDO MODE and Ch.4)
   • Over current protection circuit(OCP)
   LDO block of NJW4750 can choose 2 kinds of overcurrent protection function.
   1. Fold back:
      Limits the output current as the output voltage decreases.
   2. Latch:
      The function as the power supply is suspended at $V_{FBx} \leq 0.4V$.
      Latch is released by setting all EN pin to Low or VIN1 pin to 0V.
   ※ Fold back system is independent each Ch. Latch system suspends all output of IC.

6. Common protection function / features
   • Thermal shutdown function (TSD)
   When junction temperature of the NJW4750 exceeds the 160°C*, internal thermal shutdown circuit function stops SW function. When junction temperature decreases to 145°C* or less, SW operation re-start from the soft start operation. The purpose of this function is to prevent malfunctioning of IC at the high junction temperature. Therefore it is not something that urges positive use. Please make sure to operate within the junction temperature range rated (-40°C to 150°C). (* Design value)

   • Standby function
   Each Ch. stops the operating and becomes standby status when the ENx(/SYNC) pin becomes less than 0.4V. The ENx(/SYNC) pins are internally pulled down with resistor (CH1 :5MΩ、CH2 :500kΩ、CH3 :500kΩ、CH4 :500kΩ), therefore the NJW4750 becomes standby mode when it is OPEN. Please connect this pin to VINx when you do not use standby function.

■ DESCRIPTION OF BLOCK FEATURES (Continued)

• Power Good function

It monitors the output status and outputs a signal from PGx pin that is internally connected to an open drain of MOSFET.

If the FB pin is within the range of -7% to + 15% of the error amplifier reference voltage, the PG pin becomes high impedance and notifies that the output voltage is normal. Otherwise the PG pin becomes low level and tells the output voltage is abnormal.

After soft start time, the Power Good function becomes effective in Ch.1, Ch.2, and Ch.3.

The Power Good function of Ch.4 becomes effective after passage for 150µs from EN4: H(@LDOVIN=3.3V).

When ENx pin control is performed by PGx pin, consider the input resistance value of ENx pin.

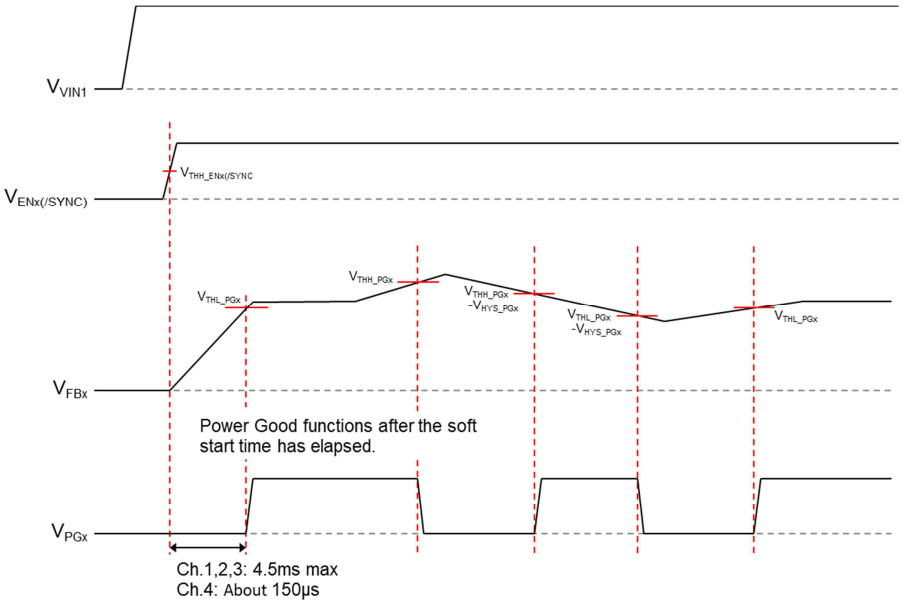


Fig.5 Power Good function timing chart

• Latch mode: added 1/fosc×40000 s delay in the last boot Ch.

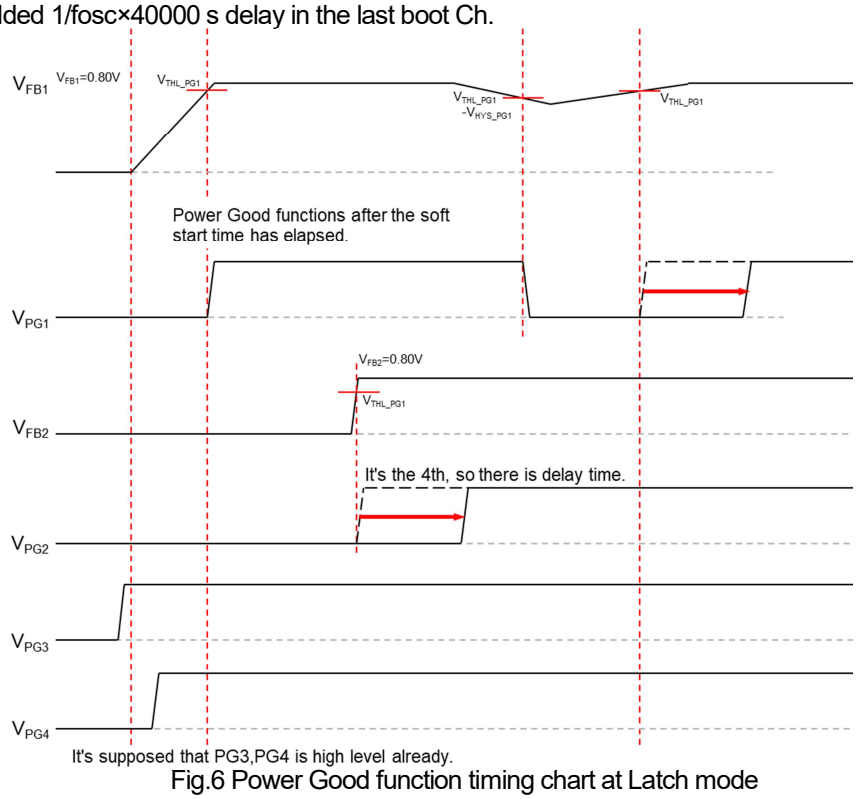


Fig.6 Power Good function timing chart at Latch mode

■ APPLICATION INFORMATION(Switching regulator)

• Oscillating frequency setting

When a switching frequency is high, a small inductor and capacitor are available.

If oscillating frequency is high, decrease in efficiency and a limit of the minimum ON time and minimum OFF time are demerit.

The buck converter of ON time and OFF time is decided the following formula.

$$t_{ON}=\frac{(V_{OUT}+V_L)}{(V_{IN}-V_{SWH}+V_L)\times f_{OSC}}[s]$$

$$t_{OFF}=\frac{1}{f_{OSC}}-t_{ON}[s]$$

V_{IN} : Input voltage

V_{OUT} : Output voltage

V_{SWH} : High-side saturation voltage

V_L : Catch Diode V_f or Lo-side saturation voltage V_{SWL}

When the ON time becomes shorter than $t_{ON\text{-}MIN}$ or OFF time becomes shorter than $t_{OFF\text{-}MIN}$, a change of duty or pulse skip operation may be performed in order to maintain output voltage at a stable state.

• Inductors

Since a large current flows into an inductor, please select an appropriate inductor such as not saturate in the application.

Inductors have an important role in slope compensation.

Inductor value is limited selection by supply voltage and oscillation frequency. Recommended selection of the inductor value is between Hlim. and Llim. shown in Fig.8.

The maximum Output current of worst condition is decided the following formula.

$$\Delta I_L=\frac{(V_{IN}-V_{OUT})\times V_{OUT}}{L\times V_{IN}\times f_{OSC}}[A]$$

$$I_{OUT}=I_{LIMx(MIN)}-\frac{\Delta I_L}{2}[A]$$

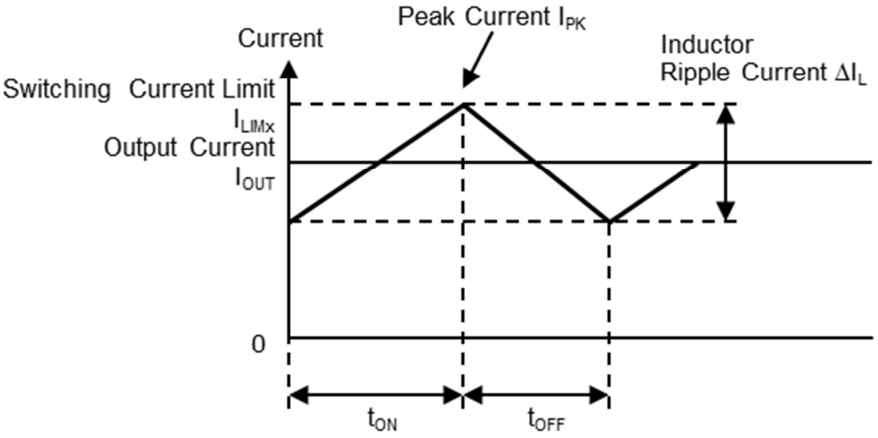


Fig.7 Inductor current state transition (Continuous conduction mode)

■ APPLICATION INFORMATION(Switching regulator)

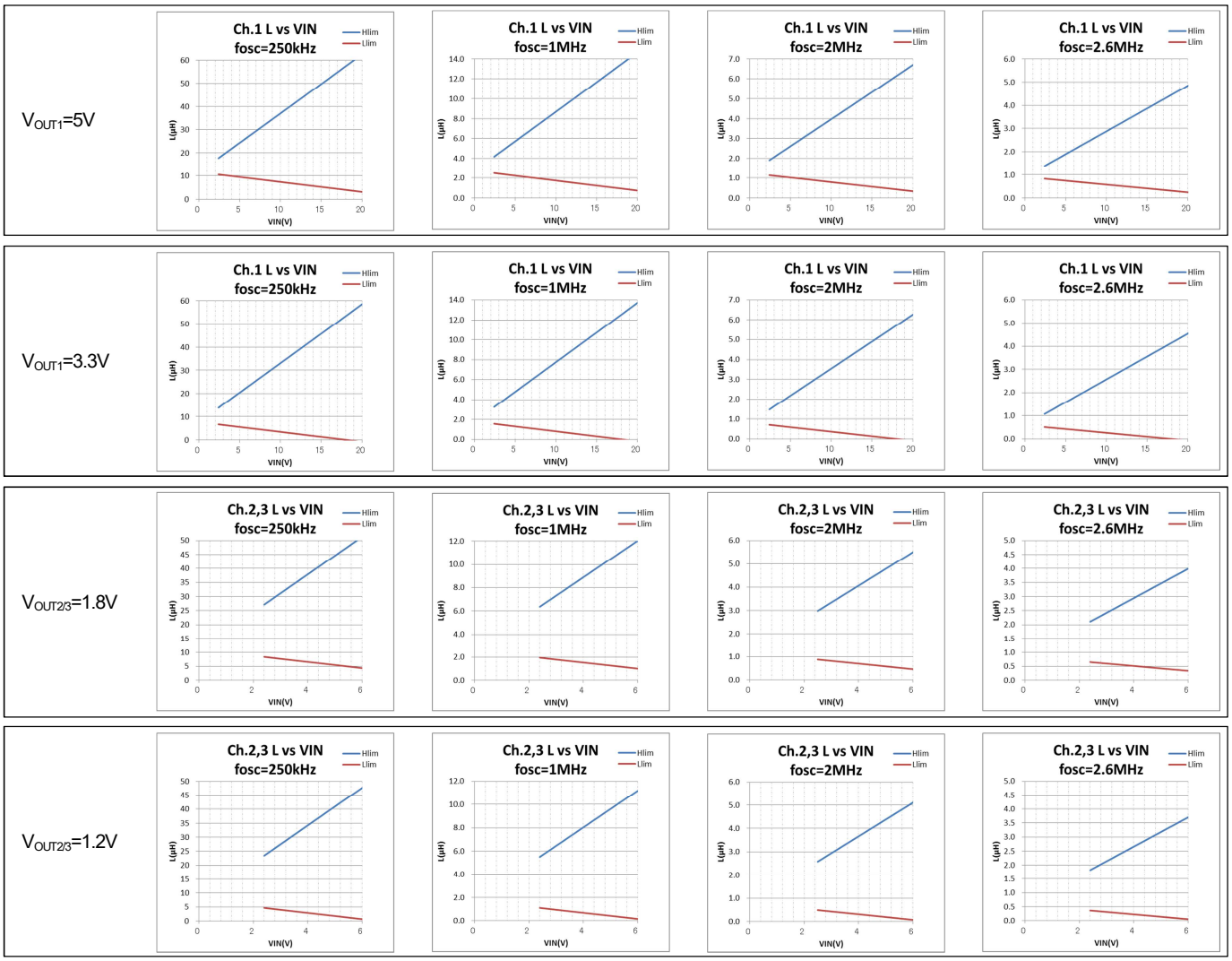


Fig.8 Inductance range.

• Input capacitor

Transient current which is responsive to frequency flows into the input section of a switching regulator. When impedance of a power supply line is high, power supply will be unstably, and the performance of the IC can't be drawn out sufficiently.

Therefore, since the impedance of the power supply path needs to be lowered connecting a capacitor (C_{IN}) near the IC is required.

The effective input current can be expressed by the following formula.

$$I_{RMS}=I_{OUT}\times\frac{\sqrt{V_{OUT}\times(V_{IN}-V_{OUT})}}{V_{IN}}[A_{rms}]$$

In the above formula, the maximum current is obtained when $V_{IN}=2\times V_{OUT}$, and the result in this case is $I_{RMS}=I_{OUT(MAX)}\div 2$. When the input capacitor in selecting, please carry out an evaluation based on an application, and decide a capacitor value that has adequate margin.

■ APPLICATION INFORMATION(Switching regulator)

• Output capacitor

An output capacitor stores power from the inductor, and stabilizes voltage provided to the output.
The NJW4750 is designed phase compensation so that output capacitor of low ESR can be used. Therefore a ceramic capacitor is the most suitable.
Since capacity of a ceramic capacitor may decline by DC supply voltage and temperature change, please confirm it's characteristics on specification sheet.
When selecting an output capacitor, must be considered Equivalent Series Resistance (ESR) characteristics, ripple current, and breakdown voltage.
In case of using a low ESR capacitor, it's possible to lower the ripple voltage.

The output ripple noise can be expressed by the following formula.

$$V_{ripple(p-p)}=\Delta I_L \times \left(ESR+\frac{1}{8\times f_{OSC}\times C_{OUT}}\right)[V]$$

The effective ripple current that flows in a capacitor (I_{RMS}) is obtained by the following equation.

$$I_{RMS}=\frac{\Delta I_L}{2\sqrt{3}}[A_{rms}]$$

• Setting of phase compensation

The NJW 4750 has a built-in phase compensation circuit.
Table 4 shows the values of extern al parts based on oscillation frequency and output voltage.

Table 4 Value of phase compensation

f_{OSC}	V_{OUT}	C_{OUT}	C_{FB}	R_{FB}	R2
1MHz or more	2.5V, 2.8V, 3.3V, 3.6V, 5V	10µF or more	22pF	1kΩ	30kΩ to 82kΩ
	1.8V	22µF or more	22pF	1kΩ	30kΩ to 82kΩ
	1.1V*, 1.2V*	47µF or more	22pF	1kΩ	30kΩ to 82kΩ
500kHz or less	ALL	100µF or more	open	open	30kΩ to 82kΩ

* V_{VIN2} is 4 V or less.
If V_{VIN2} is set to higher than 4 V, the oscillating frequency is limited up to 1.5MHz.

■ APPLICATION INFORMATION(Switching regulator)

• Catch diode

When the switch element is in OFF cycle, the power stored in the inductor flows to the output capacitor via the catch diode. Therefore an electric current according to the load current flows to the diode every cycle. Since a diode's forward saturation voltage and current accumulation cause power loss, a Schottky Barrier Diode (SBD), which has a low forward saturation voltage, is most suitable.

When select the SBD, the reverse current at the high temperature is important, too.

The characteristic of SBD has a high reverse current than a general diode. If the reverse current is large, it leads to the loss of the diode, so check the specification of the SBD

• Setting output voltage

The output voltage V_{OUT} is determined by the relative resistances of R1, R2.

$$V_{OUT}=\left(\frac{R2}{R1}+1\right)\times V_B[V]$$

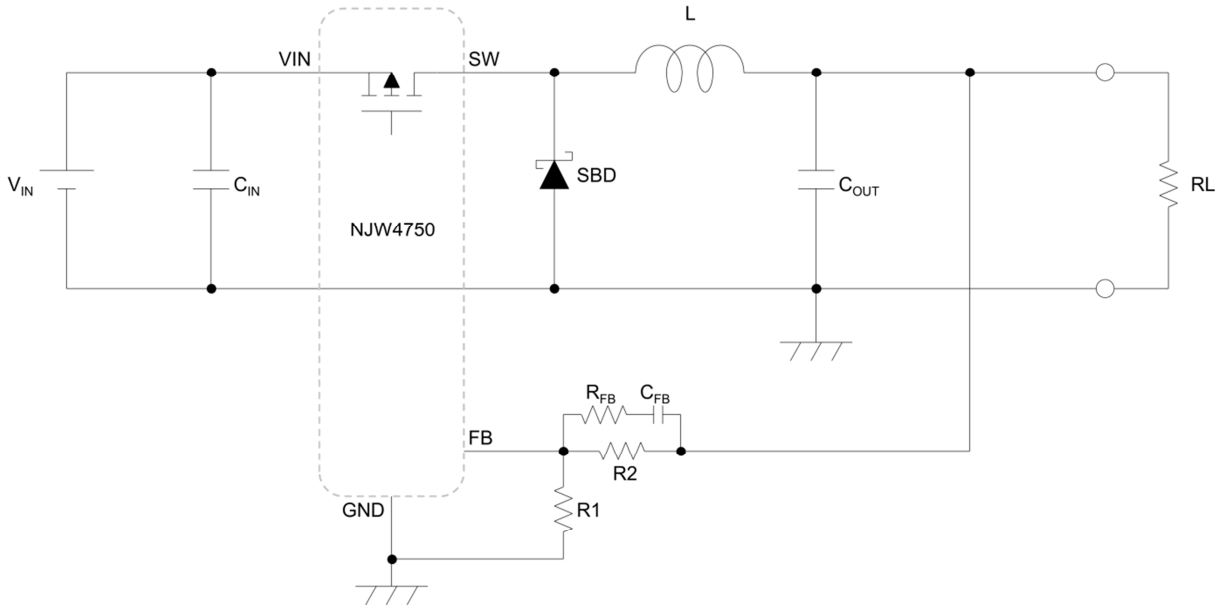


Fig.9 Output voltage setting

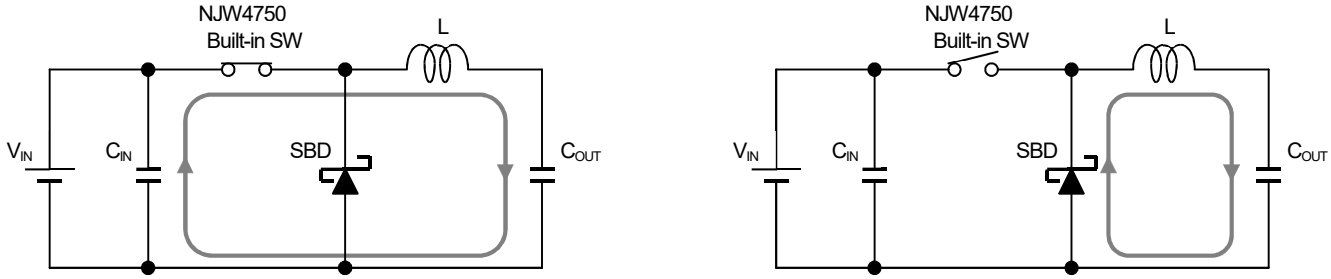
■ APPLICATION INFORMATION(Switching regulator)

• Board layout

In the switching regulator application, since the current flow according to the oscillating frequency, the substrate (PCB) layout is very important.

Therefore, a current flowing line must be wide and short as much as possible. Fig.10 shows a current loop of a step-down converter. (In case of synchronous rectification, SBD is changed to built-in SW.)

Especially, the loop of C_{IN} - SW - SBD which has a high frequency switching, is necessary to configure minimum loop as top priority. It is effective in reducing of spike noise caused by parasitic inductor.



(a) Buck converter SW ON (b) Buck converter SW OFF

Fig.10 Current loop of buck converter

About concerning the GND, it is preferred to separate the power GND and the signal GND, and use single ground point.

The voltage sensing feedback line should be away as far away as possible from the inductor. Since this line has high impedance, it is laid out to avoid the influence noise caused by leakage flux from the inductor.

Fig.11 shows example of wiring at buck converter.

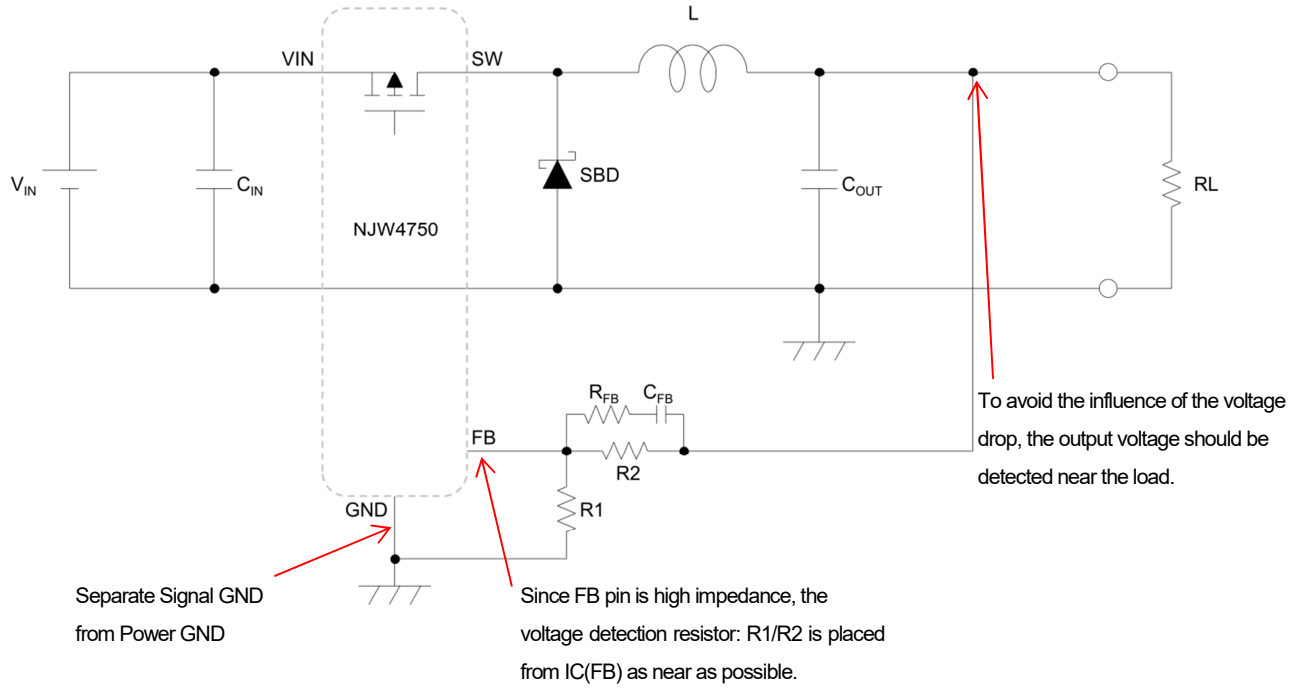


Fig.11 Board layout for buck Converter

■ APPLICATION INFORMATION(LDO)

• Setting of output voltage

The output voltage V_{OUT} is determined by the relative resistances of R1, R2.

$$V_{OUT}=\left(\frac{R2}{R1}+1\right)\times V_B[V]$$

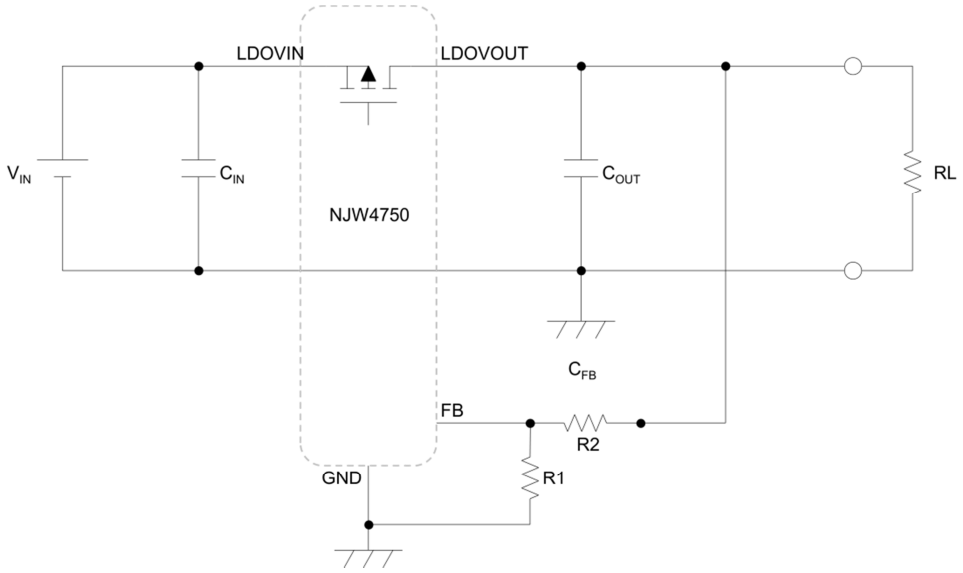


Fig.12 Output voltage setting

• Setting of phase compensation

The NJW 4750 has a built-in phase compensation circuit.

Table 5 shows the values of external parts based on output voltage.

Table 5 Value of phase compensation

V_{OUT}	C_{OUT}	R2
ALL	6.8μF to 22μF	47kΩ

■ CALCULATION OF PACKAGE POWER

The loss of NJW 4750 is the sum of the loss due to switching converter and the loss due to LDO.

• Switching convertor

Input Power : $P_{IN} = V_{IN} \times I_{IN}$ [W]
Output Power : $P_{OUT} = V_{OUT} \times I_{OUT}$ [W]
Diode Loss : $P_{DIODE} = V_F \times I_{L(avg)} \times$ OFF duty [W]
Power Consumption : $P_{LOSS} = P_{IN} - P_{OUT} - P_{DIODE}$ [W]

Where:

V_{IN}	: Input Voltage of Converter	I_{IN}	: Input Current of Converter
V_{OUT}	: Output Voltage of Converter	I_{OUT}	: Output Current of Converter
V_F	: Diode's Forward Saturation Voltage	$I_{L(avg)}$	: Inductor Average Current
OFF Duty	: Switch OFF Duty Cycle		

• LDO

Input Power : $P_{IN} = V_{IN} \times I_{IN}$ [W]
Output Power : $P_{OUT} = V_{OUT} \times I_{OUT}$ [W]
Power Consumption : $P_{LOSS} = P_{IN} - P_{OUT}$ [W]

Where:

V_{IN}	: Input Voltage of LDO	I_{IN}	: Input Current of LDO
V_{OUT}	: Output Voltage of LDO	I_{OUT}	: Output Current of LDO

Efficiency (η) is calculated as follows.

$\eta = (P_{OUT} \div P_{IN}) \times 100$ [%]

Please consider temperature derating to the calculated power consumption.
Please consider design power consumption in rated range referring to the power dissipation vs. ambient temperature characteristics.

■ APPLICATION DESIGN EXAMPLES

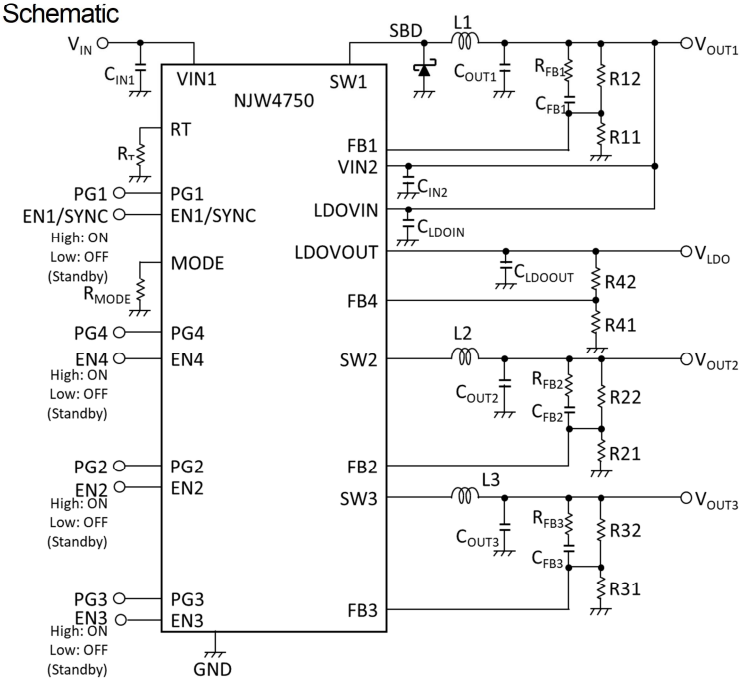
Spec

IC: NJW4750

Output: 3.3V (Ch.1)
1.8V (Ch.2)
1.2V (Ch.3)
2.8V (Ch.4)

Oscillating frequency: 2.0MHz

Schematic

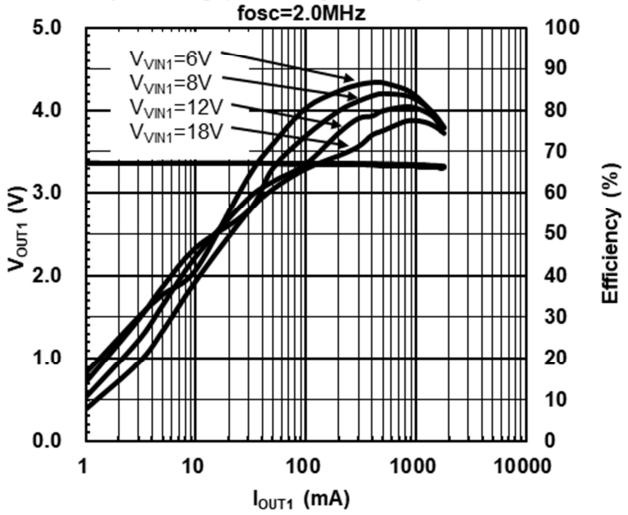


Parts list

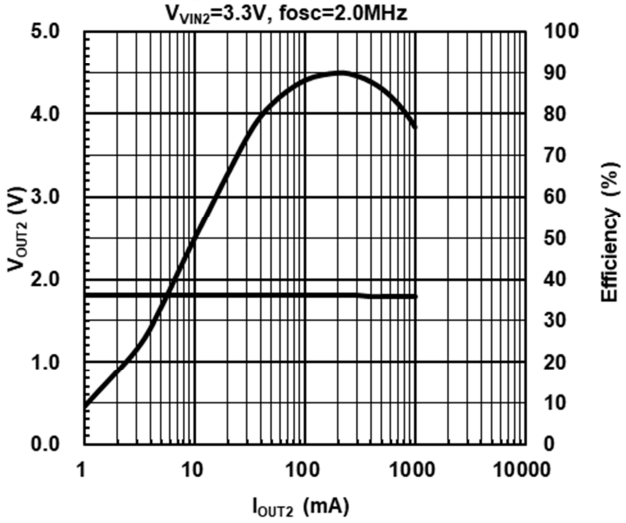
Ref.	Part number	Overview	Manufacture
IC	NJW4750MHH-T1	Quad Channel Combination Regulator	New Japan Radio
C_{IN1}	CGA4J3X5R1H475K125AB	Ceramic Capacitor 2125 4.7uF, 50V	TDK
C_{IN2}	GRT188C81C106ME13#	Ceramic Capacitor 1608 10uF, 16V	MURATA
C_{LDOIN}	GRT188C81C106ME13#	Ceramic Capacitor 1608 10uF, 16V	MURATA
R_T	3.0kΩ	Resistor 1608 3.0kΩ, ±1%, 0.1W	Std.
L1	VLS4012ET-1R5N	inductor 1.5uH, 2.1A	TDK
SBD	CMS14	Schottky Diode 60V, 2A	TOSHIBA
C_{OUT1}	GRT188C81C106ME13#	Ceramic Capacitor 1608 10uF, 16V	MURATA
C_{FB1}	22 p F	Ceramic Capacitor 22pF, 50V	Std.
R_{FB1}	1kΩ	Resistor 1kΩ, ±1%, 0.1W	Std.
R11	24.3kΩ	Resistor 24.3kΩ, ±1%, 0.1W	Std.
R12	76.8kΩ	Resistor 76.8kΩ, ±1%, 0.1W	Std.
L2	VLS3015ET-2R2M	inductor 2.2uH, 1.5A	TDK
C_{OUT2}	GRM21BB30J226ME38L	Ceramic Capacitor 2125 22uF, 6.3V	MURATA
C_{FB2}	22 p F	Ceramic Capacitor 22pF, 50V	Std.
R_{FB2}	1kΩ	Resistor 1kΩ, ±1%, 0.1W	Std.
R21	24kΩ	Resistor 24kΩ, ±1%, 0.1W	Std.
R22	30kΩ	Resistor 30kΩ, ±1%, 0.1W	Std.
L3	VLS3015ET-2R2M	inductor 2.2uH, 1.5A	TDK
C_{OUT3}	JMK212BBJ476MG-T	Ceramic Capacitor 2125 47uF, 6.3V	TAIYO YUDEN
C_{FB3}	22pF	Ceramic Capacitor 22pF, 50V	Std.
R_{FB3}	1kΩ	Resistor 1kΩ, ±1%, 0.1W	Std.
R31	75kΩ	Resistor 75kΩ, ±1%, 0.1W	Std.
R32	37.4kΩ	Resistor 37.4kΩ, ±1%, 0.1W	Std.
C_{LDOOUT}	GRT188C81C106ME13#	Ceramic Capacitor 1608 10uF, 16V	MURATA
R41	18.7kΩ	Resistor 18.7kΩ, ±1%, 0.1W	Std.
R42	47.5kΩ	Resistor 47.5kΩ, ±1%, 0.1W	Std.
R_{MODE}	30kΩ	Resistor 30kΩ, ±1%, 0.1W/SW Hiccup MODE	Std.

■ APPLICATION CHARACTERISTICS

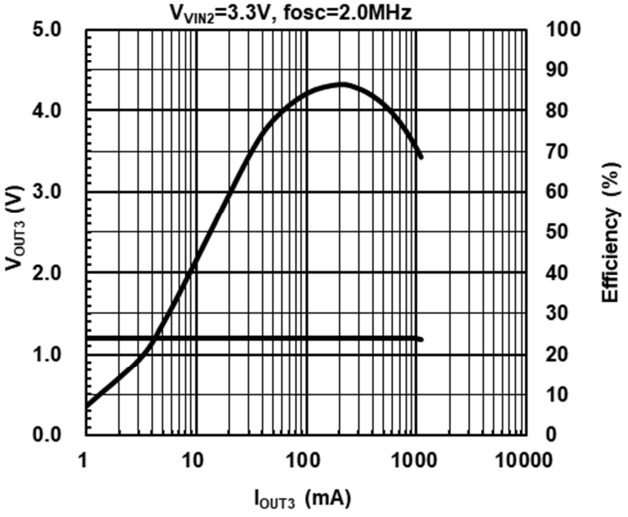
NJW4750 Ch.1
Output Voltage, efficiency vs. Output current
fosc=2.0MHz



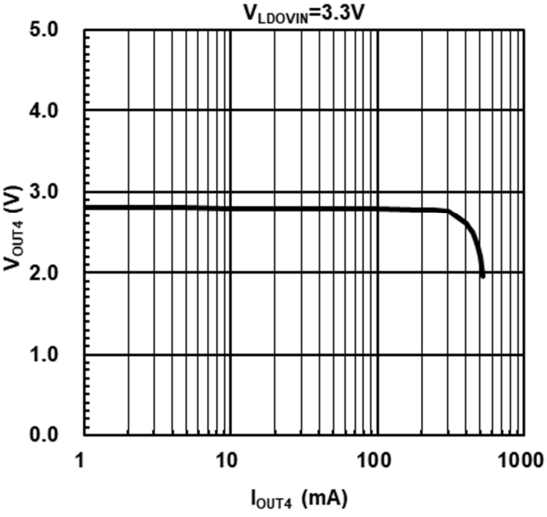
NJW4750 Ch.2
Output Voltage, efficiency vs.Output current
V_{VIN2}=3.3V, fosc=2.0MHz



NJW4750 Ch.3
Output Voltage, efficiency vs. Output current
V_{VIN2}=3.3V, fosc=2.0MHz



NJW4750 Ch.4
Output Voltage, efficiency vs. Output current
V_{LDOVIN}=3.3V

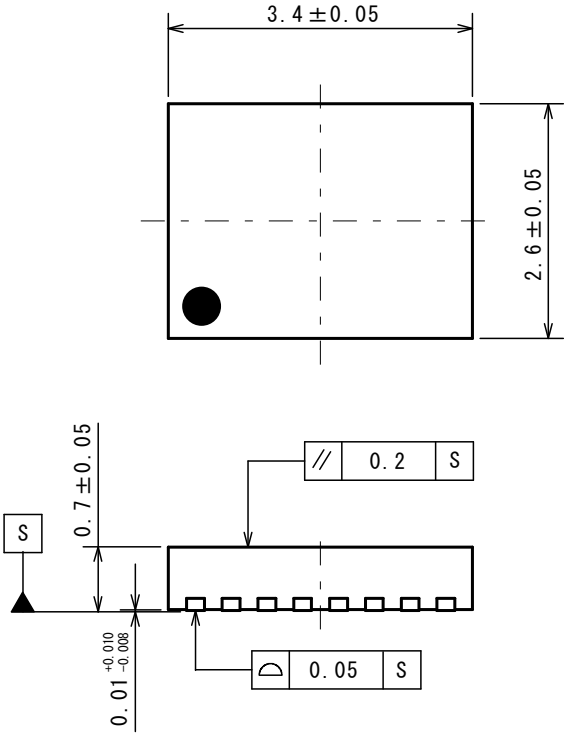


■ PACKAGE/ FOOTPATTERN

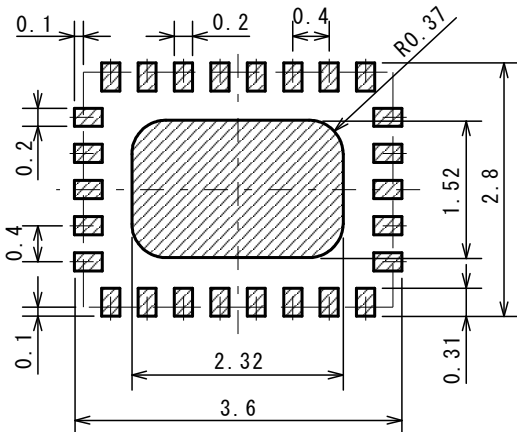
EQFN26-HH

Unit: mm

PACKAGE DIMENSIONS



EXAMPLE OF SOLDER PADS DIMENSIONS

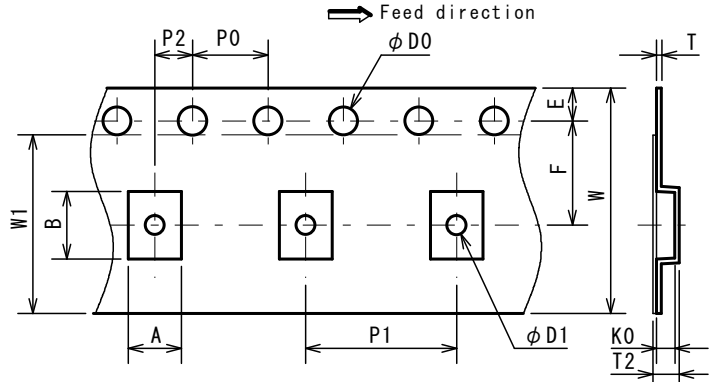


EQFN26-HH

■ PACKAGING INFORMATION

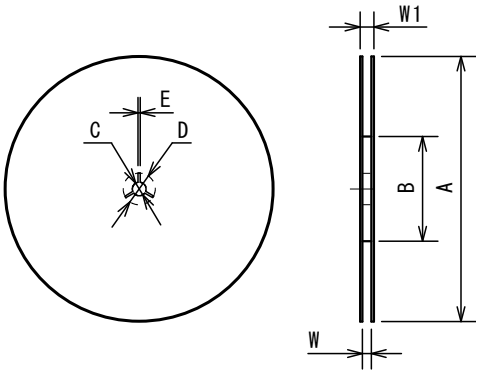
Unit: mm

TAPING DIMENSIONS



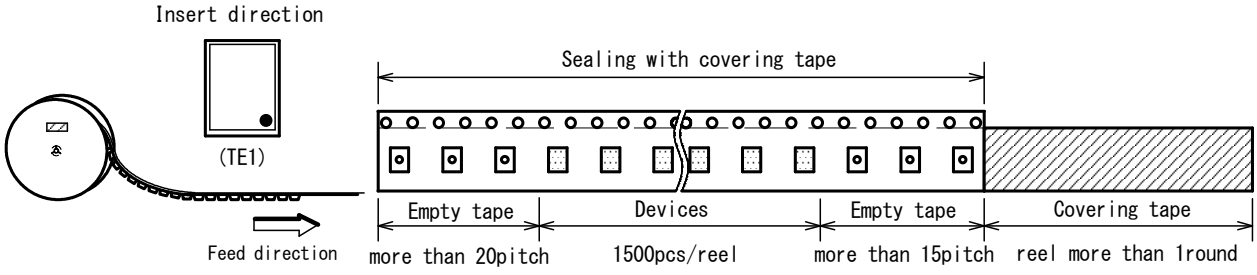
SYMBOL	DIMENSION	REMARKS
A	2.8±0.05	BOTTOM DIMENSION
B	3.6±0.05	BOTTOM DIMENSION
D0	$1.5^{+0.1}_{0}$	
D1	$1.0^{+0.1}_{0}$	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.25±0.05	
T2	1.2	
K0	0.85±0.05	
W	$12.0^{+0.3}_{-0.1}$	
W1	9.5	THICKNESS 0.1max

REEL DIMENSIONS

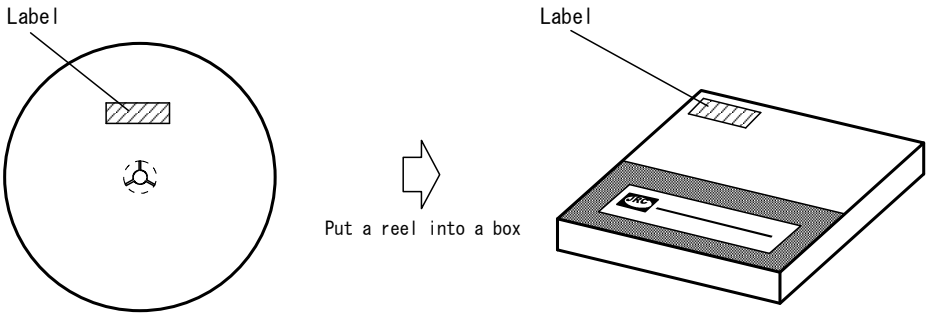


SYMBOL	DIMENSION
A	$\phi 180^{0}_{-3}$
B	$\phi 60^{+1}_{0}$
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	$13^{+1.0}_{0}$
W1	15.4±1.0

TAPING STATE



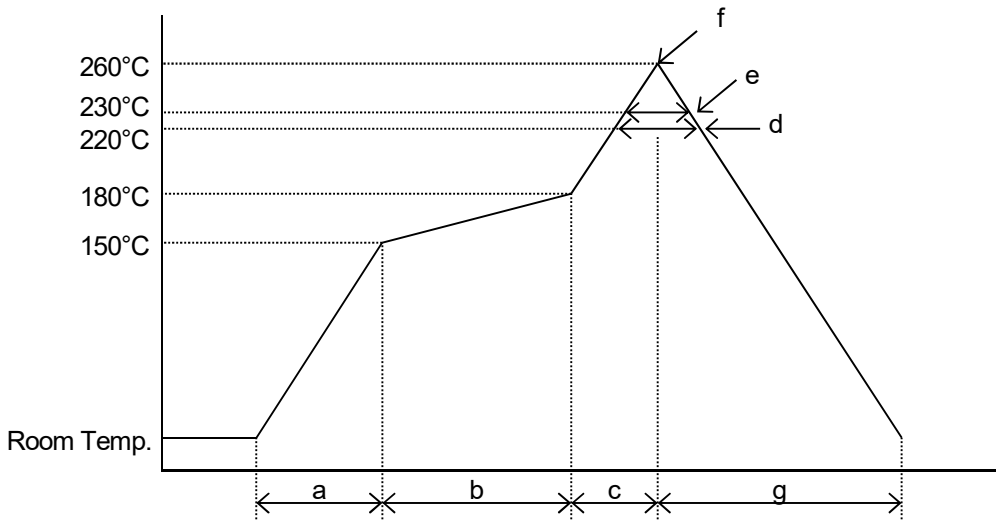
PACKING STATE



■ RECOMMENDED MOUNTING METHOD

INFRARED REFLOW SOLDERING METHOD

Recommended reflow soldering procedure



a : Temperature ramping rate	: 1 to 4°C /s
b : Pre-heating temperature	: 150 to 180°C
time	: 60 to 120s
c : Temperature ramp rate	: 1 to 4°C /s
d : 220°C or higher time	: Shorter than 60s
e : 230°C or higher time	: Shorter than 40s
f : Peak temperature	: Lower than 260°C
g : Temperature ramping rate	: 1 to 6°C /s

The temperature indicates at the surface of mold package.

■ **REVISION HISTORY**

DATE	REVISION	CHANGES
15.Jun.2018	Ver.1.0	New release

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