

MOSFET – Power, Dual N-Channel

60 V, 11.9 mΩ, 40 A



ON Semiconductor®

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NVMFD5C672NL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFD5C672NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

| $V_{(BR)DSS}$ | $R_{DS(ON)}$ MAX | I_D MAX |
|---------------|------------------|-----------|
| 60 V | 11.9 mΩ @ 10 V | 40 A |
| | 16.8 mΩ @ 4.5 V | |

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

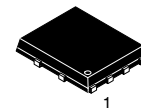
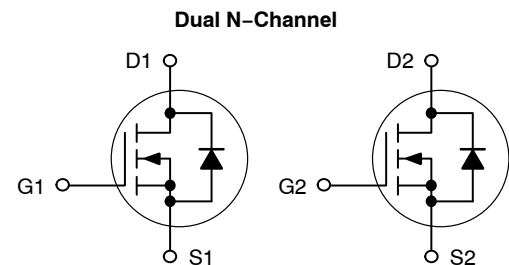
| Parameter | Symbol | Value | Unit | |
|---|--|---------------------------|------------------|---|
| Drain-to-Source Voltage | V_{DSS} | 60 | V | |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V | |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1, 2, 3) | Steady State | $T_C = 25^\circ\text{C}$ | I_D 40 | A |
| | | $T_C = 100^\circ\text{C}$ | 31 | |
| Power Dissipation $R_{\theta JC}$ (Notes 1, 2) | Steady State | $T_C = 25^\circ\text{C}$ | P_D 42 | W |
| | | $T_C = 100^\circ\text{C}$ | 21 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3) | Steady State | $T_A = 25^\circ\text{C}$ | I_D 11 | A |
| | | $T_A = 100^\circ\text{C}$ | 8.0 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1, 2) | Steady State | $T_A = 25^\circ\text{C}$ | P_D 3.1 | W |
| | | $T_A = 100^\circ\text{C}$ | 1.5 | |
| Pulsed Drain Current | $T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$ | I_{DM} 161 | A | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +175 | $^\circ\text{C}$ | |
| Source Current (Body Diode) | I_S | 35.2 | A | |
| Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, I_{L(pk)} = 2 \text{ A}$) | E_{AS} | 66 | mJ | |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

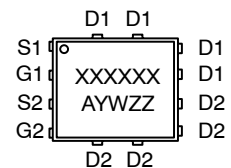
| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|---------------------------|
| Junction-to-Case – Steady State | $R_{\theta JC}$ | 3.55 | $^\circ\text{C}/\text{W}$ |
| Junction-to-Ambient – Steady State (Note 2) | $R_{\theta JA}$ | 47.51 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



DFN8 5x6 (SO8FL) CASE 506BT

MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------------------------------|--|------------------------|-----|-----|-------|
| OFF CHARACTERISTICS | | | | | | |
| Drain-to-Source Breakdown Voltage | V _{(BR)DSS} | V _{GS} = 0 V, I _D = 250 μA | 60 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | V _{(BR)DSS} /T _J | | | 27 | | mV/°C |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{GS} = 0 V, V _{DS} = 60 V | T _J = 25 °C | | 10 | μA |
| | | | T _J = 125°C | | 100 | |
| Gate-to-Source Leakage Current | I _{GSS} | V _{DS} = 0 V, V _{GS} = 20 V | | | 100 | nA |

ON CHARACTERISTICS (Note 4)

| | | | | | | |
|--|-------------------------------------|--|-----------------------|------|------|-------|
| Gate Threshold Voltage | V _{GS(TH)} | V _{GS} = V _{DS} , I _D = 30 μA | 1.2 | | 2.2 | V |
| Negative Threshold Temperature Coefficient | V _{GS(TH)} /T _J | | | -5.7 | | mV/°C |
| Drain-to-Source On Resistance | R _{DS(on)} | V _{GS} = 10 V | I _D = 10 A | 9.8 | 11.9 | mΩ |
| | | V _{GS} = 4.5 V | I _D = 10 A | 13.4 | 16.8 | |
| Forward Transconductance | g _{FS} | V _{DS} = 15 V, I _D = 10 A | | 27.5 | | S |

CHARGES, CAPACITANCES & GATE RESISTANCE

| | | | | | | |
|------------------------------|---------------------|--|--|------|--|----|
| Input Capacitance | C _{ISS} | V _{GS} = 0 V, f = 1 MHz, V _{DS} = 25 V | | 793 | | pF |
| Output Capacitance | C _{OSS} | | | 383 | | |
| Reverse Transfer Capacitance | C _{RSS} | | | 9.0 | | |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 4.5 V, V _{DS} = 48 V; I _D = 10 A | | 5.7 | | nC |
| Total Gate Charge | Q _{G(TOT)} | V _{GS} = 10 V, V _{DS} = 48 V; I _D = 10 A | | 12.3 | | |
| Threshold Gate Charge | Q _{G(TH)} | V _{DS} = 48 V; I _D = 10 A | | 1.5 | | |
| Gate-to-Source Charge | Q _{GS} | | | 2.7 | | |
| Gate-to-Drain Charge | Q _{GD} | | | 1.2 | | |
| Plateau Voltage | V _{GP} | | | 2.8 | | V |

SWITCHING CHARACTERISTICS (Note 5)

| | | | | | | |
|---------------------|---------------------|---|--|----|--|----|
| Turn-On Delay Time | t _{d(ON)} | V _{GS} = 4.5 V, V _{DS} = 48 V, I _D = 10 A, R _G = 1.0 Ω | | 11 | | ns |
| Rise Time | t _r | | | 30 | | |
| Turn-Off Delay Time | t _{d(OFF)} | | | 22 | | |
| Fall Time | t _f | | | 28 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|-----------------|--|------------------------|------|-----|-----|----|
| Forward Diode Voltage | V _{SD} | V _{GS} = 0 V, I _S = 10 A | T _J = 25°C | | 0.9 | 1.2 | V |
| | | | T _J = 125°C | | 0.8 | | |
| Reverse Recovery Time | t _{RR} | V _{GS} = 0 V, dI _S /dt = 20 A/μs, I _S = 10 A | | 26 | | ns | |
| Charge Time | t _a | | | 12.3 | | | |
| Discharge Time | t _b | | | 13.5 | | | |
| Reverse Recovery Charge | Q _{RR} | | | 13 | | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

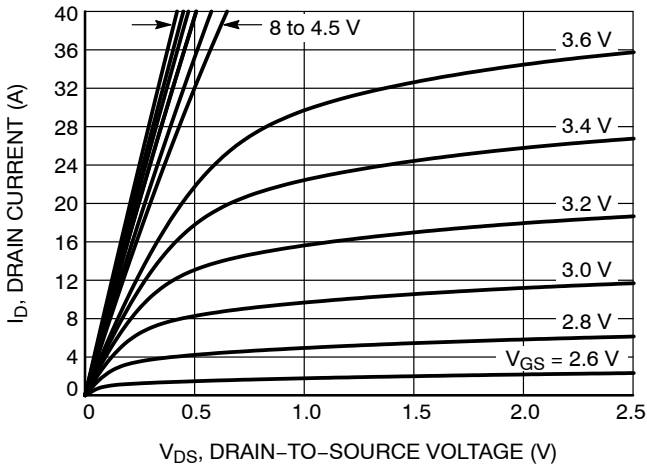


Figure 1. On-Region Characteristics

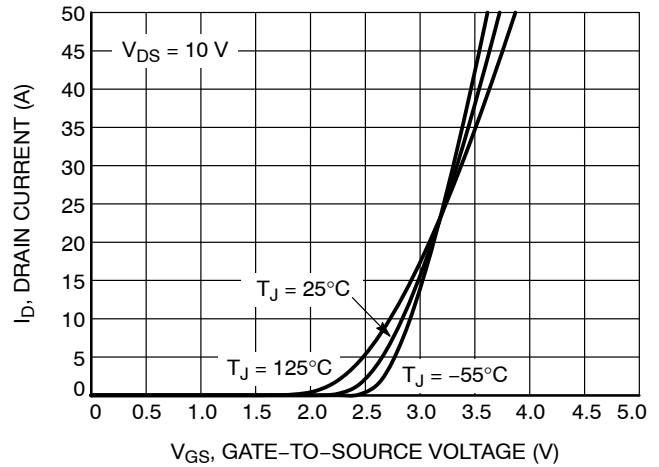


Figure 2. Transfer Characteristics

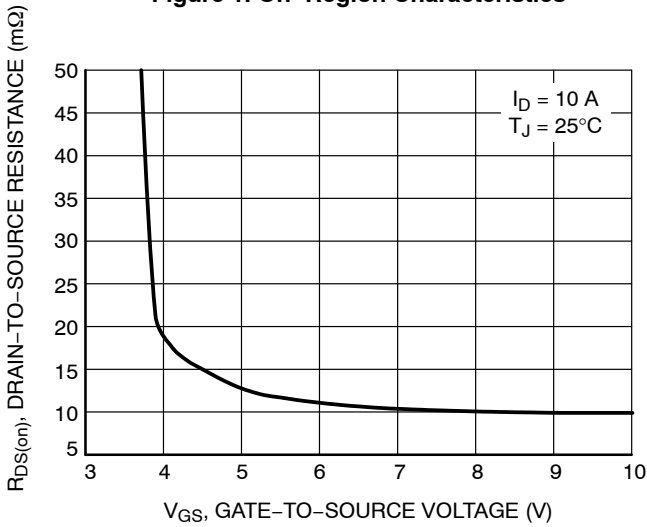


Figure 3. On-Resistance vs. Gate-to-Source Voltage

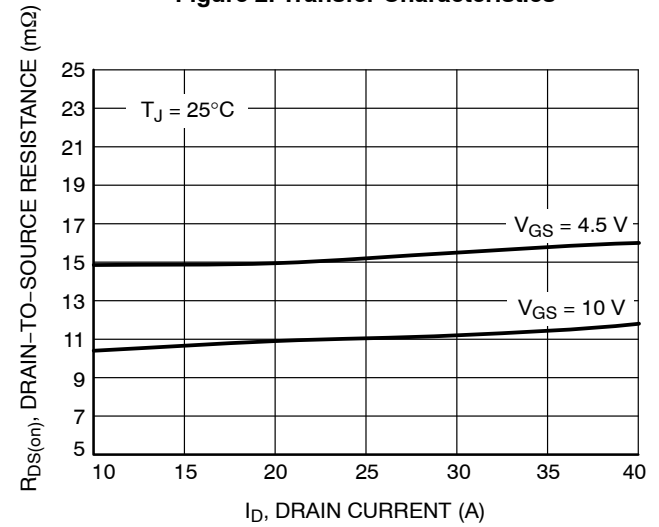


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

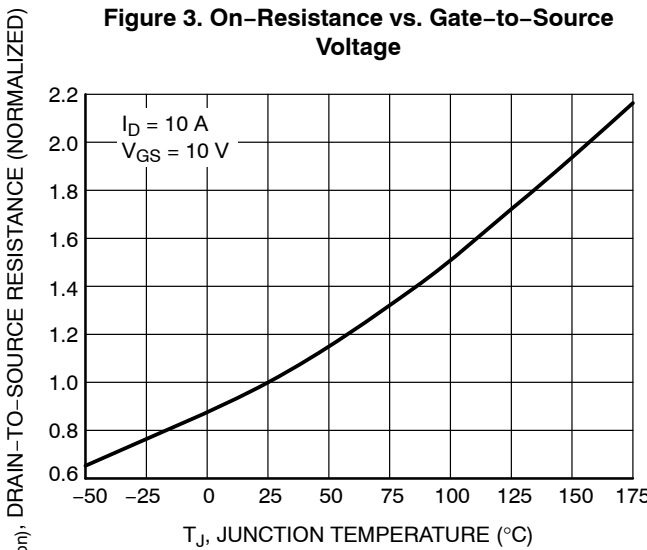


Figure 5. On-Resistance Variation with Temperature

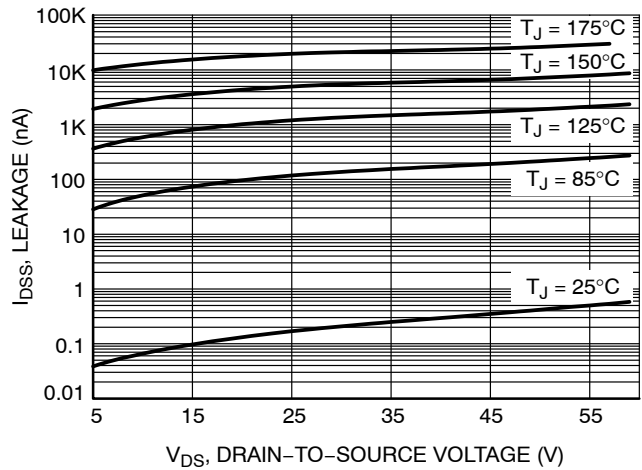


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

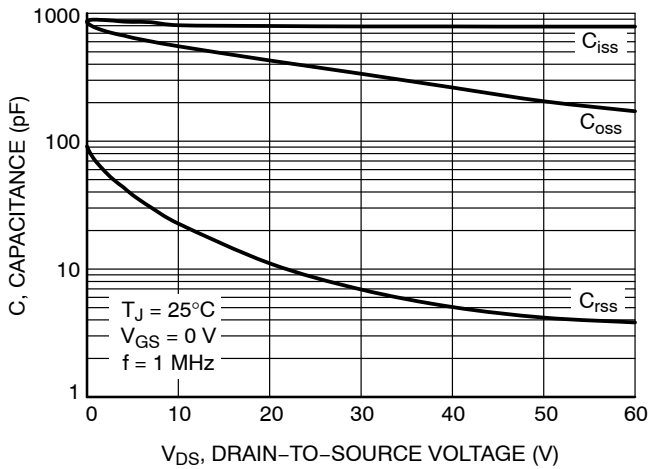


Figure 7. Capacitance Variation

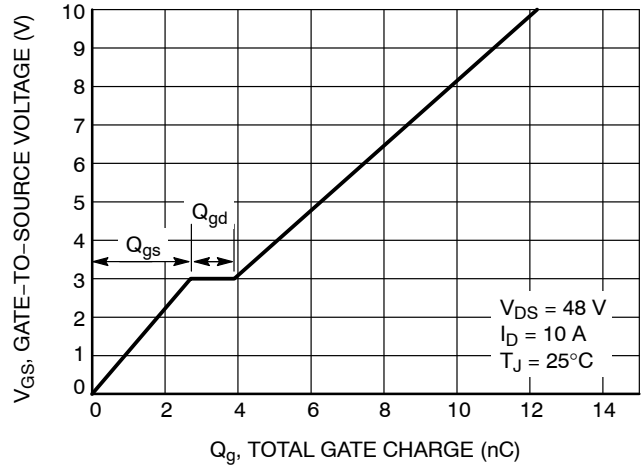


Figure 8. Gate-to-Source vs. Total Charge

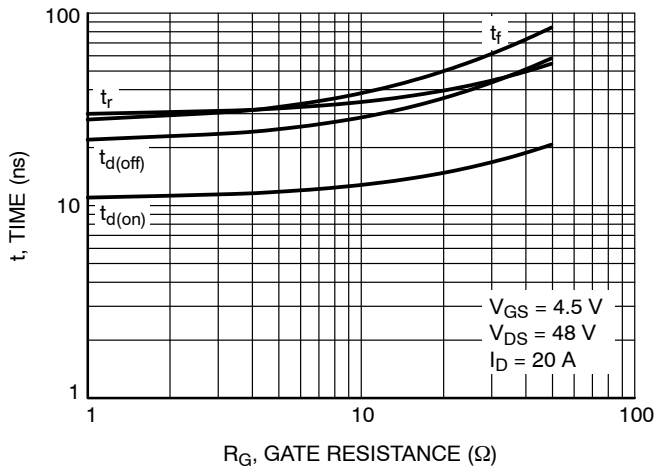


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

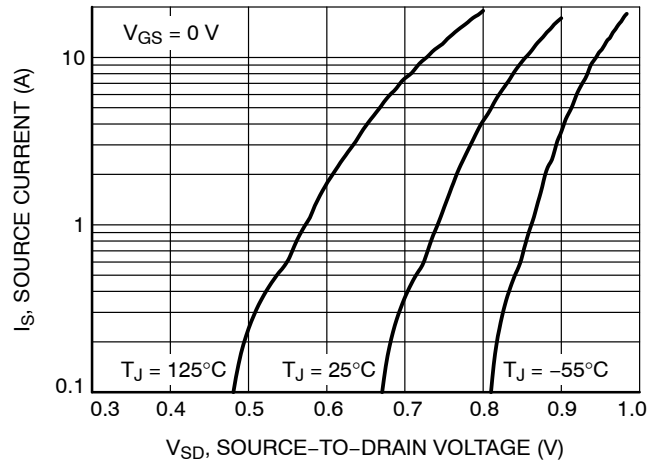


Figure 10. Diode Forward Voltage vs. Current

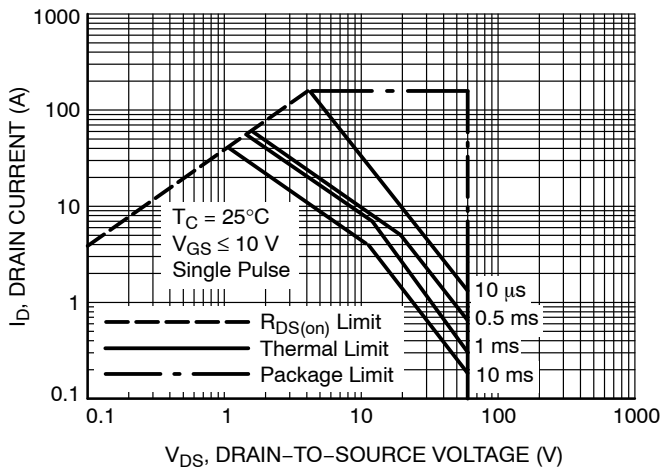


Figure 11. Maximum Rated Forward Biased Safe Operating Area

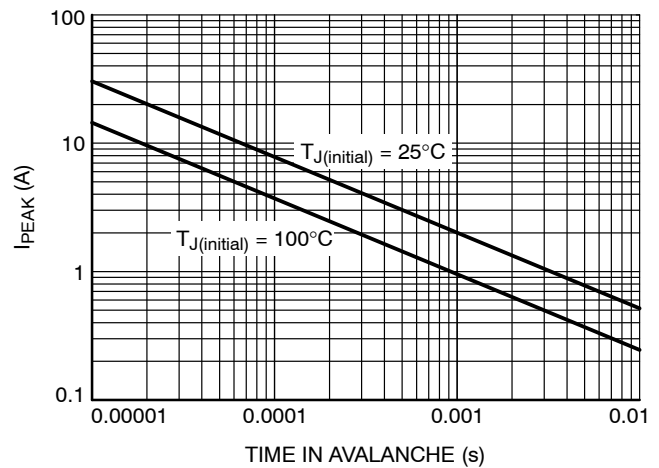


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

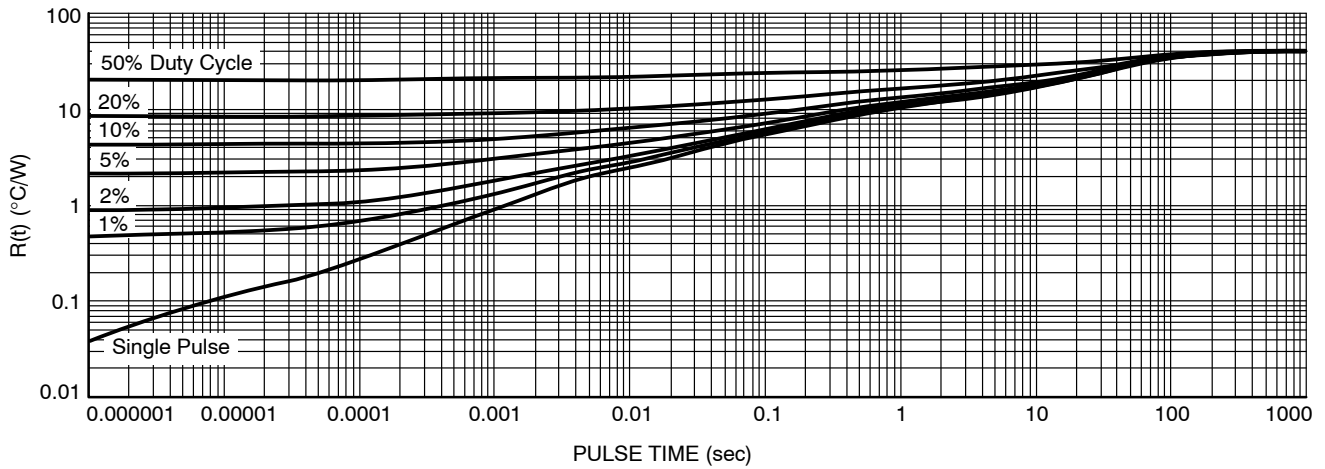


Figure 13. Thermal Response

DEVICE ORDERING INFORMATION

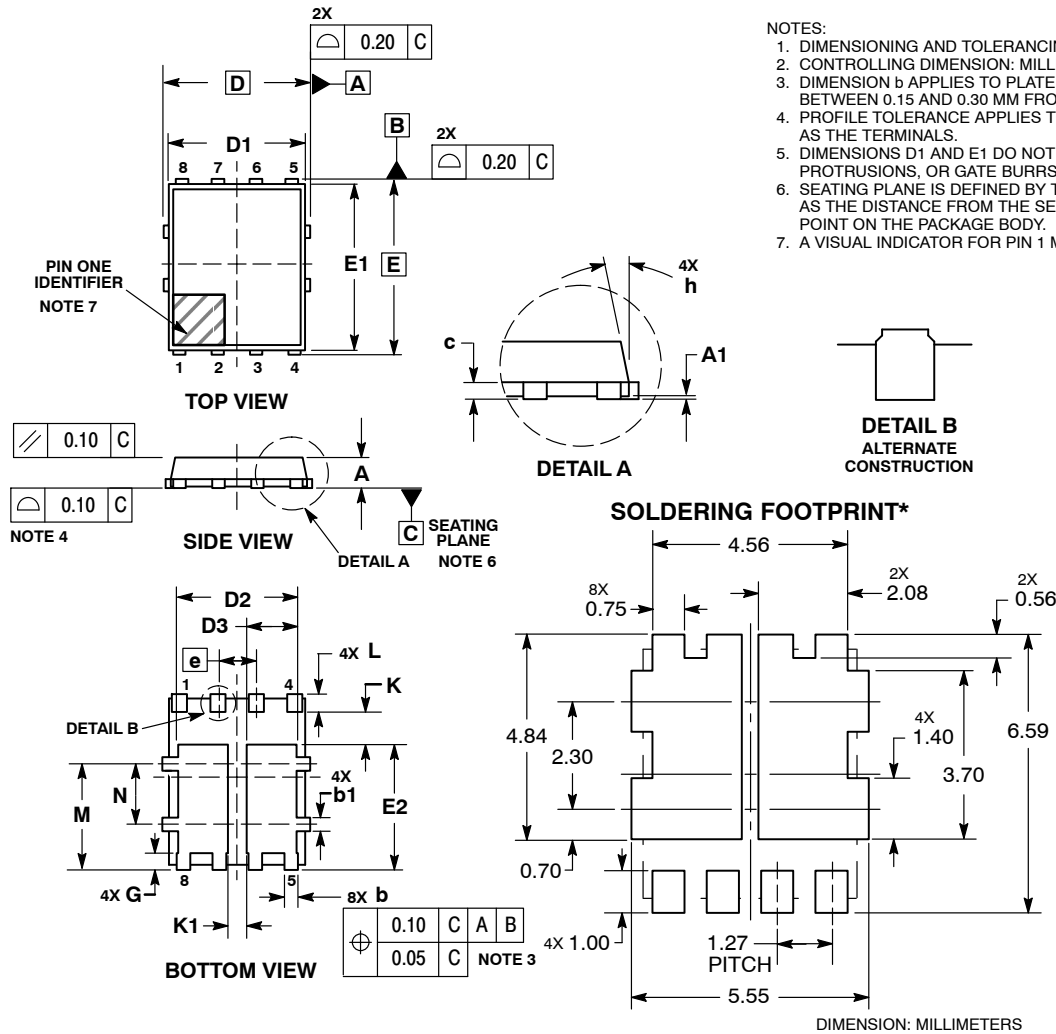
| Device | Marking | Package | Shipping† |
|-------------------|---------|------------------------------------|--------------------|
| NVMFD5C672NLT1G | 5C672L | DFN8 (Pb-Free) | 1500 / Tape & Reel |
| NVMFD5C672NLWFT1G | 672LWF | DFN8 (Pb-Free, Wettable Flanks) | 1500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVMFD5C672NL

PACKAGE DIMENSIONS

DFN8 5x6, 1.27P Dual Flag (SO8FL-Dual) CASE 506BT ISSUE E



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. PROFILE TOLERANCE APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
6. SEATING PLANE IS DEFINED BY THE TERMINALS. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. A VISUAL INDICATOR FOR PIN 1 MUST BE LOCATED IN THIS AREA.

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN | MAX | MAX |
| A | 0.90 | ---- | 1.10 |
| A1 | ---- | ---- | 0.05 |
| b | 0.33 | 0.42 | 0.51 |
| b1 | 0.33 | 0.42 | 0.51 |
| c | 0.20 | ---- | 0.33 |
| D | 5.15 BSC | | |
| D1 | 4.70 | 4.90 | 5.10 |
| D2 | 3.90 | 4.10 | 4.30 |
| D3 | 1.50 | 1.70 | 1.90 |
| E | 6.15 BSC | | |
| E1 | 5.70 | 5.90 | 6.10 |
| E2 | 3.90 | 4.15 | 4.40 |
| e | 1.27 BSC | | |
| G | 0.45 | 0.55 | 0.65 |
| h | ---- | ---- | 12 ° |
| K | 0.51 | ---- | ---- |
| K1 | 0.56 | ---- | ---- |
| L | 0.48 | 0.61 | 0.71 |
| M | 3.25 | 3.50 | 3.75 |
| N | 1.80 | 2.00 | 2.20 |

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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