

REALTEK

RTL8821CU-CG

**Single-Chip IEEE 802.11a/b/g/n/ac 1T1R
WLAN with Integrated Bluetooth Smart
Ready with USB 2.0 Interface**

DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 0.2r16, May., 2019
Track ID:



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USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2016/02/02	Preliminary release.
0.2r05	2016/6/20	Modify general description and features
0.2r07	2016/8/16	Modify general description and features
0.2r08	2016/9/06	Modify general description and features
0.2r09	2016/12/29	Modify RFIO description
0.2r10	2017/04/10	Update power on timing diagram
0.2r15	2018/12/06	Modify Bluetooth description
0.2r16	2019/05/24	Update Mark Information

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1. General Description

The Realtek RTL8821CU-CG is a highly-integrated IEEE 802.11 a/b/g/n/ac MAC/Baseband/RF WLAN and Bluetooth Baseband/RF single chip. For Wireless LAN (WLAN) operation, it supports 1-stream 802.11ac solution with Multi-user MIMO (Multiple-Input, Multiple-Output) STA mode with USB2.0 network interface controller. For Bluetooth operation, it supports Bluetooth Smart Ready with USB interface controller.

The RTL8821CU-CG baseband implements multiuser Multiple-Input Multiple-Output (MIMO) Orthogonal Frequency Division Multiplexing (OFDM) STA mode with one transmit and one receive path (1T1R). Features include one spatial stream transmission, short Guard Interval (GI) of 400ns, spatial spreading, and support for variant channel bandwidths. Moreover, RTL8821CU-CG provides one spatial stream Space-Time Block Code (STBC) and Low Density Parity Check (LDPC) to extend the range of transmission. As the recipient, the RTL8821CU-CG also supports explicit sounding packet feedback that helps senders with beamforming capability.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11 a, 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and QPSK with data scrambling capability, are available. CCK provides support for legacy data rates, with long or short preamble. The high speed FFT/IFFT paths are combined with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation of the individual subcarriers. The compatible coding rate of 1/2, 2/3, 3/4, and 5/6 provides up to 433.3Mbps for IEEE 802.11ac with MIMO-OFDM.

The RTL8821CU-CG builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams. Robust interference detection and suppression are provided to protect against Bluetooth, cordless phone, and microwave oven interference.

Receive vector diversity for multi-stream application is implemented for efficient utilization of the MIMO channel. Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end.

The RTL8821CU-CG supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control functions to obtain better performance in the analog portions of the transceiver.

The RTL8821CU-CG MAC supports 802.11e for multimedia applications, 802.11i and WAPI (Wireless Authentication Privacy Infrastructure) for security, and 802.11n/ac for enhanced MAC protocol efficiency. Protocol efficiency is significantly improved by using packet aggregation techniques, such as A-MPDU

with BA and A-MSDU. Power saving mechanisms, such as Legacy Power Save, U-APSD, and MIMO, can reduce the power wasted during idle time. They can also compensate for the extra power required to transmit MIMO-OFDM. The RTL8821CU-CG provides simple legacy and 20MHz/40MHz/80MHz co-existence mechanism to ensure backward and network compatibility.

The RTL8821CU-CG Bluetooth controller complies with Bluetooth core specification v4.2, and supports dual mode (BR/EDR + AMP + Low Energy Controllers). It is backward compatible with previous versions including v2.1 + EDR. For BR/EDR, it can support scatternet topology up to four active links in slave mode, and seven active links in master mode. For Low Energy, it supports multiple states and allows eight active links in master mode. Both BR/EDR and LE can operate simultaneously.

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2. Features

General Information

- 56pins QFN
- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11a/b/g/n/ac compatible WLAN
- Support 802.11ac 1x1, Wave-2 compliant with MU-MIMO STA mode
- Complete 802.11n MIMO solution for 2.4GHz and 5GHz band
- Maximum PHY data rate up to 86.7Mbps using 20MHz bandwidth, 200Mbps using 40MHz bandwidth, and 433.3Mbps using 80MHz bandwidth.
- Backward compatible with 802.11a/b/g devices while operating at 802.11n data rates
- Backward compatible with 802.11a/n devices while operating at 802.11ac data rates.

Host Interface

- Complies with USB 2.0 for WLAN and BT controller
- USB Multi-Function for both BT (USB function 0) and WLAN (USB function 1)
- USB LPM/ Selective Suspend supported

Standards Supported

- IEEE 802.11a/b/g/n/ac compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- IEEE 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services
- IEEE 802.11h DFS, TPC, Spectrum Measurement
- IEEE 802.11k Radio Resource Measurement
- WAPI (Wireless Authentication Privacy Infrastructure) certified.
- Cisco Compatible Extensions (CCX) for WLAN devices

MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate Block Acknowledgement (BA)
- Long NAV for media reservation with CF-End for NAV release
- PHY-level spoofing to enhance legacy compatibility
- Channel management and co-existence
- Multiple BSSID feature allows the RTL8821CU-CG to assume multiple MAC identities when used as a wireless bridge

- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- WiFi Direct supports wireless peer to peer applications.
- WiFi NAN (Neighborhood Area Network) support

Other Features

- Supports Wake-On-WLAN via Magic Packet and Wake-up frame
- Transmit Beamforming
- Support S3/S4 AES/TKIP group key update

Peripheral Interfaces

- Up to 15 General Purpose Input/Output pins
- Three configurable LED pins (mux with GPIO pins)

PHY Features

- IEEE 802.11ac OFDM
- IEEE 802.11n OFDM
- One Transmit and One Receive path
- 5MHz / 10MHz / 20MHz / 40MHz / 80MHz bandwidth transmission
- Support 2.4GHz and 5GHz band channels
- Short Guard Interval (400ns)
- Sounding packet.
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, 64QAM and 256QAM modulation.

- WiFi FTM (Fine Time Measurement) supported
- WiFi TDLS (Tunneled Direct Link Setup) Supported

- Support Network List Offload
- CCA on secondary through RTS/CTS handshake.
- Support TCP/UDP/IP checksum offload
- Generates 40MHz clock for peripheral chip.
- Single external power source 3.3V only

Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6

- Maximum data rate 54Mbps in 802.11g, 150Mbps in 802.11n and 433.3bps in 802.11ac.
- Switch diversity used for DSSS/CCK
- Support STBC Receiving
- Support LDPC Transmitting
- Hardware antenna diversity
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC
- Build-in both 2.4GHz and 5GHz PA
- Build-in both 2.4GHz and 5GHz LNA

Bluetooth Controller

- Compatible with Bluetooth 2.1+EDR
- Support Bluetooth 4.2 system
- Integrated MCU to execute Bluetooth protocol stack
- Supports all packet types in basic rate and enhanced data rate
- Support Bluetooth 5.0 High Duty Cycle Non-Connectable Advertising
- Supports Secure Simple Pairing
- Enhanced BT/WIFI Coexistence Control to improve transmission quality in different profiles
- Bluetooth 4.0 Dual Mode support: Simultaneous LE and BR/EDR
- Supports multiple Low Energy states

Bluetooth Transceiver

- Fast AGC control to improve receiving dynamic range
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy
- Integrated 32K oscillator for power management

3. Application Diagrams

3.1. 11ac Dual-Band 1x1 RF Application

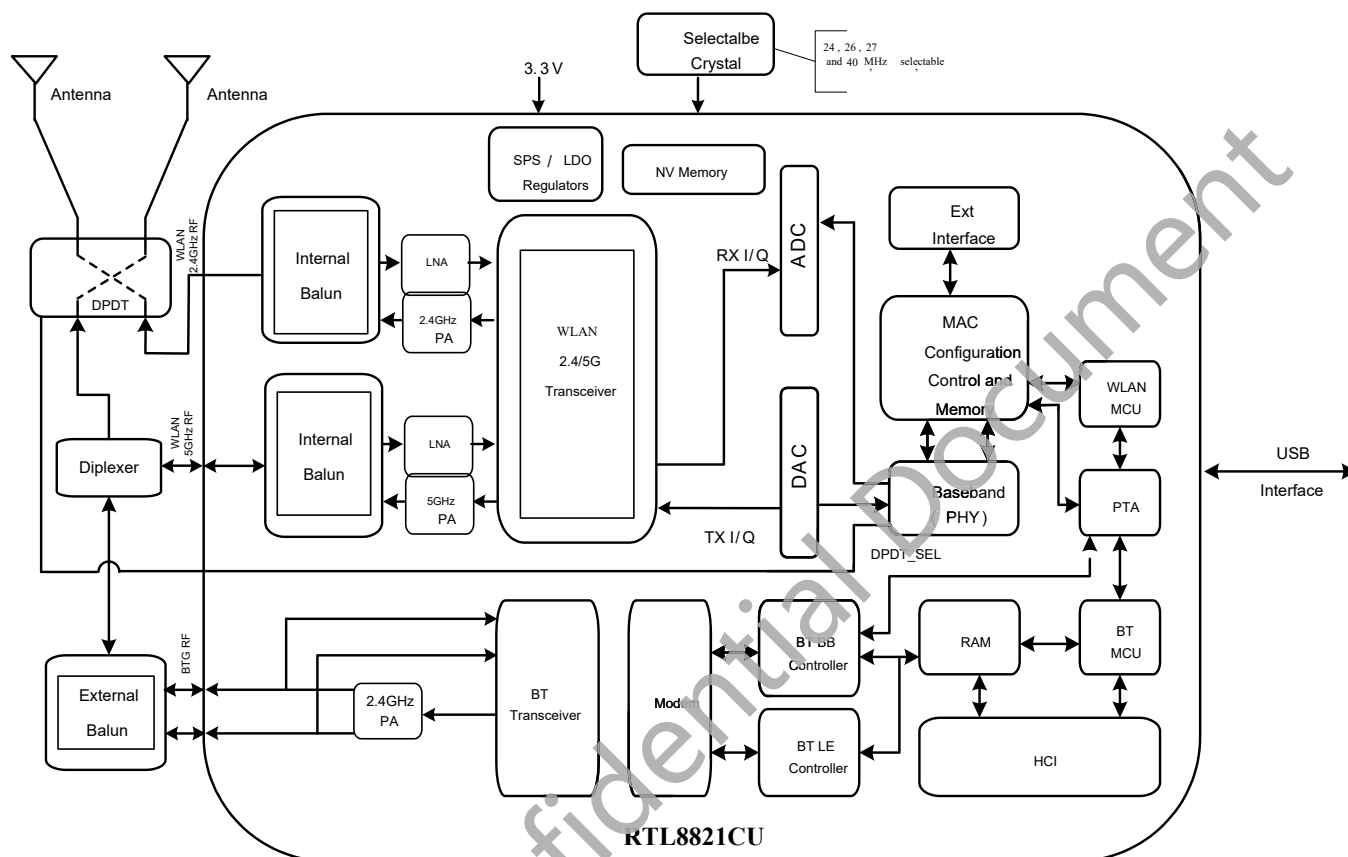


Figure 1. Dual-Band MIMO 1x1 Solution (11ac 1x1 MAC/BB/RF + PA) and Integrated Bluetooth Controller Solution --- RTL8821CU-CG

4. Pin Assignments

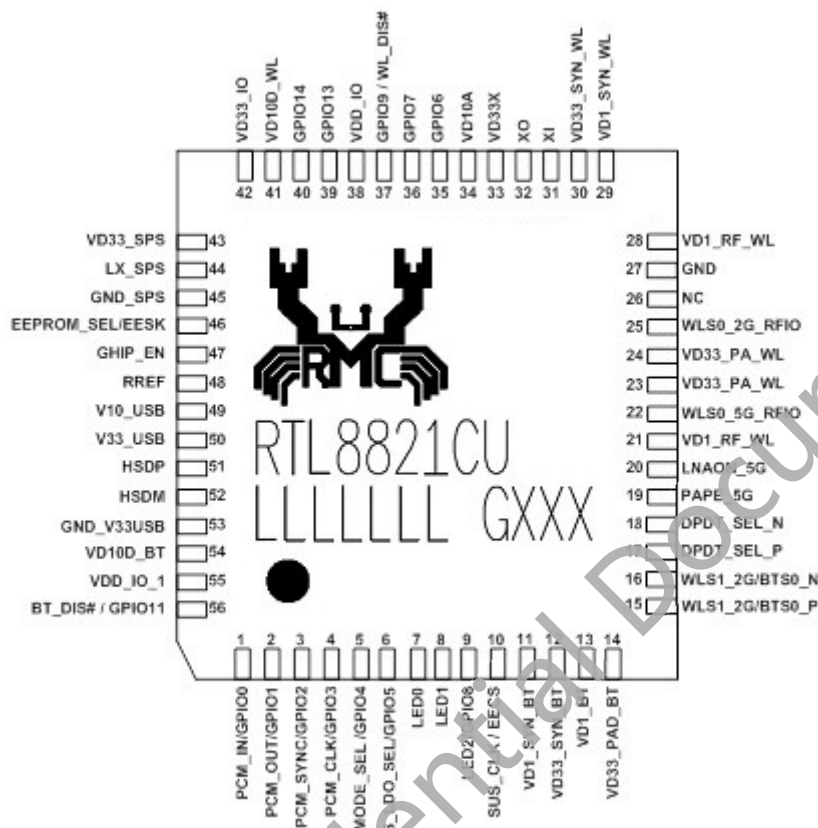


Figure 2. Pin Assignments

4.1. Package Identification & Mark Information

Body (mm ²)	LOGO FONT		Mark Example					備註 Remark
	LOGO SIZE	2.7 x 2.2 mm ²						
7x7								1. LOGO 靠左對齊 LOGO aligns to left 2. Pin1 位置在正印的左下 Pin1 mark orientation : bottom left
Line	Item	FONT	a (mm)	b (mm)	c (mm)	d (mm)	e (mm)	對齊 Alignment
1	Part no.	Realtek standard	0.75	0.30	0.10	0.20	-	Left
	Lot no.	Realtek standard	0.75	0.30	0.10	0.20	-	Left
2	Date Code (BDC/ADC)	Realtek standard	0.75	0.30	0.10	0.20	-	Left 並與 Lot no.間距 1 個字元 Left and space 1 character width with Lot no.

Figure 2, 'Green' package is indicated by a 'G'. The location marked is indicated by 'T'. The version is shown in the location marked 'V'.

5. Pin Descriptions

The following signal type codes are used in the table 1 to 9,

I: Input

P: Power pin

O: Output

N/A: No Bonding pin

I/O: Input/Output pin

5.1. Power on Trap Pin

Symbol	Type	Pin No.	Description
TEST_MODE_SEL	I	5	This pin is also shared with GPIO4 0: Normal operation mode 1: Test/debug mode
SPS_LDO_SEL	I	6	This pin is also shared with GPIO5 0: Internal switching regulator select 1: Internal LDO select
EEPROM_SEL	I	46	This pin is also shared with EESK pin 0: Internal NW memory select 1: External EEPROM select

Table 1. Power-On Trap Pins

5.2. USB Transceiver Interface

Symbol	Type	Pin No.	Description
HSDP	I/O	51	High-Speed USB D+ Signal
HSDM	I/O	52	High-Speed USB D- Signal

Table 2. USB Transceiver Interface

5.3. EEPROM Interface

Symbol	Type	Pin No.	Description
EECS	O	10	External EEPROM Chip Select
EESK	O	46	External EEPROM Clock

Table 3. EEPROM Interface

5.4. RF Interface

Symbol	Type	Pin No	Description
WLS1_2G/BTS0_P	I/O	15	BT/WLAN 2G RF Differential I/O P
WLS1_2G/BTS0_N	I/O	16	BT/WLAN 2G RF Differential I/O N
DPDT_SEL_P	O	17	External DPDT CONTROL
DPDT_SEL_N	O	18	External DPDT CONTROL
PAPE_5G	O	19	External 5G PAPE CONTROL
LNAON_5G	O	20	External 5G LNA CONTROL
WLS0_5G_RFIO	O	22	WLAN 5G RF I/O
WLS0_2G_RFIO	O	25	WLAN 2G RF I/O

Table 4. RF Interface

5.5. LED Interface

Symbol	Type	Pin No	Description
LED0	O	7	LED Pin (Active Low)
LED1	O	8	LED Pin (Active Low)
LED2	O	9	LED Pin (Active Low), shared with GPIO8

Table 5. LED Interface

5.6. Power Management Handshake Interface

Symbol	Type	Pin No	Description
WL_DIS#	I	37	Shared with GPIO9. This pin can externally shut down the RTL8821CU-CG WLAN function when WL_DIS# is pulled low. When this pin is pulled low, USB interface will be disabled. This pin can also be configured as the WLAN Radio-off function with host interface remaining connected.
BT_DIS#	I	56	Shared with GPIO11. This pin can externally shut down the RTL8821CU-CG BT function when BT_DIS# is pulled Low. When this pin is pulled low, USB interface will be also disabled. This pin can be also defined as the BT Radio-off function with host interface remaining connected.
CHIP_EN	I	47	This Pin Can externally shut down the RTL8821CU-CG (No Extra Power Switch Required). When this function is not required, external pull high is required.

Table 6. Power Management Handshake Interface

5.7. PCM Interface

Symbol	Type	Pin No	Description
PCM_IN	I	1	PCM data Input, shared with GPIO0
PCM_OUT	O	2	PCM data Out, shared with GPIO1
PCM_SYNC	O	3	PCM Synchronization control, shared with GPIO2
PCM_CLK	I/O	4	PCM Clock, shared with GPIO3

Table 7. PCM Interface

5.8. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	31	26M/40MHz OSC Input Input of 26M/40MHz Crystal Clock Reference
XO	O	32	Output of 26MHz/40MHz Crystal Clock Reference
SUS_CLK	I	10	Shared with EECS. External 32K or RTC clock input.
GPIO0	I/O	1	General Purpose Input/ Output Pin
GPIO1	I/O	2	General Purpose Input/ Output Pin
GPIO2	I/O	3	General Purpose Input/ Output Pin
GPIO3	I/O	4	General Purpose Input/ Output Pin
GPIO4	I/O	5	General Purpose Input/ Output Pin
GPIO5	I/O	6	General Purpose Input/ Output Pin
GPIO6	I/O	35	General Purpose Input/ Output Pin
GPIO7	I/O	36	General Purpose Input/ Output Pin
GPIO8	I/O	9	General Purpose Input/ Output Pin
GPIO9	I/O	37	General Purpose Input/ Output Pin
GPIO11	I/O	56	General Purpose Input/ Output Pin
GPIO13	I/O	39	General Purpose Input/ Output Pin
GPIO14	I/O	40	General Purpose Input/ Output Pin
NC		26	Not Connect

Table 8. Clock and Other Pins

5.9. Power Pins

Symbol	Type	Pin No	Description
LX_SPS	P	44	Switching Regulator Output
VD33_SPS	P	43	Switching Regulator Input
VD33_IO	P	42	VDD3.3V for Digital IO
VDD_IO_1	P	55	VDD for GPIO0~5 , GPIO11
VDD_IO	P	38	VDD for GPIO9,EECS,CHIP_EN,GPIO6,GPIO7,GPIO13,GPIO14

VD10D_WL	P	41	1.05V for WLAN digital power
VD10D_BT	P	54	1.05V for BT digital power
GND_SPS	P	45	Switching Regulator Ground
GND	P	27	GND
GND_V33USB	P	53	USB Ground
V10_USB	P	49	1.05V for USB
V33_USB	P	50	3.3V for USB
RREF	P	48	Precision Resistor for Bandgap
VD1_BT	P	13	VDD 1.05V for BT RF
VD33_PAD_BT	P	14	VDD 3.3V for BT PAD
VD1_SYN_BT	P	11	VDD 1.05V for BT synthesizer
VD33_SYN_BT	P	12	VDD 3.3V for BT synthesizer
VD33_PA_WL	P	23	VDD 3.3V for WLAN PA
VD33_PA_WL	P	24	VDD 3.3V for WLAN PA
VD1_RF_WL	P	21	VDD 1.05V for WLAN RF
VD1_RF_WL	P	28	VDD 1.05V for WLAN RF
VD1_SYN_WL	P	29	VDD 1.05V for WLAN synthesizer
VD33_SYN_WL	P	30	VDD 3.3V for WLAN synthesizer
VD33X	P	33	VDD 3.3V for crystal
VD10A	P	34	VDD 1.05V for crystal

Table 9. Power Pins

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

Table 10. Temperature Limit Ratings

6.2. DC Characteristics

6.2.1. Power Supply Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD10	1.05V Core Supply Voltage	0.945	1.05	1.155	V

Table 11. DC Characteristics

6.2.2. Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V _{IH}	Input high voltage	2.0	3.3	3.6	V
V _{IL}	Input low voltage	--	0	0.9	V
V _{OH}	Output high voltage	2.97	--	3.3	V
V _{OL}	Output low voltage	0	--	0.33	V

Table 12. 3.3V GPIO DC Characteristics

* 3.3V and 1.2V ripple < 100mV

7. Interface Timing Specification

7.1. USB Bus Timing during Power On Sequence

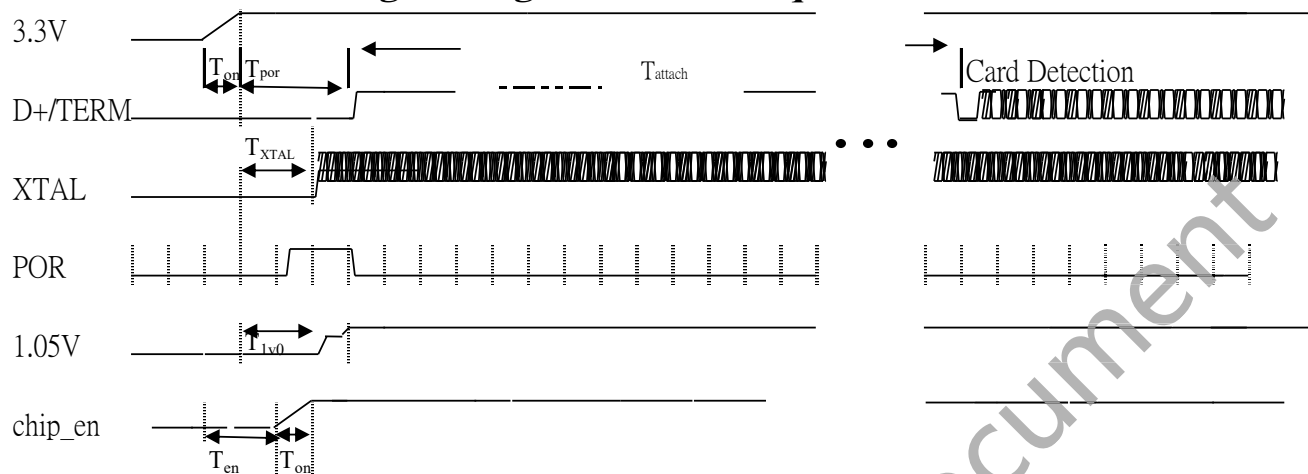


Figure 3. RTL8821CU-CG USB Bus Power On Sequence

T_{on}: The main power ramp up duration

T_{por}: The power on reset releases and power management unit executes power on tasks

T_{attach}: USB attach state. The duration from resistor attached to USB host starting card detection procedure

T_{xtal}: XTAL starts

T_{en}: Interval between the rising point of 3.3V and chip_en

The power on flow description:

After main 3.3V ramp up, the internal power on reset is released by power ready detection circuit and the power management unit will be enabled. The power management unit enables the internal regulator and clock circuits.

The power management unit also enables the USB circuits.

USB analog circuits attach registers to indicate the insertion of the USB device

Symbol	Unit	Min	Typical	Max
T _{on}	ms	--	1.5	5
T _{por}	ms	--	2	20
T _{xtal}	ms	--	1.5	8
T _{attach}	ms	100	250	--
T _{1v0}	ms	-	3	11
T _{en}	ms	0	0	5

Table 13. The typical timing range

7.2. PCM Interface Characteristics

The RTL8821CU-CG supports a PCM digital audio interface that is used for transmitting digital audio/voice data to/from the Audio Codec. Features are supported as below:

- Supports Master and Slave mode
- Programmable long/short Frame Sync
- Supports 8-bit A-law/ μ -law, and 13/16-bit linear PCM formats
- Supports sign-extension and zero-padding for 8-bit and 13-bit samples
- Supports padding of Audio Gain to 13-bit samples
- PCM Master Clock Output: 64, 128, 256, or 512kHz
- Supports SCO/ESCO link

7.2.1. PCM Format

FrameSync is the synchronizing function used to control the transfer of DAC_Data and ADC_Data. A Long FrameSync indicates the start of ADC_Data at the rising edge of FrameSync (Figure 4), and a Short FrameSync indicates the start of ADC_Data at the falling edge of FrameSync (Figure 5).

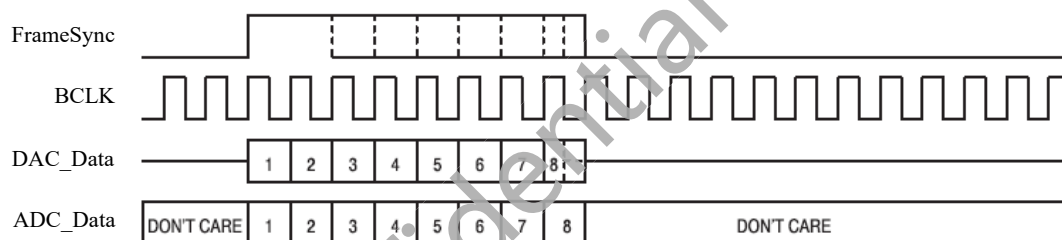


Figure 4. Long FrameSync

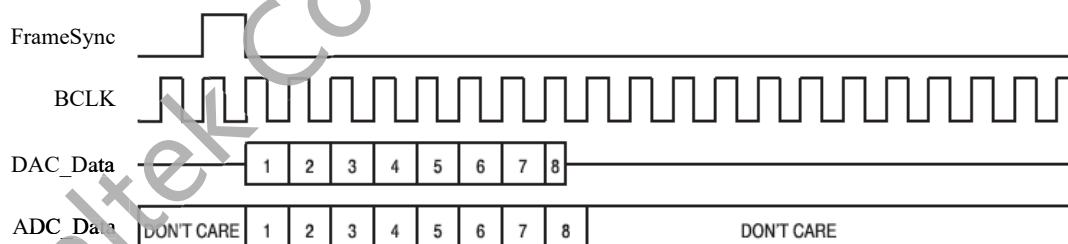


Figure 5. Short FrameSync

7.2.2. Sign Extension and Zero Padding for 8-Bit and 13-Bit Samples

For 16-bit linear PCM output, 3 or 8 unused bits may be sign extended/zero padded (Figure 6, Figure 7, Figure 8, Figure 9)

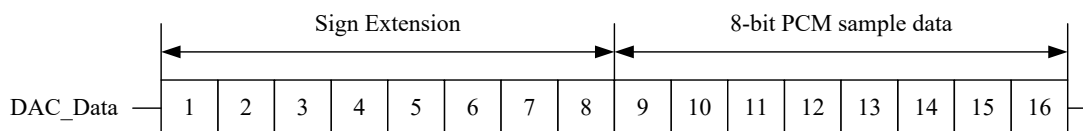


Figure 6. 16-Bit Output Data with 8-Bit PCM Sample Data and Sign Extension

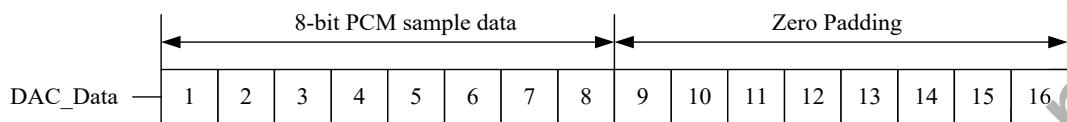


Figure 7. 16-Bit Output Data with 8-Bit PCM Sample Data and Zero Padding

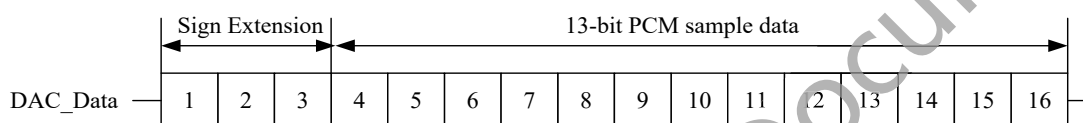


Figure 8. 16-Bit Output Data with 13-Bit PCM Sample Data and Sign Extension

For 16-bit linear PCM output, 3-bit programmable audio gain value can be padded to 13-bit sample data.

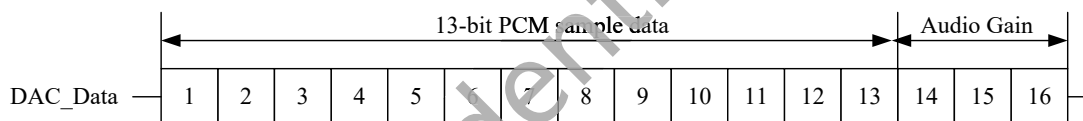


Figure 9. 16-Bit Output Data with 13-Bit PCM Sample Data and Audio Gain

7.2.3. PCM Interface Timing

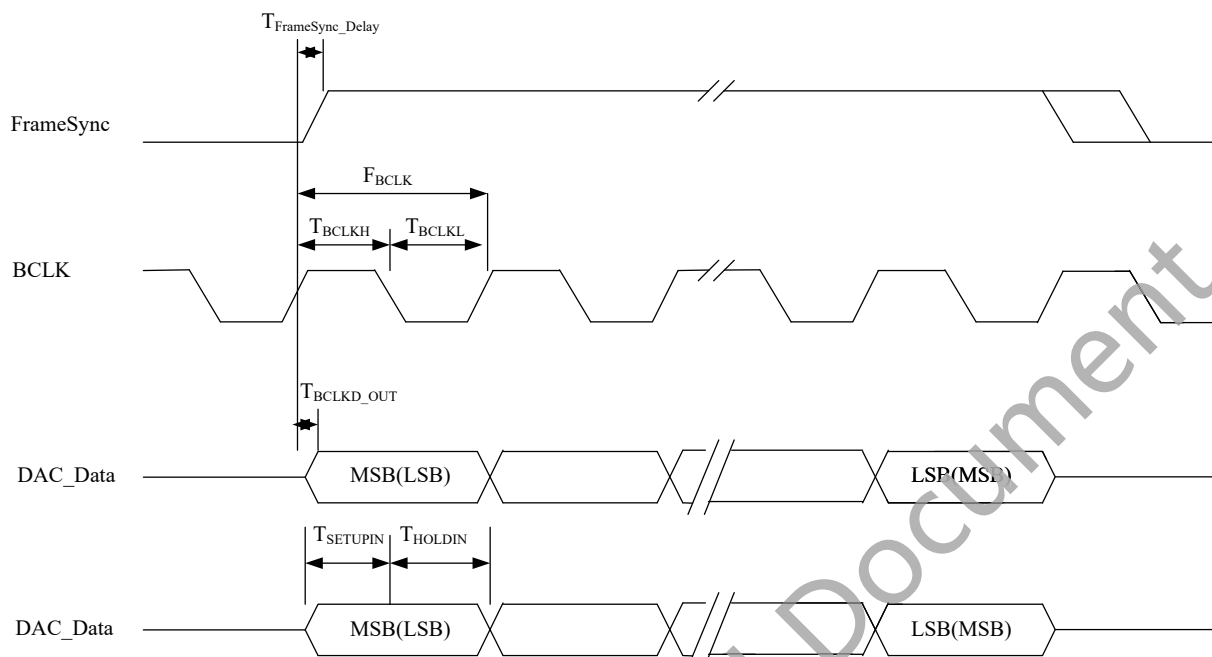


Figure 10. PCM Interface (Long FrameSync)

7.3. System Power Sequence

7.3.1. Power Off Sequence

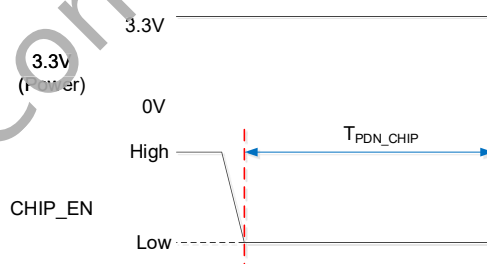
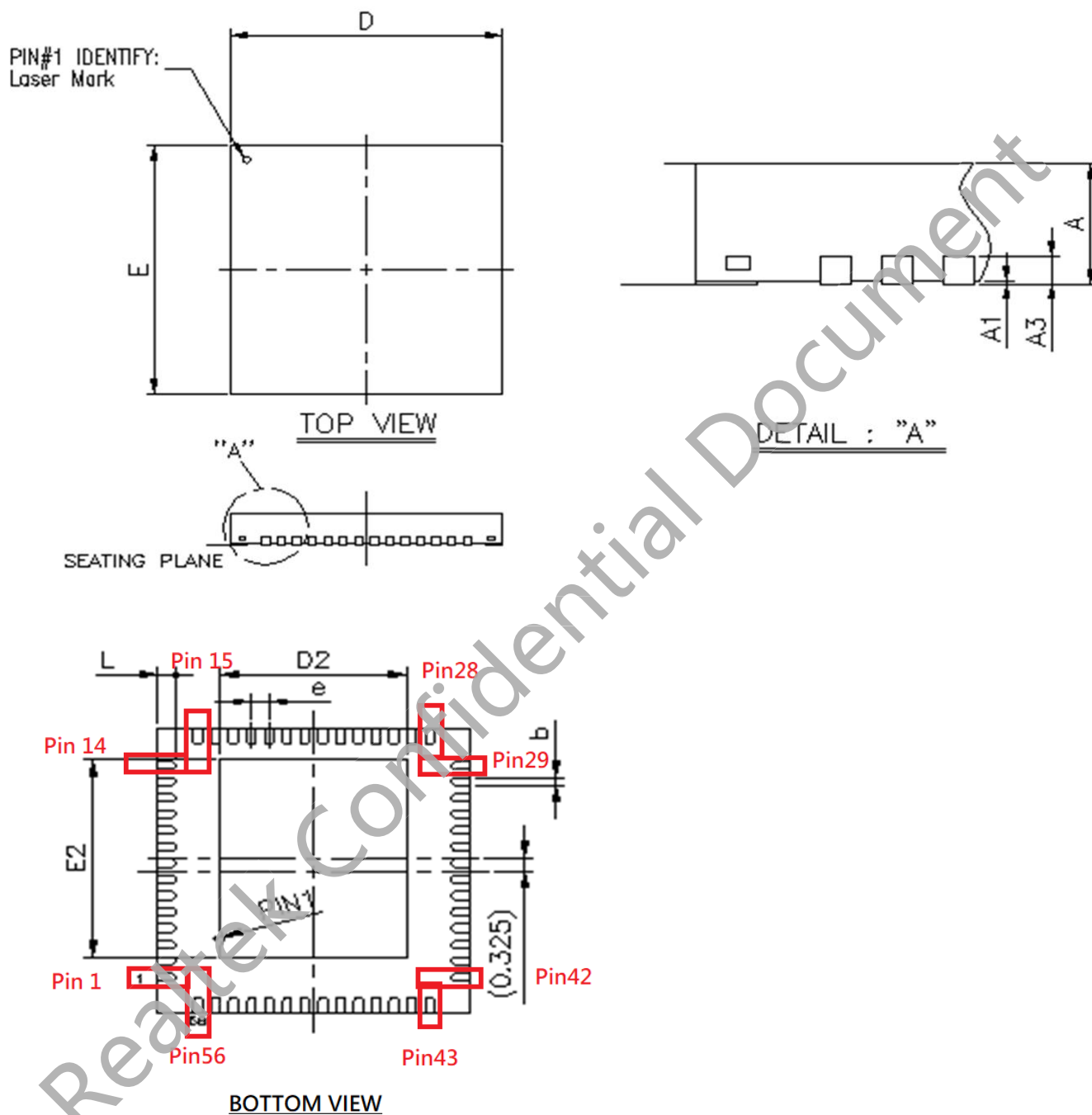


Figure 11. RTL8821CU-CG Power Off Sequence

Table 14. RTL8821CU-CG Power Off Timing Parameters

	Min	Typical	Max	Unit	Description
T_{PDN_CHIP}	100	100	X	ms	CHIP_EN keep low duration

CHIP_EN can externally shutdown the RTL8821CU-CG when CHIP_EN is pulled low. The keeping low duration must be more than T_{PDN_CHIP}



8.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A ₁	0.00	0.02	0.05	0.000	0.001	0.002
A ₃	0.2 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	7.00 BSC			0.276 BSC		
D ₂	4.10	4.20	4.30	0.161	0.165	0.169
E ₂	4.75	4.85	4.95	0.187	0.191	0.195
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes :

1. CONTROLLING DIMENSION : MILLIMETER(mm).
2. REFERENCE DOCUMENTL : JEDEC MO-220.

Table 15. Package Dimensions Notes

9. Ordering Information

Part Number	Package	Status
RTL8821CU-CG	QFN56 , 'Green' Package	Mass Production

Table 15. Ordering Information

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