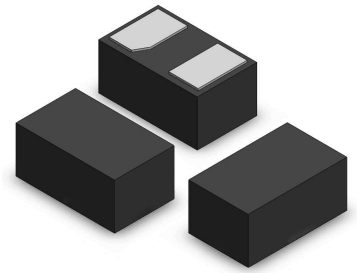
Transient Voltage Suppressors for ESD Protection

ESD3.3V02D-ULC

Description

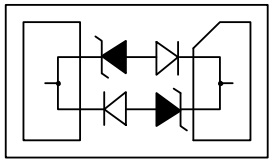
The ESD3.3V02D-ULC is ultra low capacitance TVS arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from over-voltage caused by ESD (electrostatic discharge), CDE (Cable Discharge Events), and EFT (electrical fast transients).



Feature

- Ultra small SMD package
- Ultra-Low capacitance
- Protects One Bidirectional I/O line
- Low clamping voltage
- Working voltages :3.3V
- Low leakage current
- IEC61000-4-2(ESD):±25kV (air discharge)
  ±20kV (contact discharge);

Functional Diagram



Applications

- USB 3.0 / USB 3.1 Interfaces
- HDMI 1.4 / HDMI 2.0 Interfaces
- Video Graphics Cards
- Notebooks, Desktops, and Servers
- Portable Instrumentation
- Industrial Controls
- Peripherals

Mechanical Data

- JEDEC 0201/DFN0603 Package
- Molding Compound Flammability Rating : UL 94V-O
- Weight 0.3 Milligrams(Approximate)
- Polarity: Color band denotes cathode end.
- Mounting position: Any

Mechanical Characteristics

Symbol	Parameter	Value	Units
P_{PP}	**Peak Pulse Power (tp=8/20μs waveform)**	96	Watts
T_L	**Lead Soldering Temperature**	260 (10 sec.)	ºC
T_{STG}	**Storage Temperature Range**	-55 to +150	ºC
T_J	**Operating Junction Temperature Range**	-40 to +125	ºC

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Electrical Characteristics (@ 25℃ Unless Otherwise Specified)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Reverse Working Voltage	V_{RWM}	--	--	--	3.3	V
Reverse Breakdown Voltage	V_{BR}	I_T=1mA;	4.5	--	--	V
Reverse Leakage Current	I_R	V_{RWM} =3.3V, T=25°C;	--	--	1	μA
Positive Clamping Voltage	V_C	I_{PP} =4.8A, T_P =8/20μs;	--	--	20	V
TLP Clamping Voltage	V_{CL}	I_{PP} =16A, T_P =100ns;	--	19.6	--	V
Junction capacitance	C_J	V_R = 0V, f = 1MHz;	--	--	0.25	pF

Characteristic Curves

Fig1. 8/20μs Pulse Waveform

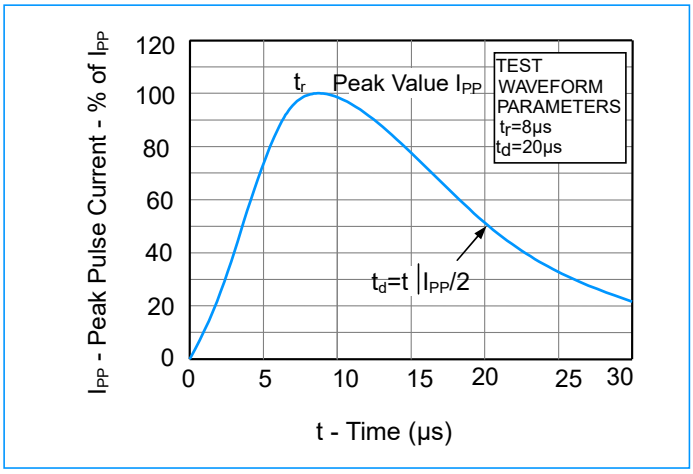


Fig2. Power Rating Derating Curve

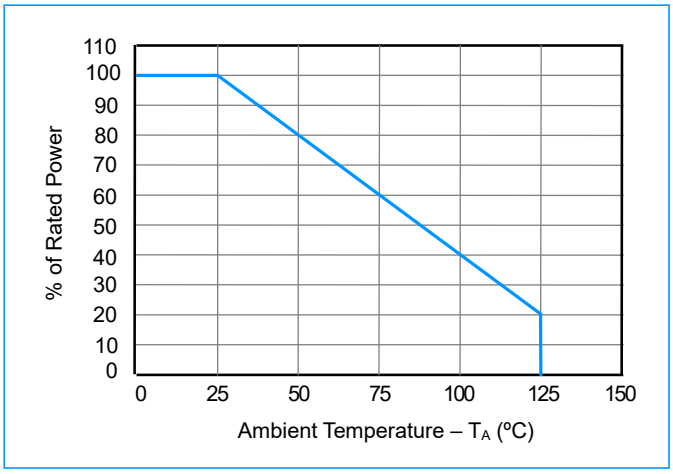


Fig3. Clamping Voltage vs. Peak Pulse Current

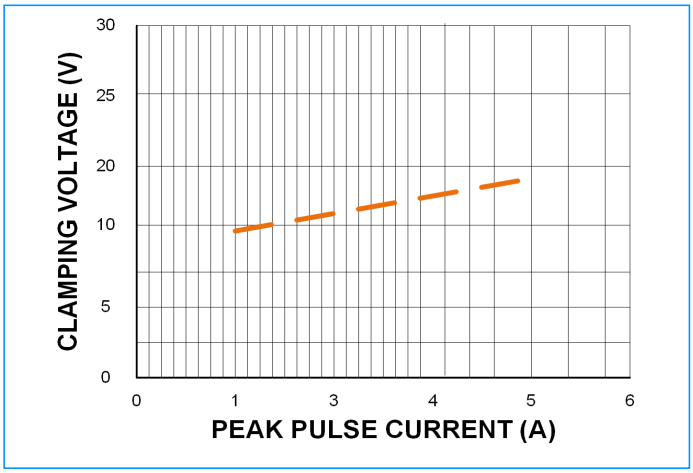
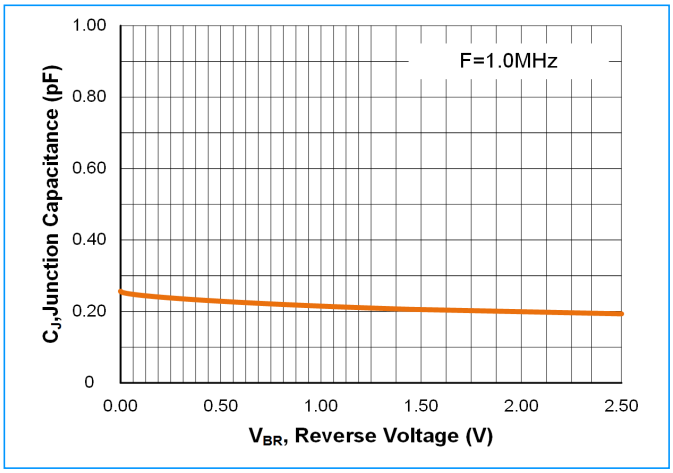


Fig4. Typic Capacitance vs. Reverse Voltage



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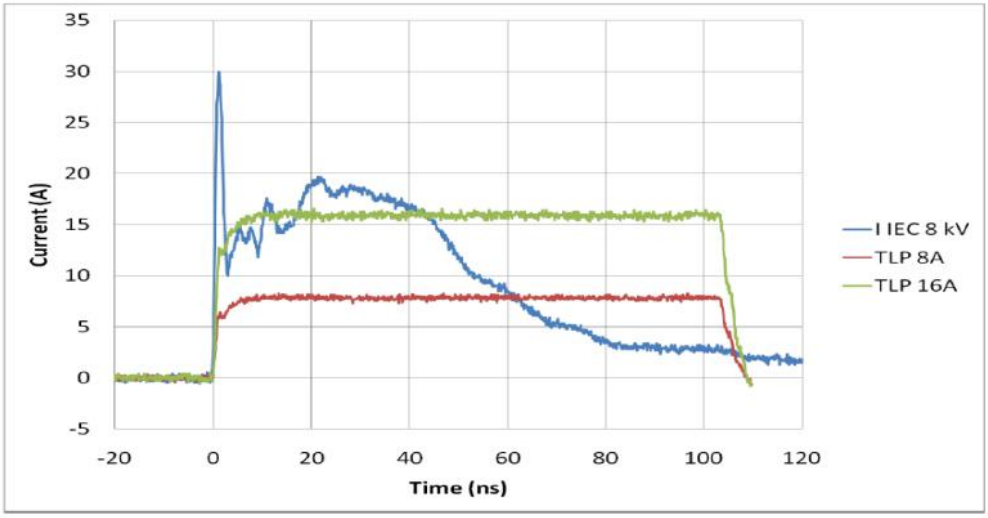
Transmission Line Pulse (TLP)

Transmission Line Pulse (TLP) is a measurement technique used in the Electrostatic Discharge (ESD) arena to characterize performance attributes of devices under ESD stresses. TLP is able to obtain current versus voltage (I−V) curves in which each data point is obtained with a 100 ns long pulse, with currents up to 40 A. TLP was first used in the ESD field to study human body model (HBM) in integrated circuits, but it is an equally valid tool in the field of system level ESD. The applicability of TLP to system level ESD is illustrated in Figure 1, which compares an 8 KV IEC 61000−4−2 current waveform with TLP current pulses of 8 and 16 A. The current levels and time duration for the pulses are similar and the initial rise time for the TLP pulse is comparable to the rise time of the IEC 61000−4−2's initial current spike. This application note will give a basic introduction to TLP measurements and explain the datasheet parameters extracted from TLP for SDI Technology's protection products.



Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

Comparison of a Current Waveform of IEC 61000−4−2 with TLP Pulses at 8 and 16 A.

The IEC 61000−4−2 ESD waveforms is true to the Standard and is shown here as captured on an oscilloscope. The points A, B, and C show the points on the waveforms specified in IEC 61000−4−2.

Transmission Line Pulse (TLP) Version.

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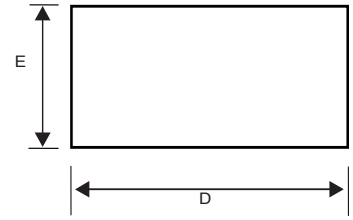
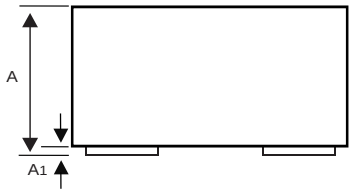
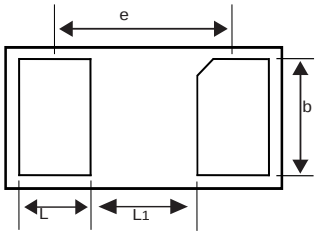
0201/DFN0603 Package Outline & Dimensions

0201/DFN0603

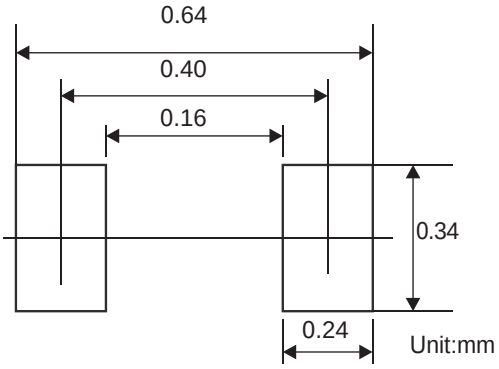






Symbol	Millimeters		
	Min	Nom	Max
A	0.270	0.300	0.340
A1	0	0.020	0.050
D	0.550	0.600	0.650
E	0.250	0.300	0.350
e	0.340REF		
L	0.140	0.180	0.240
b	0.200	0.250	0.300
L1	0.150REF		

Suggested PAD Layout



Ordering Information

Device	Marking	Package	Quantity	Reel Size
ESD3.3V02D-ULC	3L	0201/DFN0603	10,000pcs/Reel	7 inch

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