

NTMFS4833NA

Power MOSFET

30 V, 191 A, Single N-Channel, SO-8FL

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These are Pb-Free Devices

Applications

- CPU Power Delivery
- DC-DC Converters
- Low Side Switching

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DS}	30	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$T_A = 25^\circ\text{C}$	I_D	28	A
	$T_A = 85^\circ\text{C}$		20.5	
Power Dissipation $R_{\theta JA}$ (Note 1)	$T_A = 25^\circ\text{C}$	P_D	2.7	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)	$T_A = 25^\circ\text{C}$	I_D	16	A
	$T_A = 85^\circ\text{C}$		12	
Power Dissipation $R_{\theta JA}$ (Note 2)	$T_A = 25^\circ\text{C}$	P_D	1.1	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$T_C = 25^\circ\text{C}$	I_D	191	A
	$T_C = 85^\circ\text{C}$		138	
Power Dissipation $R_{\theta JC}$ (Note 1)	$T_C = 25^\circ\text{C}$	P_D	113.6	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10 \mu\text{s}$	I_{DM}	288	A
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode) (Note 3)		I_S	104	A
Pulse Source Current (Body Diode) (Note 3)		I_{SM}	312	A
Drain to Source dV/dt		dV/dt	6	V/ns
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $V_{DD} = 30 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_L = 35 \text{ A}_{pk}$, $L = 1.0 \text{ mH}$, $R_G = 25 \Omega$)		EAS	612.5	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

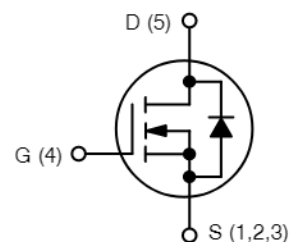
1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size (Cu area = 50 mm² [1 oz]).
3. Guaranteed by design.



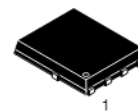
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$V_{(BR)DS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	2.0 m Ω @ 10 V	191 A
	3.0 m Ω @ 4.5 V	

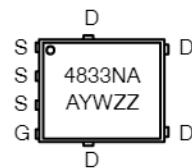


N-CHANNEL MOSFET



**SO-8 FLAT LEAD
CASE 488AA
STYLE 1**

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4833NAT1G	SO-8FL (Pb-Free)	1500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Typ	Max	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.0	1.1	°C/W
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	43	45.6	
Junction-to-Ambient – $t < 10s$ (Note 4)	$R_{\theta JA}$	16	17.1	
Junction-to-Ambient – Steady State (Note 5)	$R_{\theta JA}$	110	117.4	

4. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.

5. Surface-mounted on FR4 board using the minimum recommended pad size. (Cu area = 50 mm² [1 oz])

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			17		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\text{ }\mu\text{A}$	1.5	1.9	2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			7.12		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V to } 11.5\text{ V}$	$I_D = 30\text{ A}$		1.4	m Ω
			$I_D = 15\text{ A}$		1.4	
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$		2.1	
			$I_D = 15\text{ A}$		2.1	
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		30		S

CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 12\text{ V}$	2700	5100	7500	pF
Output Capacitance	C_{OSS}		800	1200	1600	
Reverse Transfer Capacitance	C_{RSS}			580	1300	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$	7.4	37	58	nC
Threshold Gate Charge	$Q_{G(TH)}$			6.0		
Gate-to-Source Charge	Q_{GS}			15	32	
Gate-to-Drain Charge	Q_{GD}		7.0	14	21	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$	22	86	150	nC

SWITCHING CHARACTERISTICS (Note 7)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\text{ }\Omega$	16	23	30	ns
Rise Time	t_r		15	50	85	
Turn-Off Delay Time	$t_{d(OFF)}$		10	36	32	
Fall Time	t_f			24	71	
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\text{ }\Omega$	8.5	12.5	16.5	ns
Rise Time	t_r		15	30	45	
Turn-Off Delay Time	$t_{d(OFF)}$		16	51	86	
Fall Time	t_f			14	42	

6. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

7. Switching characteristics are independent of operating junction temperatures.

NTMFS4833NA

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V},$ $I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$		0.8	1.0	V
			$T_J = 125^\circ\text{C}$		0.63	0.9	
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$			39	65	ns
Charge Time	t_a				19		
Discharge Time	t_b				19		
Reverse Recovery Charge	Q_{RR}				36	57	nC

PACKAGE PARASITIC VALUES

Source Inductance	L_S	$T_A = 25^\circ\text{C}$		0.50		nH
Drain Inductance	L_D			0.005		nH
Gate Inductance	L_G			1.84		nH
Gate Resistance	R_G			0.6	1.3	Ω

6. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

7. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

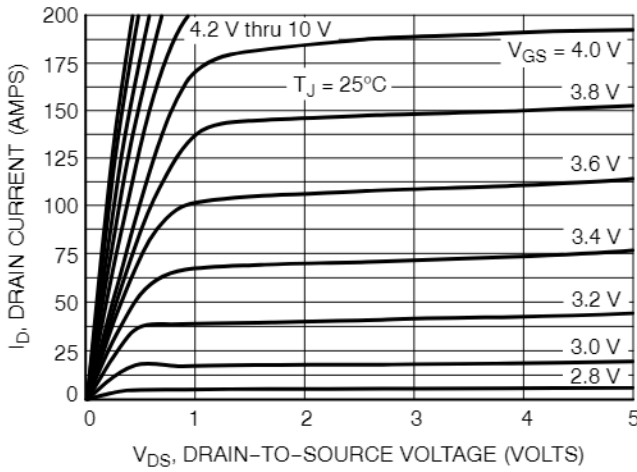


Figure 1. On-Region Characteristics

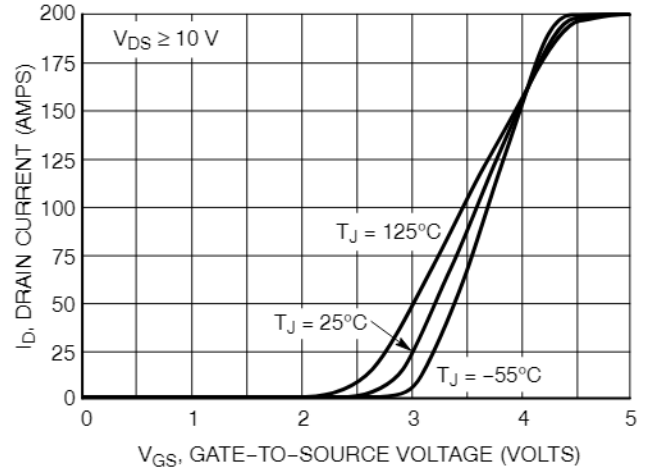


Figure 2. Transfer Characteristics

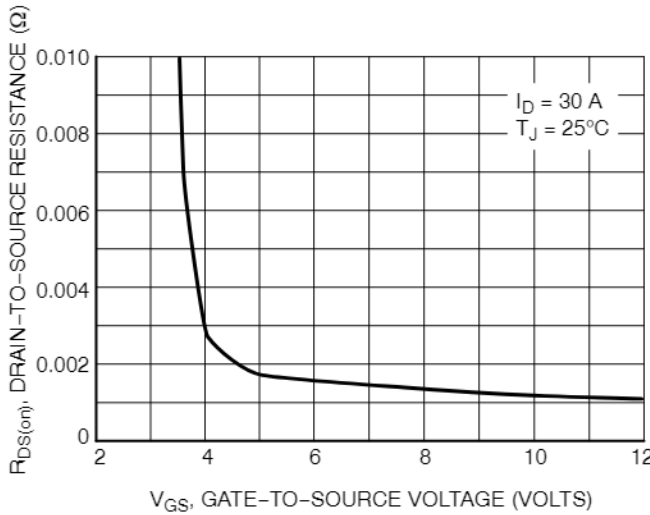


Figure 3. On-Resistance vs. Gate-to-Source Voltage

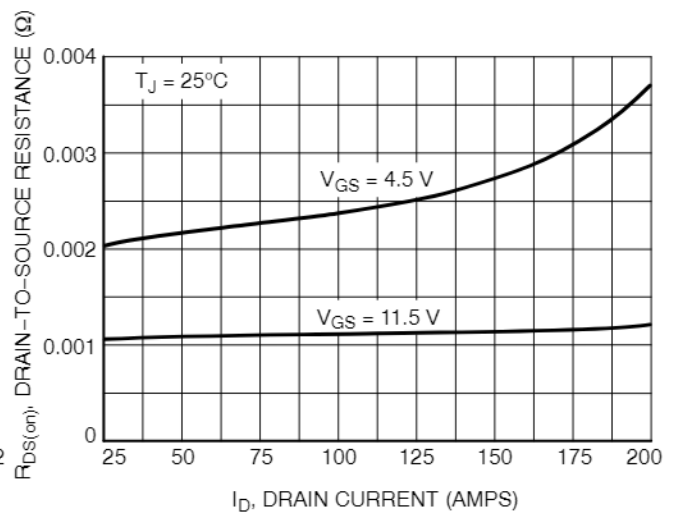


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

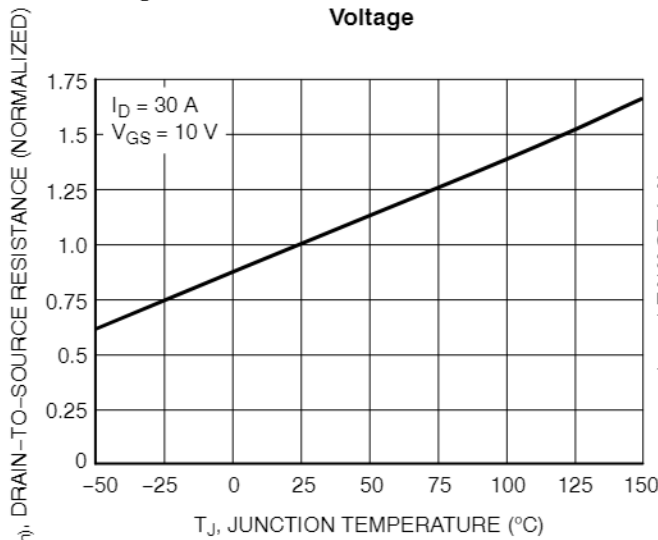


Figure 5. On-Resistance Variation with Temperature

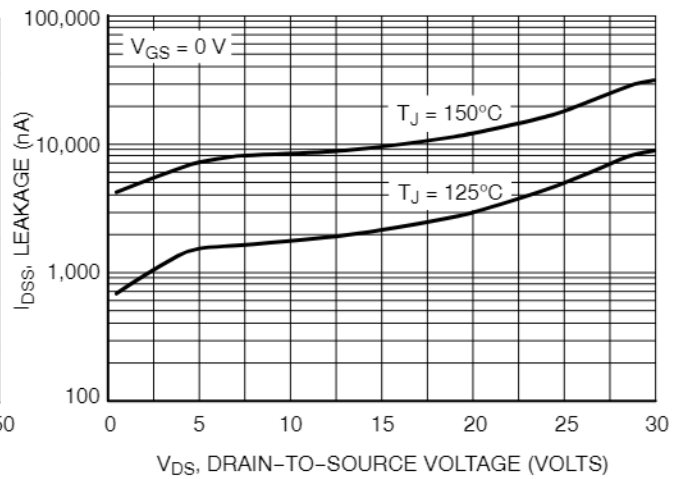
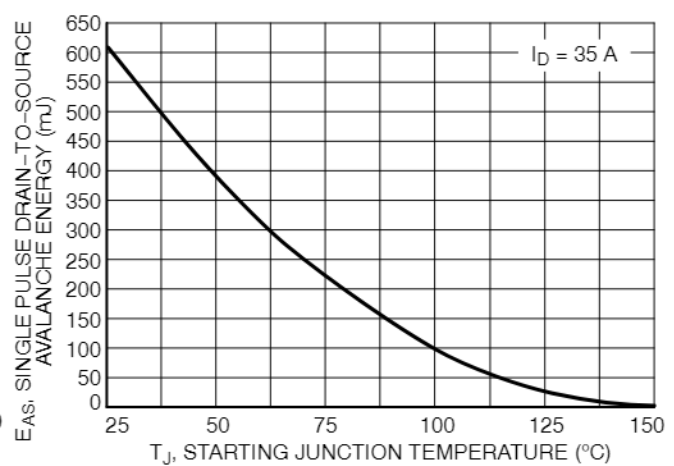
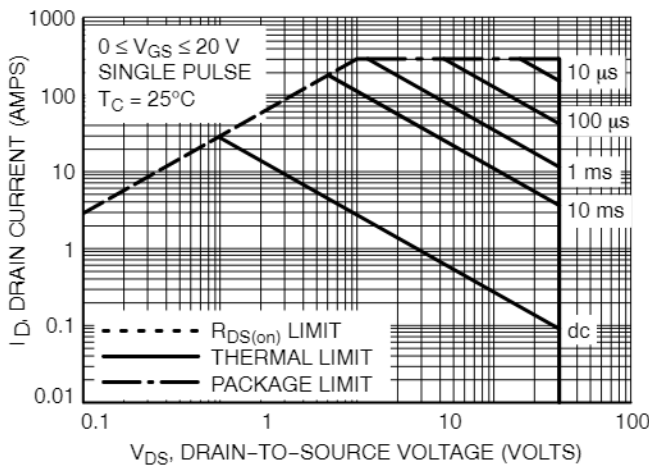
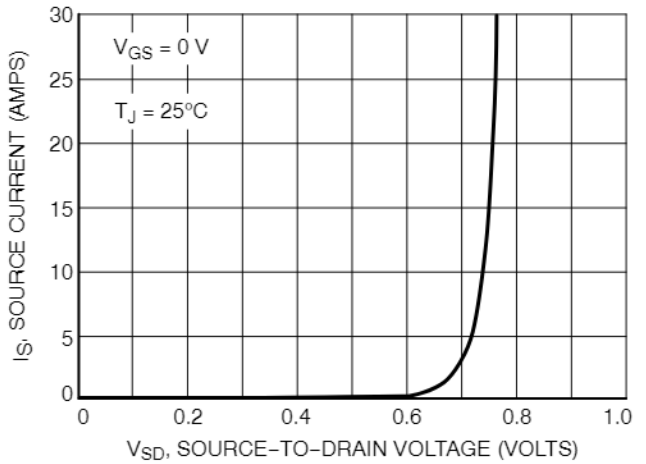
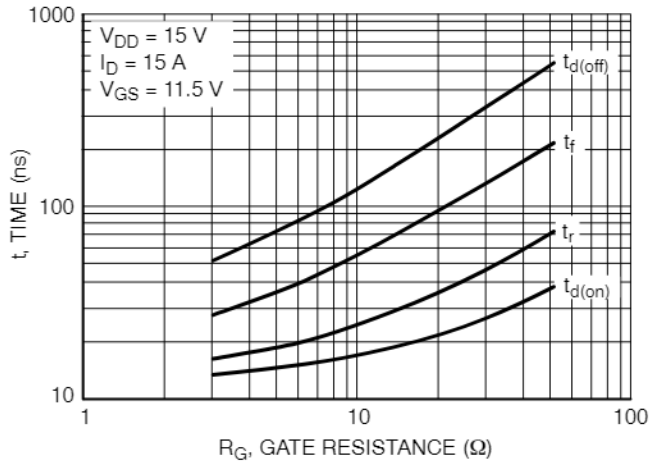
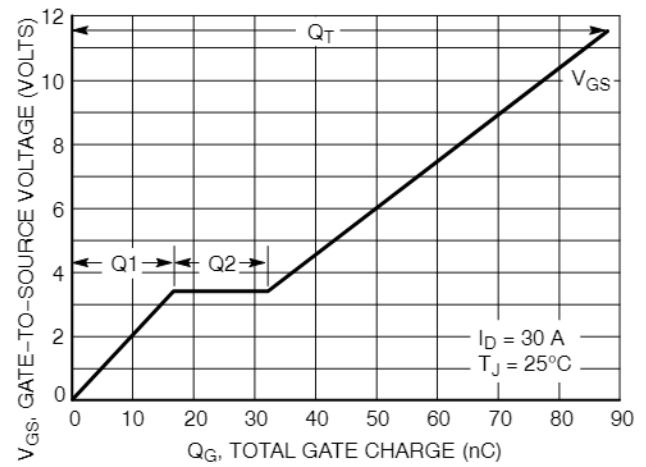
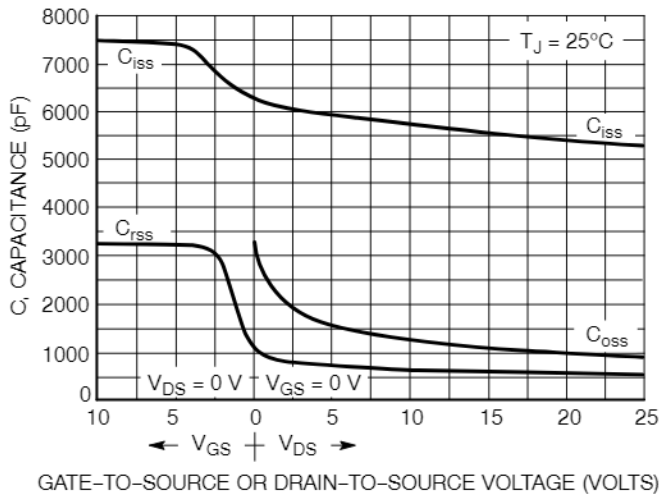


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES



TYPICAL PERFORMANCE CURVES

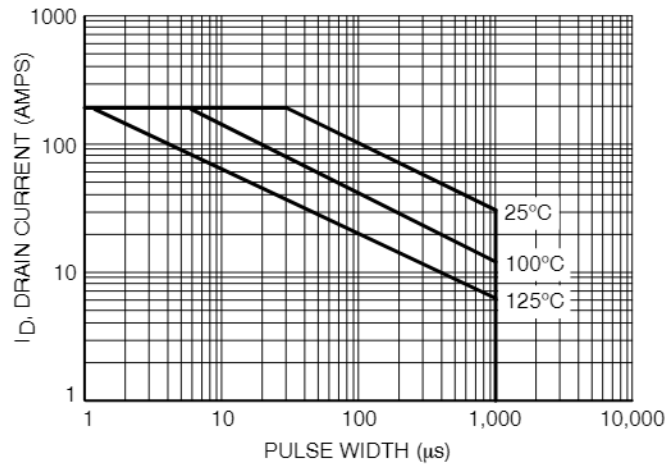


Figure 13. Avalanche Characteristics

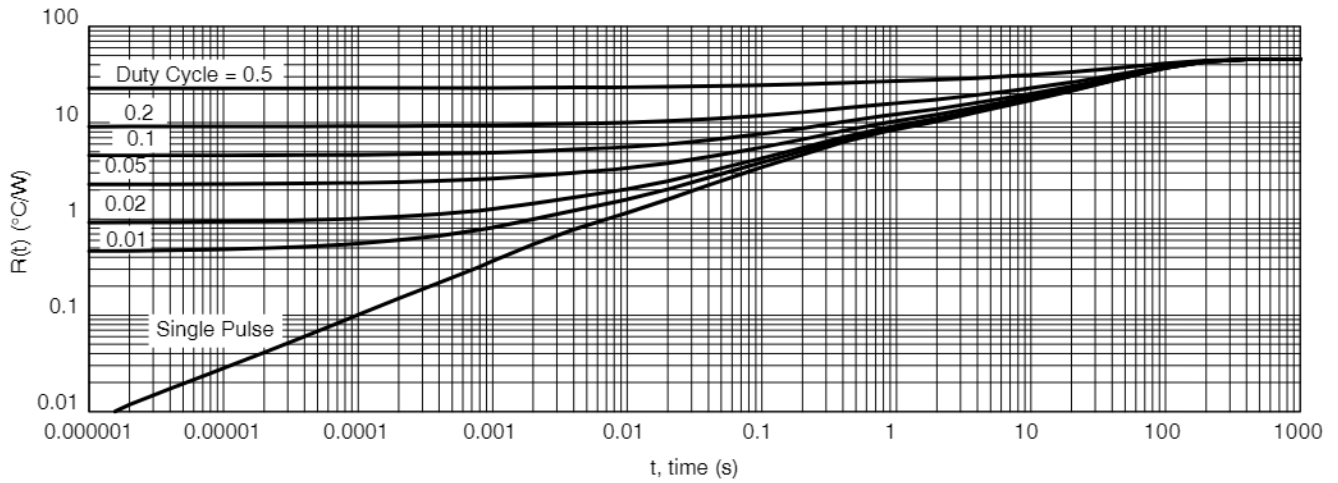


Figure 14. FET Thermal Response

PACKAGE DIMENSIONS

MECHANICAL DRAWING OF THE 486AA MICROPROCESSOR PACKAGE

TOP VIEW: Shows the package outline with dimensions D, D1, E1, E, and pin locations 1, 2, 3, 4. Features include a 2X hole with a 0.20 diameter and a 2X hole with a 0.20 diameter. A 2X hole with a 0.20 diameter is also shown.

SIDE VIEW: Shows the package profile with dimensions A, A1, and a 0.10 diameter hole. A detail A is indicated.

DETAIL A: A circular detail showing the internal structure of the package, including a 4X hole with a 0.20 diameter and a 3X hole with a 0.20 diameter. A seating plane is indicated.

SOLDERING FOOTPRINT*: Shows the dimensions for the soldering footprint, including 3X holes with a 1.270 diameter and 4X holes with a 0.750 diameter. Other dimensions include 0.965, 1.330, 2X 0.495, 3.200, 0.905, 0.475, 1.530, 4.560, and 4.530.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	---	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
Ø	0.0	---	12.0

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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