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Vishay Siliconix

# P-Channel 100 V (D-S) 175 °C MOSFET



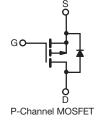
PRODUCT SUMMARY				
V <sub>DS</sub> (V)	-100			
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS}$ = -10 V	0.043			
$R_{DS(on)}$ max. ( $\Omega$ ) at $V_{GS}$ = -4.5 V	0.048			
Q <sub>g</sub> typ. (nC)	54			
I <sub>D</sub> (A) <sup>a</sup>	-37			
Configuration	Single			

#### **FEATURES**

- TrenchFET® Power MOSFET
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912







ORDERING INFORMATION	
Package	DPAK (TO-252)
Lead (Pb)-free and halogen-free	SUD50P10-43L-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25 °C, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V <sub>DS</sub>	-100	V	
Gate-source voltage		V <sub>GS</sub>	± 20	7 v	
	T <sub>C</sub> = 25 °C		-37.1 <sup>a</sup>		
Continuous drain surrent (T = 175 °C) h	T <sub>C</sub> = 125 °C	1 , [	-31 <sup>a</sup>		
Continuous drain current (T <sub>J</sub> = 175 °C) <sup>b</sup>	T <sub>A</sub> = 25 °C	I <sub>D</sub>	-9.2 <sup>b, c</sup>		
	T <sub>A</sub> = 125 °C	1	-7.7 b, c	1	
Pulsed drain current		I <sub>DM</sub>	-40	Α Α	
Continuous source surrent (diada conduction)	T <sub>C</sub> = 25 °C		-50 <sup>a</sup>		
Continuous source current (diode conduction)	T <sub>A</sub> = 25 °C	l <sub>S</sub> –	-6.9 b, c		
Avalanche current	. 0.4	I <sub>AS</sub>	-35		
Single pulse avalanche energy	L = 0.1 mH	E <sub>AS</sub>	61	mJ	
	T <sub>C</sub> = 25 °C		136		
Maximum power dissipation	T <sub>C</sub> = 70 °C	1 , [	95	10/	
	T <sub>A</sub> = 25 °C	P <sub>D</sub>	8.3 b, c	W	
	T <sub>A</sub> = 70 °C	1 -	5.8 b, c	7	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
lunction to embiant 8	t ≤ 10 s	D	15	18	
Junction-to-ambient <sup>a</sup>	Steady state	$R_{thJA}$	40	50	°C/W
Junction-to-case (drain)		R <sub>thJC</sub>	0.85	1.1	

#### Note

- a. Package limited
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 sd. Maximum under steady state conditions is 40 °C/W

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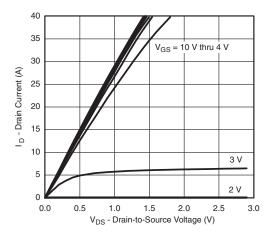
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static					<u> </u>	
Drain-source breakdown voltage	V <sub>DS</sub>	VGS = 0 V, I <sub>D</sub> = -250 μA	-100	_	_	V
VDS temperature coefficient	$\Delta V_{DS}/T_{J}$			-109	-	1400
VGS(th) temperature coefficient	$\Delta V_{GS(th)}/T_J$	- I <sub>D</sub> = -250 μA		5.9	-	mV/°C
Gate-source threshold voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}, I_D = -250 \mu A$	-1	-	- 3	V
Gate-source leakage	I <sub>GSS</sub>	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
		V <sub>DS</sub> = -100 V, V <sub>GS</sub> = 0 V	-	-	-1	
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -100 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 55 °C	-	-	-10	μA
On-state drain current a	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, V_{GS} = -10 \text{ V}$	-40	-	-	Α
5	_	$V_{GS} = -10 \text{ V}, I_D = -9.2 \text{ A}$	-	0.036	0.043	
Drain-source on-state resistance a	R <sub>DS(on)</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -7.7 A	-	0.040	0.048	Ω
Forward transconductance a	9 <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -9.2 A		38	-	S
Dynamic <sup>b</sup>			I.	•	•	
Input capacitance	C <sub>iss</sub>		-	4600	-	
Output capacitance	C <sub>oss</sub>	$V_{DS} = -50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	230	-	pF
Reverse transfer capacitance	C <sub>rss</sub>		-	175	-	1
Talal and a share a	0	$V_{DS} = -50 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -9.2 \text{ A}$	-	106	160	
Total gate charge	Qg		-	54	81	
Gate-source charge	$Q_{gs}$	$V_{DS} = -50 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -9.2 \text{ A}$	-	14	-	nC
Gate-drain charge	Q <sub>gd</sub>		-	26	-	
Gate resistance	$R_{g}$	f = 1 MHz	-	4	-	Ω
Turn-on delay time	t <sub>d(on)</sub>		-	15	25	
Rise time	t <sub>r</sub>	$V_{DD} = -50 \text{ V}, R_{L} = 6.5 \Omega$	-	20	30	1
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong -7.7 \text{ A}, V_{GEN} = -10 \text{ V}, R_g = 1 \Omega$	-	110	165	ns
Fall time	t <sub>f</sub>		-	100	150	1
Turn-on delay time	t <sub>d(on)</sub>		-	42	65	
Rise time	t <sub>r</sub>	$V_{DD} = -50 \text{ V, R}_{L} = 6.5 \Omega$	-	160	240	
Turn-off delay time	t <sub>d(off)</sub>	$I_D \cong -7.7 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$	-	100	150	ns
Fall time	t <sub>f</sub>		-	100	150	1
Drain-source body diode characteristics						
Continuous source-drain diode current	Is	T <sub>C</sub> = 25 °C	-	-	-50	
Pulse diode forward current <sup>a</sup>	I <sub>SM</sub>	1	-	-	-40	A
Body diode voltage	$V_{SD}$	I <sub>S</sub> = - 7.7 A	-	-0.8	-1.2	V
Body diode reverse recovery time	t <sub>rr</sub>		-	60	90	ns
Body diode reverse recovery charge	Q <sub>rr</sub>	7.7.4. divide 100.4/15 T.L. 05.00	-	150	225	nC
Reverse recovery fall time	ta	l <sub>F</sub> = -7.7 A, dl/dt = 100 A/μs, TJ = 25 °C	-	46	-	
Reverse recovery rise time	t <sub>b</sub>		_	14	-	ns

#### Notes

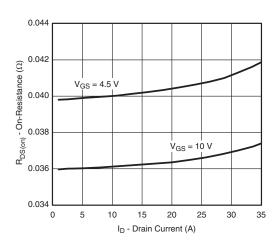
- a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

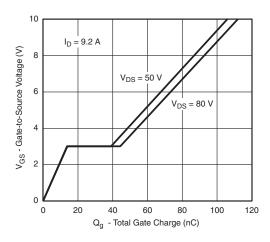




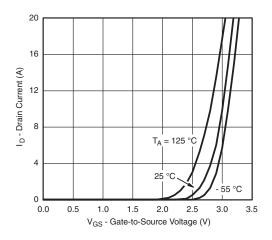
#### **Output Characteristics**



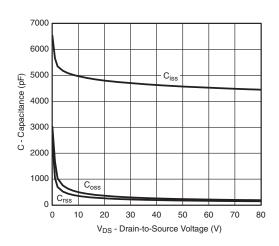
### On-Resistance vs. Drain Current and Gate Voltage



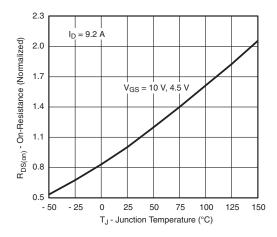
**Gate Charge** 



**Transfer Characteristics** 

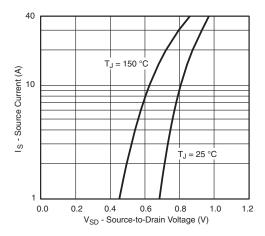


Capacitance

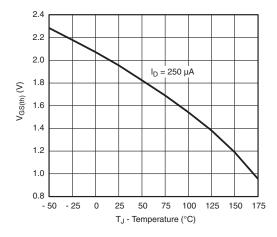


On-Resistance vs. Junction Temperature

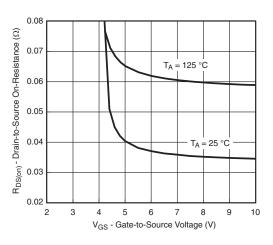




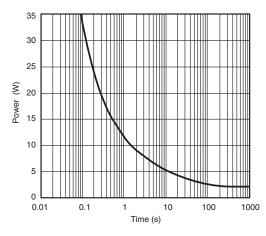
#### Source-Drain Diode Forward Voltage



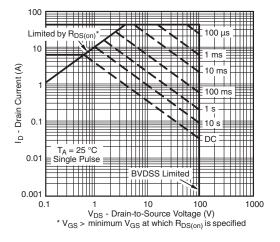
**Threshold Voltage** 



On-Resistance vs. Gate-to-Source Voltage

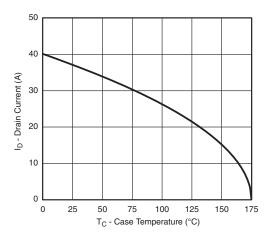


Single Pulse Power, Junction-to-Ambient

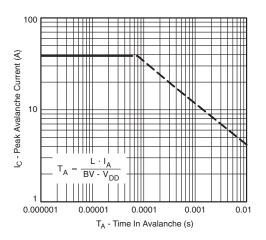


Safe Operating Area, Junction-to-Ambient

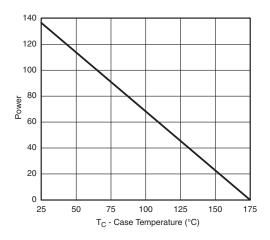




### Current Derating <sup>a</sup>



Single Pulse Avalance Capability

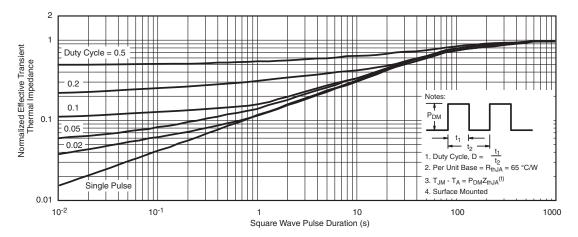


Single Pulse Power, Junction-to-Ambient

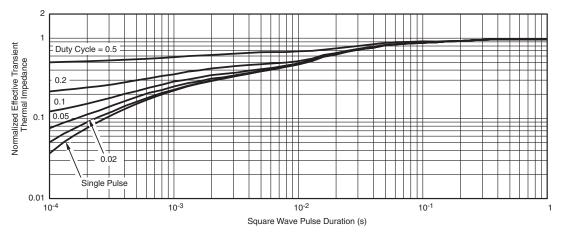
#### Note

a. The power dissipation P<sub>D</sub> is based on T<sub>J</sub> max. = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit





#### Normalized Thermal Transient Impedance, Junction-to-Ambient



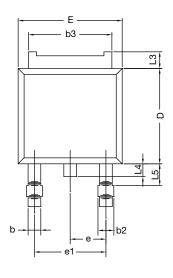
Normalized Thermal Transient Impedance, Junction-to-Case

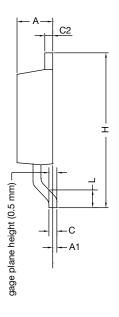
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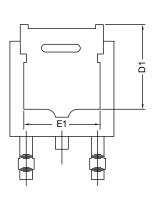


# **TO-252AA Case Outline**

## **VERSION 1: FACILITY CODE = Y**







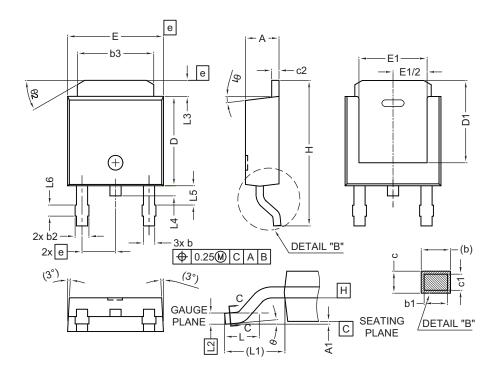
	MILLIMETERS		
DIM.	MIN.	MAX.	
А	2.18	2.38	
A1	-	0.127	
b	0.64	0.88	
b2	0.76	1.14	
b3	4.95	5.46	
С	0.46	0.61	
C2	0.46	0.89	
D	5.97	6.22	
D1	4.10	-	
Е	6.35	6.73	
E1	4.32	=	
Н	9.40	10.41	
е	2.28 BSC		
e1	4.56 BSC		
L	1.40	1.78	
L3	0.89	1.27	
L4	-	1.02	
L5	1.01	1.52	

#### Note

• Dimension L3 is for reference only



#### **VERSION 2: FACILITY CODE = N**



	MILLIMETERS		
DIM.	MIN.	MAX.	
А	2.18	2.39	
A1	-	0.13	
b	0.65	0.89	
b1	0.64	0.79	
b2	0.76	1.13	
b3	4.95	5.46	
С	0.46	0.61	
c1	0.41	0.56	
c2	0.46	0.60	
D	5.97	6.22	
D1	5.21	-	
E	6.35	6.73	
E1	4.32	-	
е	2.29 BSC		
Н	9.94	10.34	

	MILLIMETERS		
DIM.	MIN.	MAX.	
L	1.50	1.78	
L1	2.74	ł ref.	
L2	0.51	BSC	
L3	0.89	1.27	
L4	-	1.02	
L5	1.14	1.49	
L6	0.65	0.85	
θ	0°	10°	
θ1	0°	15°	
θ2	25°	35°	

#### Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022

DWG: 5347



# **RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)**



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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