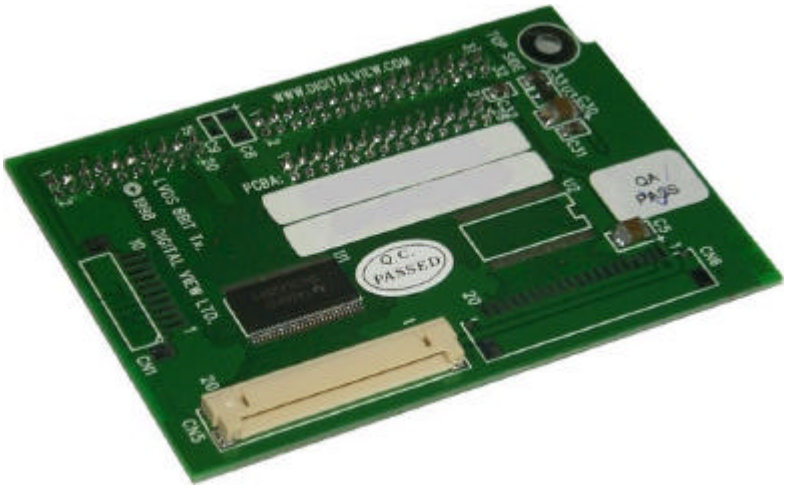
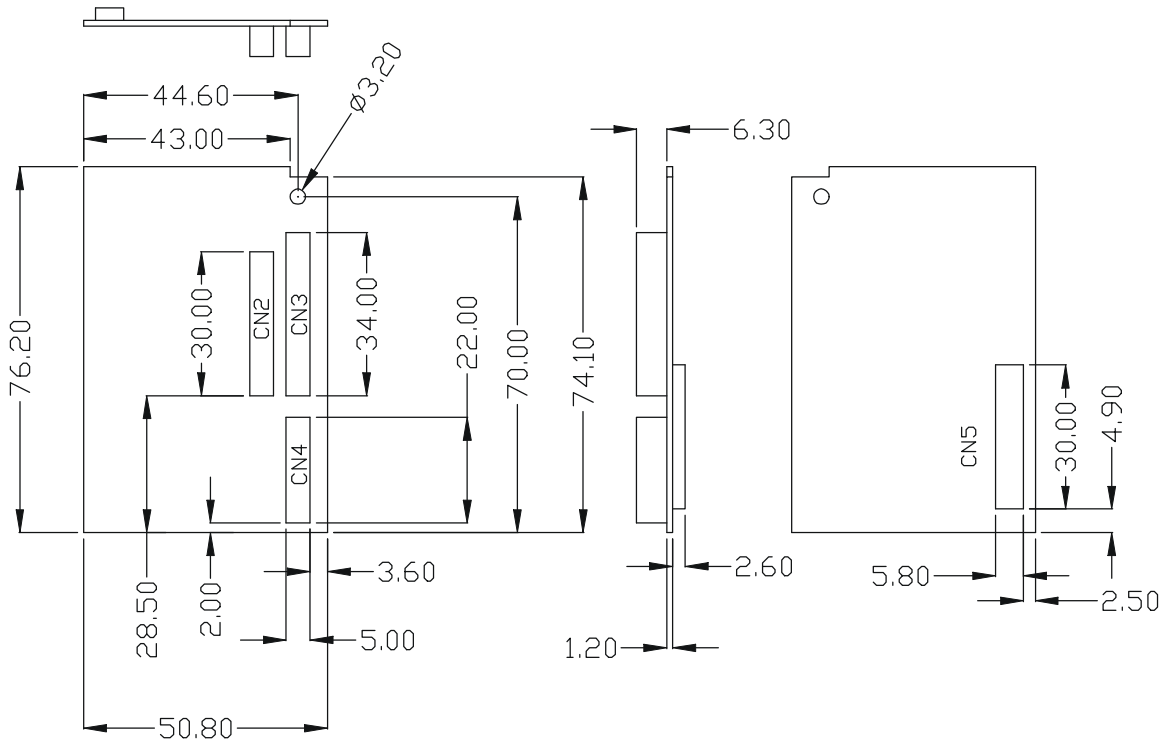
LVDS Add On Board

The LVDS add-on board of P/N : 4164702-10 designs for single pixel LVDS panel.



Mechanical drawing



Connector pin assignment :

CN5 – Panel connector: HIROSE DF14-20P-1.25

PIN	SYMBOL	DESCRIPTION
1	VLCD	Panel power supply
2	VLCD	Panel power supply
3	GND	Ground
4	GND	Ground
5	/OUT00	Negative differential LVDS data 00
6	OUT00	Positive differential LVDS data 00
7	GND	Ground
8	/OUT01	Negative differential LVDS data 01
9	OUT01	Positive differential LVDS data 01
10	GND	Ground
11	/OUT02	Negative differential LVDS data 02
12	OUT02	Positive differential LVDS data 02
13	GND	Ground
14	/CLKOUT0	Negative LVDS clock 0
15	CLKOUT0	Positive LVDS clock 0
16	GND	Ground
17	/OUT03	Negative differential LVDS data 03
18	OUT03	Positive differential LVDS data 03
19	GND	Ground
20	NC	No connection

CN2 – Panel connector: HIROSE DF11-28DS-2DSA

PIN	SYMBOL	DESCRIPTION
1	GND	Ground
2	GND	Ground
3	ER2	Even data bit R2
4	OR2	Odd data bit R2
5	ER3	Even data bit R3
6	OR3	Odd data bit R3
7	ER4	Even data bit R4
8	OR4	Odd data bit R4
9	ER5	Even data bit R5
10	OR5	Odd data bit R5
11	EG2	Even data bit G2
12	OG2	Odd data bit G2
13	EG3	Even data bit G3
14	OG3	Odd data bit G3
15	EG4	Even data bit G4
16	OG4	Odd data bit G4
17	EG5	Even data bit G5
18	OG5	Odd data bit G5
19	EB2	Even data bit B2
20	OB2	Odd data bit B2
21	EB3	Even data bit B3
22	OB3	Odd data bit B3
23	EB4	Even data bit B4
24	OB4	Odd data bit B4
25	EB5	Even data bit B5
26	OB5	Odd data bit B5
27	GND	Ground
28	GND	Ground

CN3 – Panel connector: HIROSE DF11-32DS-2DSA

PIN	SYMBOL	DESCRIPTION
1	NC	No Connection
2	NC	No Connection
3	VLCD12	12V VLCD
4	NC	No connection
5	GND	Ground
6	GND	Ground
7	ER6	Even data bit R6
8	OR6	Odd data bit R6
9	ER7	Even data bit R7 (MSB)
10	OR7	Odd data bit R7 (MSB)
11	EG6	Even data bit G6
12	OG6	Odd data bit G6
13	EG7	Even data bit G7 (MSB)
14	OG7	Odd data bit G7 (MSB)
15	EB6	Even data bit B6
16	OB6	Odd data bit B6
17	EB7	Even data bit B7 (MSB)
18	OB7	Odd data bit B7 (MSB)
19	GND	Ground
20	GND	Ground
21	Vcc	DC +5v, reserved & not normally used
22	Vcc	DC +5v, reserved & not normally used
23	VS	Vertical sync
24	/PwrDn	Power down control signal (5V TTL)
25	HS	Horizontal sync
26	DE	Display enable
27	VLCD	Panel supply (switched)
28	VLCD	Panel supply (switched)
29	CLE	Even dot clock (shift clock)
30	CLO	Odd dot clock (shift clock)
31	GND	Ground
32	GND	Ground

CN4 - Hirose DF11-20DF-2DSA

PIN	SYMBOL	DESCRIPTION
1	GND	Ground
2	GND	Ground
3	NC	No connection
4	NC	No connection
5	ER0	Even data bit R0 (LSB)
6	OR0	Odd data bit R0 (LSB)
7	ER1	Even data bit R1
8	OR1	Odd data bit R1
9	EG0	Even data bit G0 (LSB)
10	OG0	Odd data bit G0 (LSB)
11	EG1	Even data bit G1
12	OG1	Odd data bit G1
13	EB0	Even data bit B0 (LSB)
14	OB0	Odd data bit B0 (LSB)
15	EB1	Even data bit B1
16	OB1	Odd data bit B1
17	NC	No connection
18	NC	No connection
19	GND	Ground
20	GND	Ground