极景微半导体

10-Output Low-Jitter Low-Power Clock Buffer/Level Translator

US5S310
Datasheet

Description

The US5S310 is a highly versatile, low-jitter, low-power clock fanout buffer which can distribute to ten low-jitter LVCMOS clock outputs from one of three inputs, whose primary and secondary inputs can feature differential or single-ended signals and crystal input. Such a buffer is good for use in a variety of mobile and wired infrastructure, data communication,computing, low-power medical imaging, and portable test and measurement applications. When the input is an illegal level, the output is at a defined state. One can set the core to 2.5 V or 3.3 V, and output to 1.5V, 1.8 V, 2.5 V or 3.3 V. Pin programming easily configures the CDCLVC1310. The overall additive jitter performance is 25 fs_{RMS} (typical). The US5S310 comes in a small 32-pin 5X5 QFN package.

Applications

- Wireless and Wired Infrastructure
- Networking and Data Communications
- Medical Imaging
- Portable Test and Measurement
- High-End A/V

Features

- High-Performance Crystal Buffer With Ultralow Noise Floor of –169 dBc/Hz
- Additive RMS phase jitter @ 156.25MHz：
  - 48fs RMS (10kHz - 20MHz), typical @ 3.3V/ 3.3V
- Level Translation With 3.3-V or 2.5-V Core and 3.3-V, 2.5-V, 1.8-V, or 1.5-V Output Supply
- Device inputs consist of primary, secondary,and crystal inputs, and manually selectable (through pins) using the input MUX. The primary and secondary inputs can accept LVPECL, LVDS, HCSL, SSTL or LVCMOS signals and crystal input.
  - Crystal Input accepts 10MHz to 96MHz Crystal or Single Ended Clock
  - Differential and Single-Ended Input Frequencies Supported Are up to 200 MHz
- 10 Single-Ended LVCMOS Outputs. The outputs can operate at 1.5-V, 1.8-V, 2.5-V or 3.3-V Power-Supply Voltage.
  - LVCMOS Outputs Operate up to 250 MHz
  - Output Skew Is 30 ps (Typical)
  - Total Propagation Delay Is less than 1 ns (Typical)
  - Synchronous and Glitch-Free Output Enable Is Available
- Supply voltage modes:

  V_{DD}/V_{DDO}

  3.3V/3.3V,2.5V,1.8V,1.5V

  2.5V/2.5V,1.8V,1.5V
- Industrial Temperature Range:-40°C to 85°C
- Pin-to-Pin compatible to the CDCLVC1310，LMK00101, 8L30110
- Available in a 32-pin,5mm*5mm WQFN package

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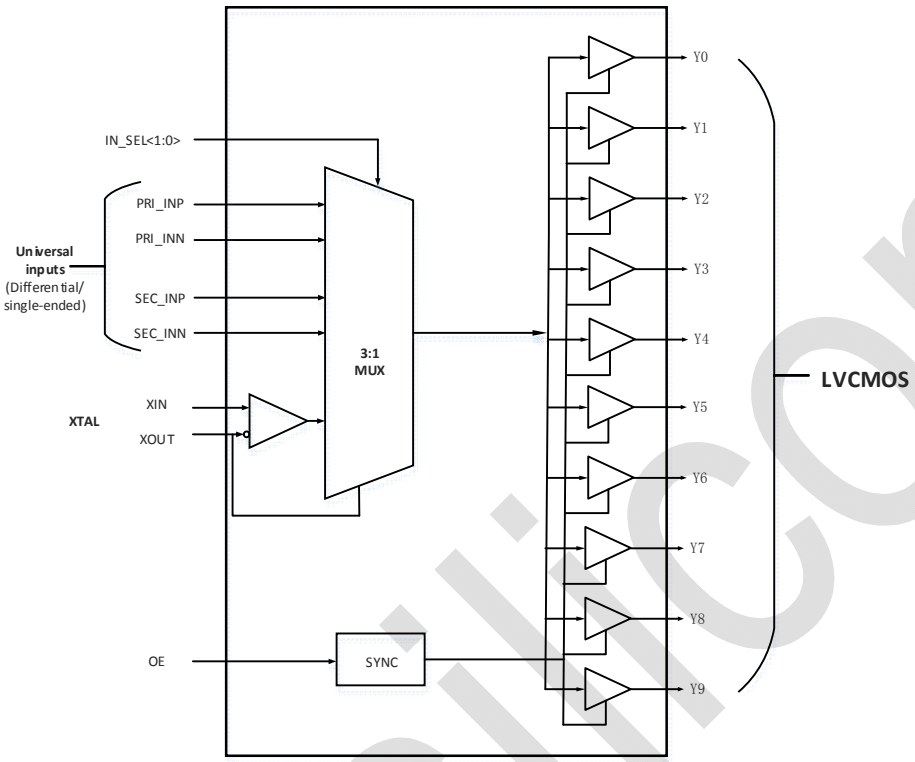
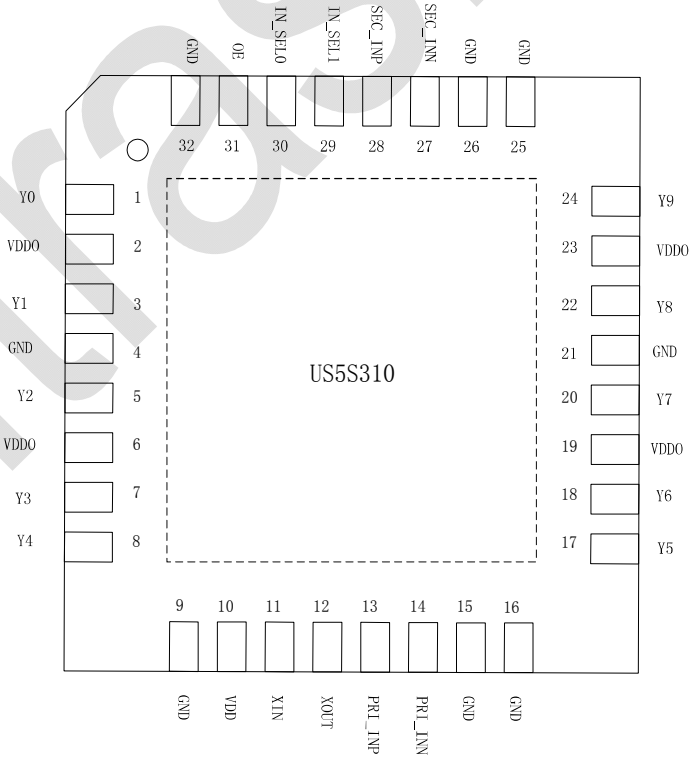
Block Diagram



Pin Assignment for 5mm x 5mm 32-Lead WQFN Package



Pin Description and Pin Characteristic Tables

Table 1: Pin Descriptions

Number	Name	Type		Description
1	Y0	Output		LVCMOS output 0
2	VDDO	Power		I/O power-supply pins
3	Y1	Output		LVCMOS output 1
4	GND	Power		Ground.
5	Y2	Output		LVCMOS output 2
6	VDDO	Power		I/O power-supply pins
7	Y3	Output		LVCMOS output 3
8	Y4	Output		LVCMOS output 4
9	GND	Power		Ground.
10	VDD	Power		Power-supply pins
11	XTAL_I	Input		Crystal oscillator interface.
12	XTAL_O	Input		Crystal oscillator interface.
13	PRI_INP	Input		Non-inverting differential or single-ended primary reference input
14	PRI_INN	Input		Inverting differential primary reference input, internally biased to Vdd / 2
15	GND	Power		Ground.
16	GND	Power		Ground.
17	Y5	Output		LVCMOS output 5
18	Y6	Output		LVCMOS output 6
19	VDDO	Power		I/O power-supply pins
20	Y7	Output		LVCMOS output 7
21	GND	Power		Ground.
22	Y8	Output		LVCMOS output 8
23	VDDO	Power		I/O power-supply pins
24	Y9	Output		LVCMOS output 9
25	GND	Power		Ground..
26	GND	Power		Ground.
27	SEC_INN	Input		Inverting differential secondary reference input, internally biased to Vdd / 2
28	SEC_INP	Input		Non-inverting differential or single-ended secondary reference input
29	IN_SEL1	Input		Input-clock selection 1
30	IN_SEL0	Input		Input-clock selection 0
31	OE	Output		LVCMOS output enable
32	GND	Power		Ground.

Function table

Input Selection

IN_sel1	IN_sel0	Input Chosen
0	0	PRI_IN
0	1	SEC_IN
1	0	XTAL or overdrive
1	1	XTAL Bypass

Input/Output Operation

Input State	Output State
PRI_INx, SEC_INx open	Logic Low
PRI_INP, SEC_INP = HIGH, PRI_INN, SEC_INN = LOW	Logic High
PRI_INP, SEC_INP = LOW, PRI_INN, SEC_INN = HIGH	Logic Low

OE Function

OE	Yx
0	High-impedance
1	Enabled

Absolute Maximum Ratings

Exposure to absolute maximum rating conditions for extended periods may affect product reliability. Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of the product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied.

Item	Rating
V_{DD}, V_{DDO} : Supply voltage	-0.5V to 4.6V
V_{IN} : Input voltage	-0.5V to VDD +0.5V
V_{OUT} : Output voltage	-0.5V to VDD +0.5V
I_{IN} : Input current	-20mA to 20mA
I_O : Continuous output current	-50mA to 50mA
T_{STG} :Storage Temperature	-65°C to 150°C

ESD Ratings

		Max	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017	±2500	V
	Machine model (MM), JEDEC Std. JESD22-A115-C	±250	
	Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002-2018	±750	

Latch up

		Max	Unit
Latch up	I-test, JEDEC STD JESD78E	±200	mA
	V-test, JEDEC STD JESD78E	4.6	V

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Ambient air temperature	-40		85	□C
T_J	Junction temperature			125	□C
V_{DD}	Power supply for Core and input Buffer blocks	3.3-5% 2.5-5%	3.3 2.5	3.3+5% 2.5+5%	V
V_{DDO}	Power supply for Bank QA or QB or REFOUT	3.3-5% 2.5-5% 1.8-5% 1.5-5%	3.3 2.5 1.8 1.5	3.3+5% 2.5+5% 1.8+5% 1.5+5%	V
I_{OH}	High-level output current, LVCMOS			-24	mA
I_{OL}	Low-level output current, LVCMOS			24	mA

INPUT CHARACTERISTICS

over recommended ranges of supply voltage (VDDO ≤ VDD), load (50 Ω to VDDO/2), and ambient temperature (unless otherwise noted)

Parameter		Test Conditions		Min	Typ	Max	Unit
DC Characteristic (OE, IN_SEL0, IN_SEL1, PRI_IN, SEC_IN)							
f_{CLKin}	Input Frequency Range			DC		250	MHz
V_{IHD}	Differential Input High Voltage	CLKin driven differentially				VDD	V
V_{ILD}	Differential Input Low Voltage			GND			V
V_{ID}	Differential Input Voltage Swing (5)			0.15		1.3	V
V_{CMD}	Differential Input Common Mode Voltage			0.5		VDD - 0.85	V
V_{IH}	Single-Ended Input High Voltage	CLK_X driven single-ended (AC or DC coupled), nCLK_X AC coupled to GND or externally biased within V_{CM} range				VDD	V
V_{IL}	Single-Ended Input Low Voltage			GND			V
V_{I_SE}	Single-Ended Input Voltage Swing			0.3		2	Vpp
V_{CM}	Single-Ended Input Common Mode Voltage			0.25		VDD - 1.2	V
ISO_{MUX}	Mux Isolation, CLK0 to CLK1	f_{OFFSET} > 50 kHz, P_{CLK_X} = 0 dBm	f_{CLK0} = 100 MHz		-112.5		dBc
			f_{CLK0} = 200 MHz		-82		
Crystal Interface (XTAL_I, XTAL_O)							
F_{CLK}	External Clock Frequency Range(4)	XTAL_I driven single-ended, XTAL_O floating				250	MHz
F_{XTAL}	Crystal Frequency Range	Fundamental mode crystal		10		48	MHz
C_{IN}	On-chip load Capacitance				4		pF

LVCMOS OUTPUT CHARACTERISTICS

over recommended ranges of supply voltage (VDDO ≤ VDD), load (50 Ω to VDDO/2), and ambient temperature (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
f_{OUT}			DC		250	MHz
V_{OH}	Output high voltage	VDDO = 3.135 V to 3.465 V	0.8*VDDO			V
		VDDO = 2.375 V to 2.625 V	0.8*VDDO			
		VDDO = 1.6 V to 2 V	0.7*VDDO			
		VDDO = 1.35 V to 1.65 V	0.7*VDDO			
V_{OL}	Output low voltage	VDDO = 3.135 V to 3.465 V			0.2*VDDO	V
		VDDO = 2.375 V to 2.625 V			0.2*VDDO	
		VDDO = 1.6 V to 2 V			0.3*VDDO	
		VDDO = 1.35 V to 1.65 V			0.3*VDDO	
R_{OUT}	Output high voltage	VDDO = 1.5V to 3.5 V		50		Ω

LVCMOS OUTPUT CHARACTERISTICS(continued)

over recommended ranges of supply voltage (VDDO ≤ VDD), load (50 Ω to VDDO/2), and ambient temperature (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$t_{SLEW-RATE}$	Output slew rate, rising and falling	VDDO=3.3V +/- 5%, 20% to 80%	0.8*VDDO			V
		VDDO=2.5V +/- 5%, 20% to 80%	0.8*VDDO			
		VDDO=1.8V +/- 200mV, 20% to 80%	0.7*VDDO			
		VDDO=1.5V +/- 150mV, 20% to 80%	0.7*VDDO			
		VDDO = 2.375 V to 2.625 V			0.2*VDDO	
		VDDO = 1.6 V to 2 V			0.3*VDDO	
		VDDO = 1.35 V to 1.65 V			0.3*VDDO	
t_{SK}	Output skew	VDDO = 1.5V to 3.5 V		30	50	ps
$t_{SK,PP}$	Part-to-part skew				2	ns
t_{DELAY}	Propagation delay	VDD = 3.3 V ±5%,VDDO = 1.35 V to VDD, C_L ≤ 5 pF	900	1400	2000	ps
		VDD = 2.5 V ±5%,VDDO = 1.35 V to VDD, C_L ≤ 5 pF	1000	1500	2300	ps
$Jitter_{ADD}$	Additive RMS Jitter Integration bandwidth 12kHz to 20 MHz 156.25MHz	Differential input, VDD = 3.3 V,VDDO = 3.3 V		48		fs,RMS
		Differential input, VDD = 2.5 V or 3.3 V,VDDO=2.5V		52		
		Differential input, VDD = 2.5 V or 3.3 V,VDDO=1.8V		77		
NF	Noise floor, Single-ended input, f = 156.25 MHz, VDD = VDDO = 3.3 V	10kHz offset		-145		dBc/Hz
		100kHz offset		-156		
		1MHz offset		-163		
		10MHz offset		-164		
		20MHz offset		-164		
	Noise floor, Differential input, f = 156.25 MHz, VDD = VDDO = 3.3 V	10kHz offset		-145		
		100kHz offset		-155		
		1MHz offset		-160		
		10MHz offset		-161		
		20MHz offset		-162		
odc	Output duty cycle	$f_{IN/OUT}$ = 125 MHz, idc = 50%	45%		55%	
t_{EN}	Output enable or disable time				2	Cycle
MUXISOLATION	MUX isolation	125MHz	55			dB

PHASE NOISE WITH XTAL (1) SELECTED

VDD = VDDO = 2.5 V or 3.3 V, f_{XTAL} = 48 MHz, T_A = 25°C (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
$Jitter_{RMS}$	RMS phase jitter	Integration bandwidth 12kHz to 5 MHz，VDD = 3.3 V,VDDO = 3.3 V		42		fs,RMS
		Integration bandwidth 12kHz to 5 MHz，VDD = 2.5 V,VDDO = 2.5 V		50		
NF	Noise floor,	100Hz offset，VDD = VDDO = 3.3 V		-77		dBc/Hz
		1kHz offset，VDD = VDDO = 3.3 V		-107		
		10kHz offset，VDD = VDDO = 3.3 V		-139		
		100kHz offset，VDD = VDDO = 3.3 V		-163		
		1MHz offset，VDD = VDDO = 3.3 V		-170		
		10MHz offset，VDD = VDDO = 3.3 V		-170		
	Noise floor,	100Hz offset，VDD = VDDO = 2.5 V		-77		
		1kHz offset，VDD = VDDO = 2.5 V		-107		
		10kHz offset，VDD = VDDO = 2.5 V		-138		
		100kHz offset，VDD = VDDO = 2.5 V		-156		
		1MHz offset，VDD = VDDO = 2.5 V		-166		
		10MHz offset，VDD = VDDO = 2.5 V		-167		
odc	Output duty cycle	$f_{IN/OUT}$ = 125 MHz, idc = 50%	45%		55%	
t_{EN}	Output enable or disable time				2	Cycle
$MUX_{ISOLATION}$	MUX isolation	156.25MHz	55			dB

(1)Crystal specification: CL = 8pF; ESR = 60 Ω (max); C0 = 3 pF; drive level = 100 µW (max)

DEVICE CURRENT CONSUMPTION

over recommended ranges of supply voltage, load and ambient temperature (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
I_{DD}	Static device current	OE = 0 V or V_{DD} ; Ref. input (PRI/SEC) = 0 V or V_{DD} ; I_O = 0 mA; VDD / VDDO = 3.3 V		9		mA
		OE = 0 V or V_{DD} ; Ref. input (PRI/SEC) = 0 V or V_{DD} ; I_O = 0 mA; VDD / VDDO = 2.5 V		7		
$I_{DD,XTAL}$	Device current with XTAL input			20		mA
C_{PD}	Power dissipation capacitance per output,	VDDO = 3.465 V; f = 100 MHz		8.8		pF
		VDDO = 2.625 V; f = 100 MHz		7.7		
		VDDO = 2 V; f = 100 MHz		7.3		
		VDDO = 1.65 V; f = 100 MHz		6.9		

(1)I_{DD} and $I_{DD,XTAL}$ is the current through V DD ; outputs enabled or in the high-impedance state; no load;

(2) This is the formula for the power dissipation calculation

$I_{DD,Total} = I_{DD} + I_{DD,Cload} + I_{DD,dyn}$ [mA]

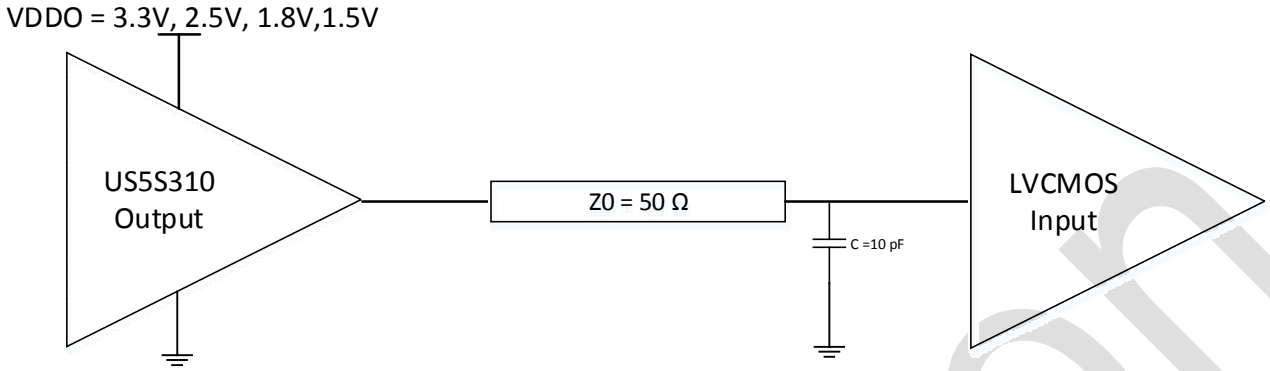
$I_{DD,dyn} = C_{PD} \times V_{DDO} \times f \times n$ [mA]

$I_{DD,Cload}$ = Cload × V_{DDO} × f × n [mA]

n = Number of switching output pins

APPLICATION INFORMATION

Typical Application Load



LVCMOS Output DC Configuration: Typical Application Load

Crystal Oscillator Input

The US5S310 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error. In addition, the recommended 12pF parallel resonant crystal tuning is shown in *Figure 2.*The optimum C1 and C2 values can be slightly adjusted for different board layouts.

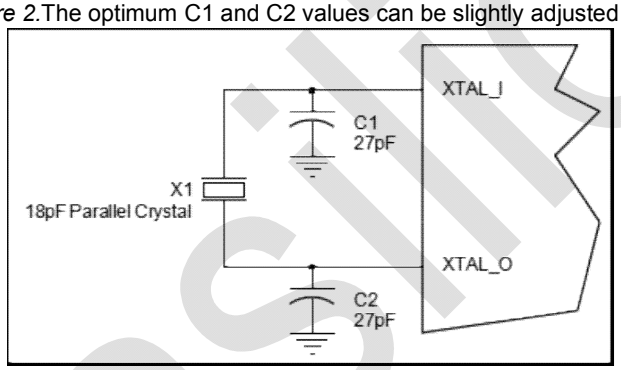
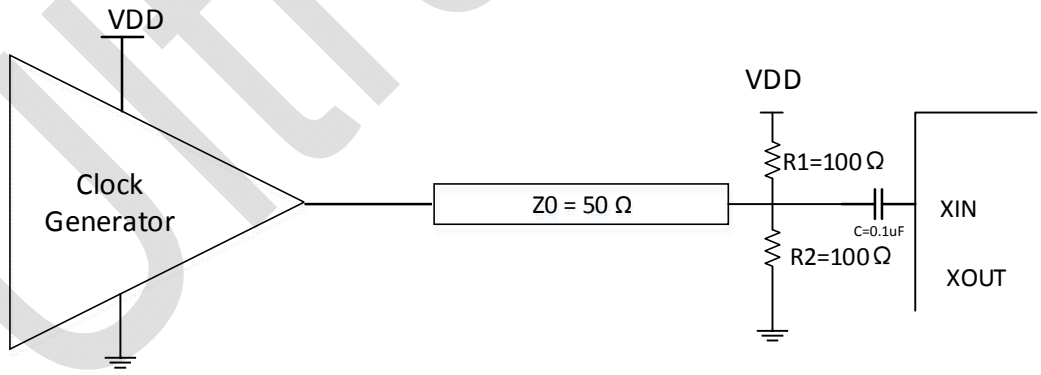


Figure 1: Crystal Input Interface

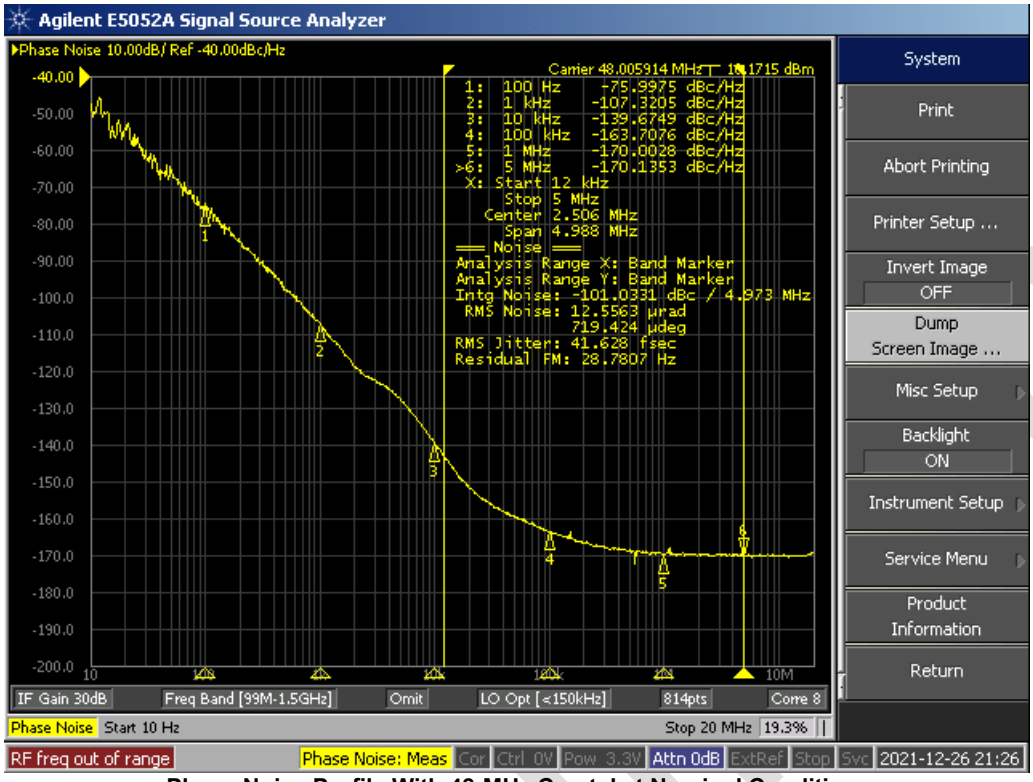
The input XIN can accept single-ended LVCMOS signals in two configurations. It is possible to overdrive the oscillator stage or to use a pure LVCMOS input (see Table 1). If overdriving the oscillator stage, it is necessary to ac-couple the input with a capacitor (see Figure 13). Otherwise, if selecting the bypass, there is no requirement for a coupling capacitor.



Single-Ended Crystal Input

Phase-Noise Performance

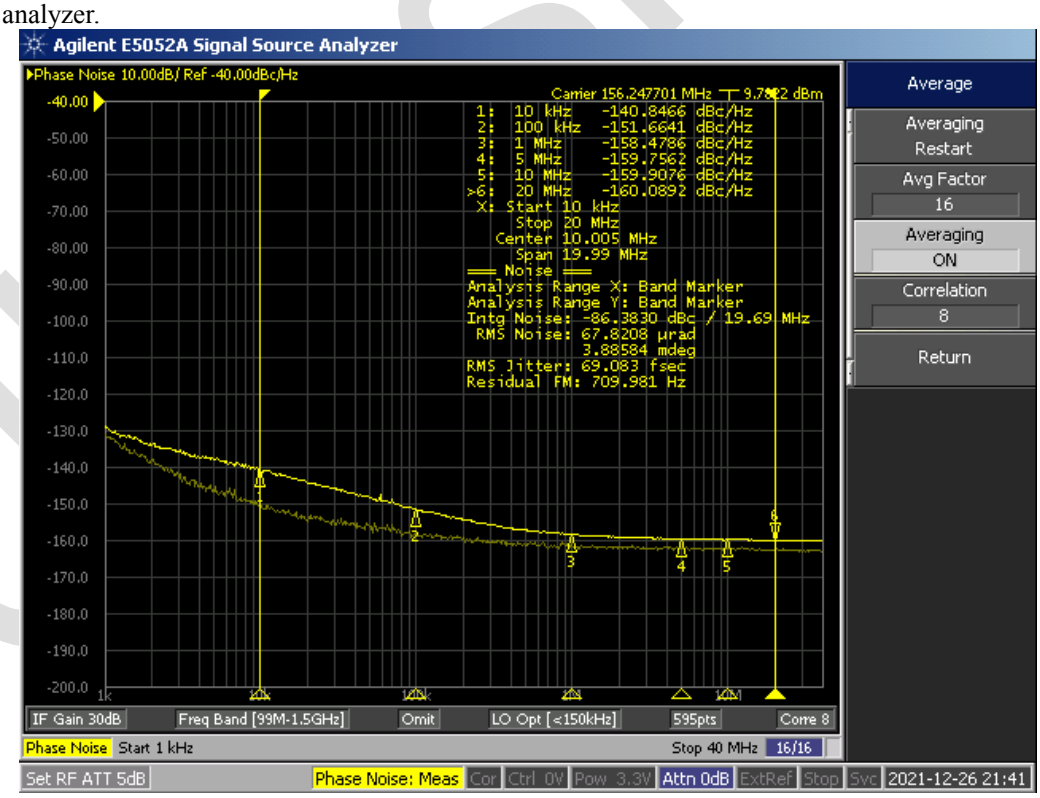
The US5S310 provides ultralow phase-noise outputs (noise floor = –170 dBc/Hz) if it has an attached crystal. Figure 14 shows the phase-noise plot of the US5S310 with a 48-MHz crystal at V_{DD} = V_{DDO} = 3.3 V and room temperature.



Phase-Noise Profile With 48-MHz Crystal at Nominal Conditions

Additive Phase Jitter

The additive phase jitter for this device was measured using an EPSON Clock Driver SG3225VEN as an input source and Agilent E5052A phase noise analyzer.



Offset from Carrier Frequency (Hz)

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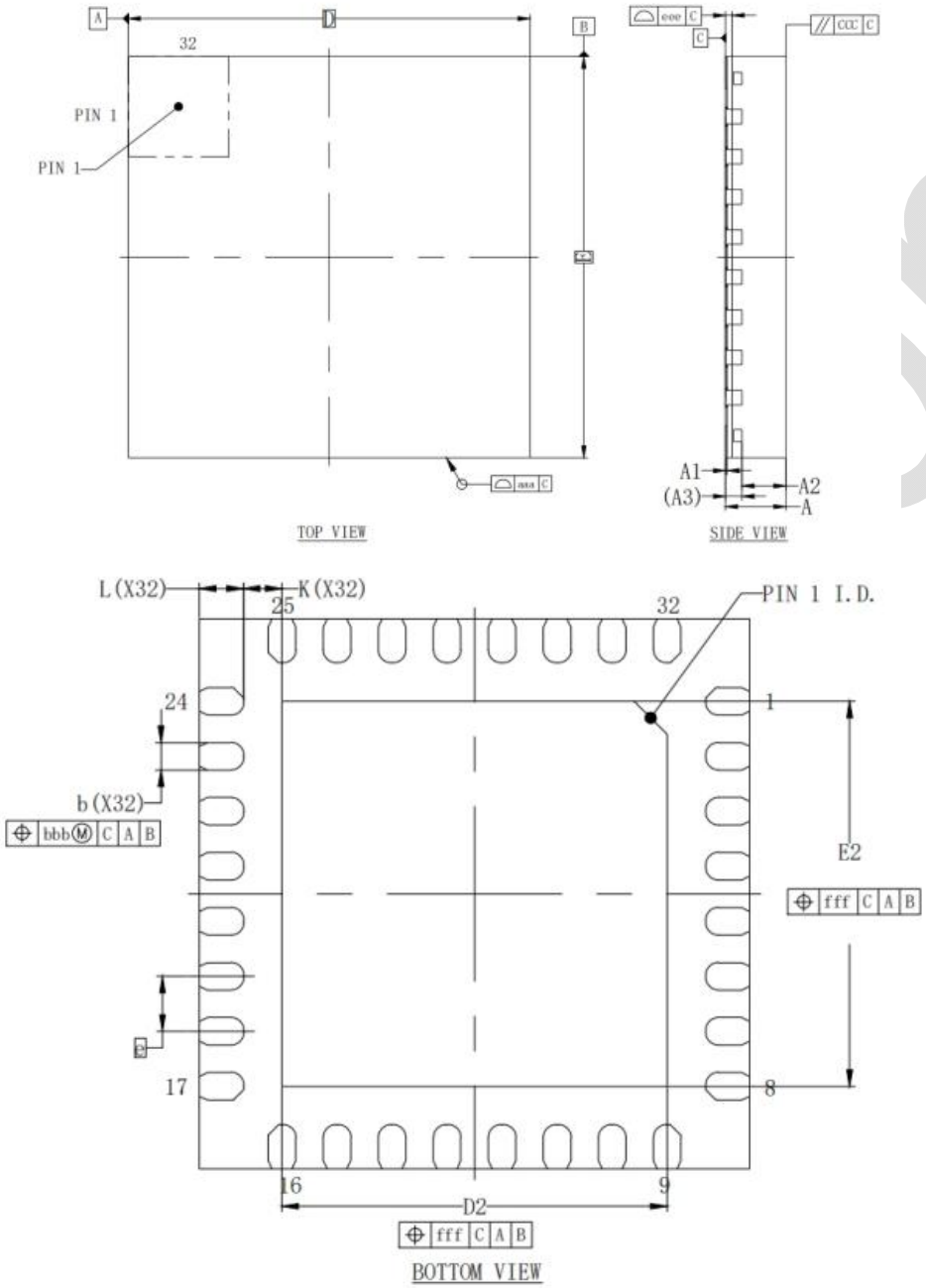
PACKAGE DIMENSIONS

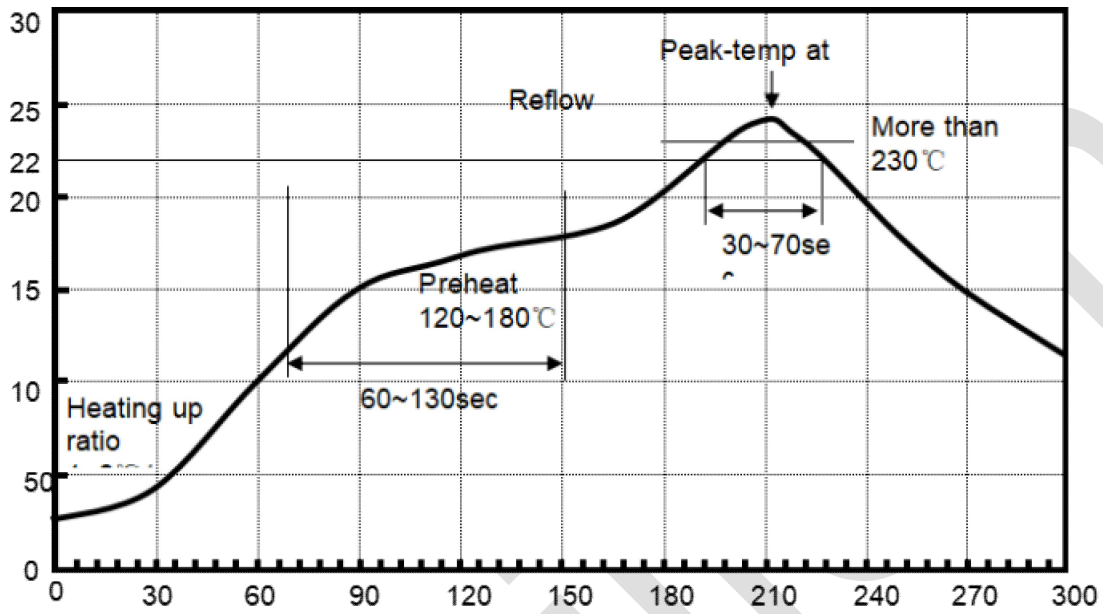


Item		Symbol	Minimum	Normal	Maximum
Body Size	X	D		5.0 BSC	
	Y	E		5.0 BSC	
Exposed Pad Size	X	D2	3.40	3.50	3.60
	Y	E2	3.40	3.50	3.60
Total Thickness		A	0.70	0.75	0.80
Stand Off		A1	0	0.02	0.05
Molding Thickness		A2		0.55	
LF Thickness		A3		0.203 REF	
Lead Width		b	0.20	0.25	0.30
Lead Length		L	0.30	0.40	0.50
Lead Pitch		e		0.50 BSC	
Lead tip to Exposed Pad		K		0.35 REF	
Package Edge Tolerance		aaa		0.10	
Lead Offset		bbb		0.10	
Molding Flatness		ccc		0.10	
Coplanarity		eee		0.08	
Exposed Pad Offset		fff		0.10	

Note：

1. Dimensioning and tolerancing conform to ASME Y14.5-2009.
2. All dimensions are in millimeters.
3. N is the total number of terminals.
4. The location of the marked terminal #1 identifier is within the hatched area.
5. ND and NE refer to the number of terminals on D and E side respectively.
6. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
7. Colanarity applies to the terminals and all other bottom surface metallization.

Reflow profile



Recommended Temperature Sn95.5Ag4.0Cu0.5