CAT6095

Digital Output Temperature Sensor

ON Semiconductor®

http://onsemi.com

TDFN−8
VP2 SUFFIX
CASE 511AK

Description

The CAT6095 is a JEDEC JC42.4 compliant Temperature Sensor designed for general purpose temperature measurements requiring a digital output.

The CAT6095 measures temperature at least 10 times every second. Temperature readings can be retrieved by the host via the serial interface, and are compared to high, low and critical trigger limits stored into internal registers. Over or under limit conditions can be signaled on the open−drain $\overline{\text{EVENT}}$ pin.

The CAT6095 is packaged in space saving TDFN package with exposed backside die attach pads (DAP). The exposed DAP reduces overall thermal resistance, thus providing faster response to thermal changes when compared to SOIC, TSSOP or SOT packages.

Features

- JEDEC JC42.4 Compliant Temperature Sensor
- Temperature Range: −40°C to +125°C
- Supply Range: 3.3 V ± 10%
- I^2C / SMBus Interface
- Schmitt Triggers and Noise Suppression Filters on SCL and SDA Inputs
- Low Power CMOS Technology
- 2 x 3 x 0.75 mm TDFN Package
- These Devices are Pb−Free and are RoHS Compliant

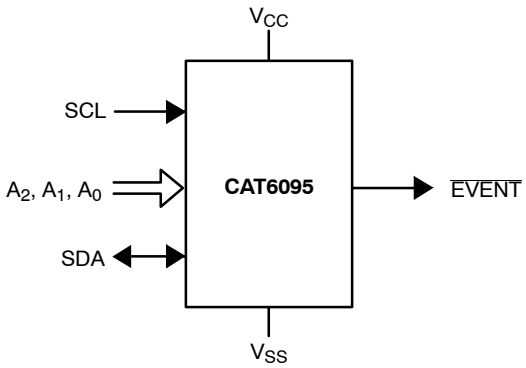
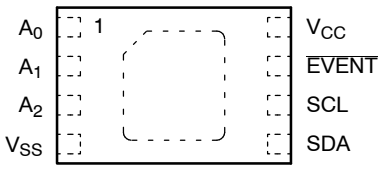


Figure 1. Functional Symbol

PIN CONFIGURATION



(Top View)

For the location of Pin 1, please consult the corresponding package drawing.

MARKING DIAGRAM

HMC	= Specific Device Code
A	= Assembly Location Code
LL	= Assembly Lot Number (Last Two Digits)
Y	= Production Year (Last Digit)
M	= Production Month (1 − 9, O, N, D)
▪	= Pb−Free Package

PIN FUNCTIONS

Pin Name	Function
A_0, A_1, A_2	Device Address Input
SDA	Serial Data Input/Output
SCL	Serial Clock Input
$\overline{\text{EVENT}}$	Open−drain Event Output
V_{CC}	Power Supply
V_{SS}	Ground
DAP	Backside Exposed DAP at V_{SS}

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 15 of this data sheet.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Operating Temperature	−45 to +130	°C
Storage Temperature	−65 to +150	°C
Voltage on any pin with respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. The A_0 pin can be raised to a HV level compatible with the use of a DDR3 SPD device sharing the bus with the TS. SCL and SDA inputs can be raised to the maximum limit, irrespective of V_{CC}.

Table 2. TEMPERATURE CHARACTERISTICS (V_{CC} = 3.3 V ± 10%, T_A = −40°C to +125°C, unless otherwise specified)

Parameter	Test Conditions/Comments	Max	Unit
Temperature Reading Error Class B, JC42.4 compliant	+75°C ≤ T_A ≤ +95°C, active range	±1.0	°C
	+40°C ≤ T_A ≤ +125°C, monitor range	±2.0	°C
	−20°C ≤ T_A ≤ +125°C, sensing range	±3.0	°C
ADC Resolution		12	Bits
Temperature Resolution		0.0625	°C
Temperature Conversion Time		100	ms
Thermal Resistance (Note 2) θ_{JA}	Junction−to−Ambient (Still Air)	92	°C/W

2. Power Dissipation is defined as $P_J = (T_J - T_A)/\theta_{JA}$, where T_J is the junction temperature and T_A is the ambient temperature. The thermal resistance value refers to the case of a package being used on a standard 2−layer PCB.

Table 3. D.C. OPERATING CHARACTERISTICS (V_{CC} = 3.3 V ± 10%, T_A = −40°C to +125°C, unless otherwise specified)

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
I_{CC}	Supply Current	TS active		200	μA
I_{SHDN}		TS shut−down; no bus activity		10	μA
I_L	I/O Pin Leakage Current	Pin at GND or V_{CC}		2	μA
V_{IL}	Input Low Voltage		−0.5	0.3 x V_{CC}	V
V_{IH}	Input High Voltage		0.7 x V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA, V_{CC} > 2.5 V		0.4	V

Table 4. A.C. CHARACTERISTICS (V_{CC} = 3.3 V ± 10%, T_A = −40°C to +125°C) (Note 3)

Symbol	Parameter	Min	Max	Units
F_{SCL} (Note 4)	Clock Frequency	10	400	kHz
t_{HIGH}	High Period of SCL Clock	600		ns
t_{LOW}	Low Period of SCL Clock	1300		ns
$t_{TIMEOUT}$ (Note 4)	SMBus SCL Clock Low Timeout	25	35	ms
t_R (Note 5)	SDA and SCL Rise Time		300	ns
t_F (Note 5)	SDA and SCL Fall Time		300	ns
$t_{SU:DAT}$ (Note 6)	Data Setup Time	100		ns
$t_{HD:DAT}$ (Note 5)	Data Hold Time (for Input Data)	0		ns
	Data Hold Time (for Output Data)	300	900	ns
$t_{SU:STA}$	START Condition Setup Time	600		ns
$t_{HD:STA}$	START Condition Hold Time	600		ns
$t_{SU:STO}$	STOP Condition Setup Time	600		ns
t_{BUF}	Bus Free Time Between STOP and START	1300		ns
T_i	Noise Pulse Filtered at SCL and SDA Inputs		100	ns
t_{PU} (Note 7)	Power−up Delay to Valid Temperature Recording		100	ms

3. Timing reference points are set at 30%, respectively 70% of V_{CC}, as illustrated in Figure 11. Bus loading must be such as to allow meeting the V_{IL}, V_{OL} as well as the various timing limits.
4. The TS interface will reset itself and will release the SDA line if the SCL line stays low beyond the $t_{TIMEOUT}$ limit. The time−out count is started (and then re−started) on every negative transition of SCL in the time interval between START and STOP.
5. In a “Wired−OR” system (such as I^2C or SMBus), SDA rise time is determined by bus loading. Since each bus pull−down device must be able to sink the (external) bus pull−up current (in order to meet the V_{IL} and/or V_{OL} limits), it follows that SDA fall time is inherently faster than SDA rise time. SDA rise time can exceed the standard recommended t_R limit, as long as it does not exceed $t_{LOW} - t_{HD:DAT} - t_{SU:DAT}$, where t_{LOW} and $t_{HD:DAT}$ are actual values (rather than spec limits). A shorter $t_{HD:DAT}$ leaves more room for a longer SDA t_R, allowing for a more capacitive bus or a larger bus pull−up resistor. At the minimum t_{LOW} spec limit of 1300 ns, the maximum $t_{HD:DAT}$ of 900 ns demands a maximum SDA t_R of 300 ns. The CAT6095’s maximum $t_{HD:DAT}$ is <700 ns, thus allowing for an SDA t_R of up to 500 ns at minimum t_{LOW}.
6. The minimum $t_{SU:DAT}$ of 100 ns is a limit recommended by standards. The TS will accept a $t_{SU:DAT}$ of 0 ns.
7. The first valid temperature recording can be expected after t_{PU} at nominal supply voltage.

Table 5. PIN CAPACITANCE (T_A = 25°C, V_{CC} = 3.3 V, f = 1 MHz)

Symbol	Parameter	Test Conditions/Comments	Min	Max	Unit
C_{IN}	SDA, $\overline{EVENT}$ Pin Capacitance	V_{IN} = 0		8	pF
	Input Capacitance (other pins)	V_{IN} = 0		6	pF

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{CC} = 3.3 V, T_A = −25°C to +125°C, unless otherwise specified.)

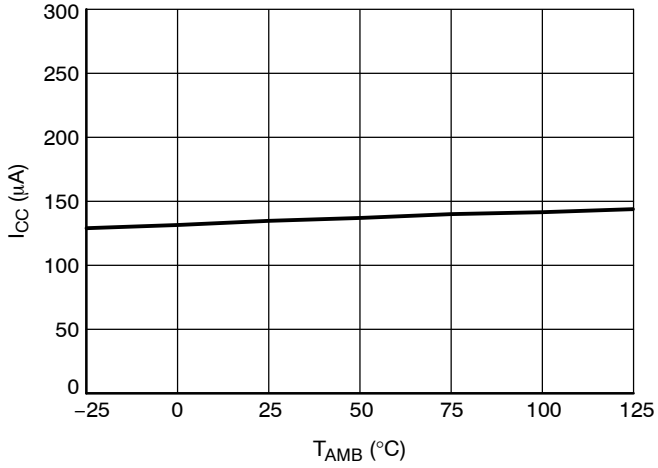


Figure 2. Active Current (I²C−bus Idle)

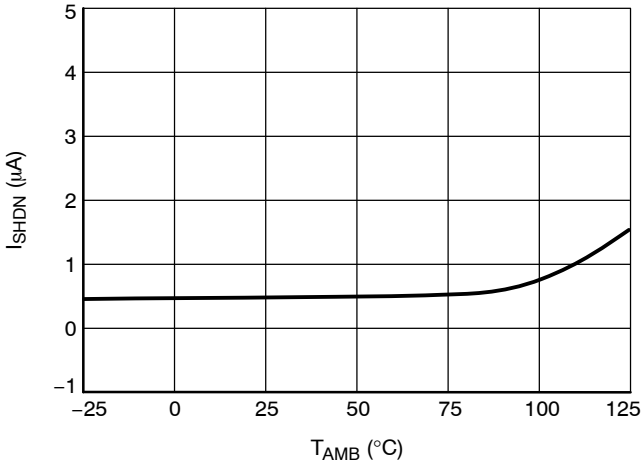


Figure 3. Standby Current (I²C−bus Idle, TS Shut−down)

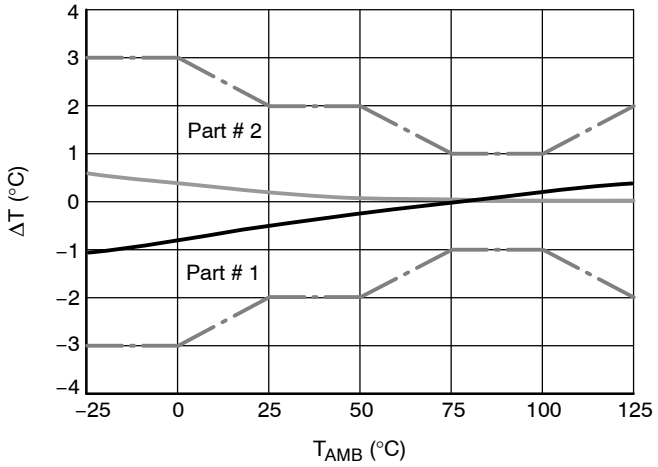


Figure 4. Temperature Read−Out Error

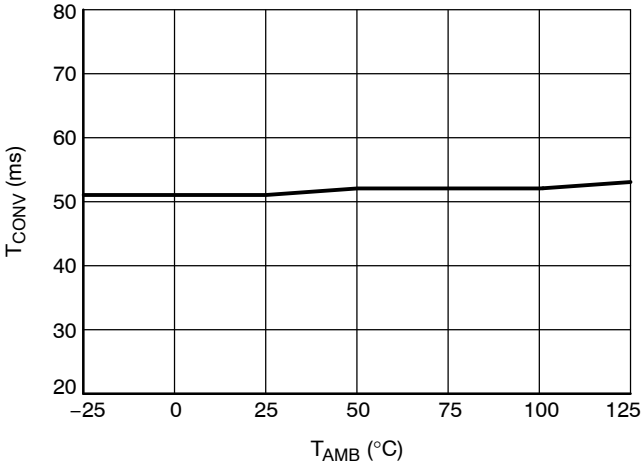


Figure 5. A/D Conversion Time

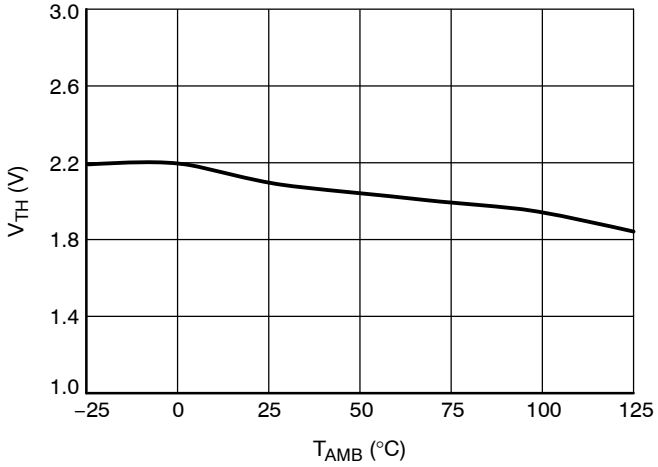


Figure 6. POR Threshold Voltage

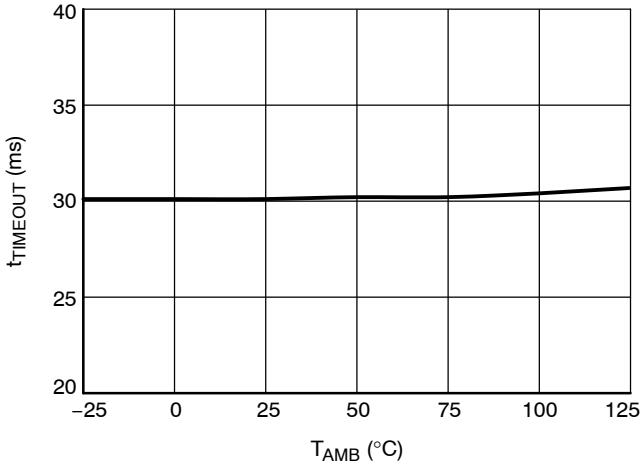


Figure 7. SMBus SCL Clock Low Timeout

Pin Description

SCL: The Serial Clock input pin accepts the Serial Clock generated by the Master (Host).

SDA: The Serial Data I/O pin receives input data and transmits data stored in the internal registers. In transmit mode, this pin is open drain. Data is acquired on the positive edge, and is delivered on the negative edge of SCL.

A0, A1 and A2: The Address pins set the device address. These pins have on−chip pull−down resistors.

$\overline{\text{EVENT}}$: The open−drain $\overline{\text{EVENT}}$ pin can be programmed to signal over/under temperature limit conditions.

Power−On Reset

The CAT6095 incorporates Power−On Reset (POR) circuitry which monitors the supply voltage, and then resets (initializes) the internal state machine below a POR trigger level of approximately 2.0 V, i.e. well below the minimum recommended V_{CC} value.

The temperature sensor (TS) powers-up into conversion mode. The internal state machine will operate properly above the POR trigger level, but valid temperature readings can be expected only after the first conversion cycle started and completed at nominal supply voltage.

Device Interface

The CAT6095 supports I^2C and SMBus data transmission protocols. These protocols describe serial communication between transmitters and receivers sharing a 2−wire data bus. Data flow is controlled by a Master device, which generates the serial clock and the START and STOP conditions. The CAT6095 acts as a Slave device. Master and Slave alternate as transmitter and receiver. Up to 8 CAT6095 devices may be present on the bus simultaneously, and can be individually addressed by matching the logic state of the address inputs A0, A1, and A2.

I^2C/SMBus Protocol

The I^2C/SMBus uses two ‘wires’, one for clock (SCL) and one for data (SDA). The two wires are connected to the V_{CC} supply via pull−up resistors. Master and Slave devices connect to the bus via their respective SCL and SDA pins. The transmitting device pulls down the SDA line to ‘transmit’ a ‘0’ and releases it to ‘transmit’ a ‘1’.

Data transfer may be initiated only when the bus is not busy (see A.C. Characteristics).

During data transfer, the SDA line must remain stable while the SCL line is HIGH. An SDA transition while SCL is HIGH will be interpreted as a START or STOP condition (Figure 8).

START

The START condition precedes all commands. It consists of a HIGH to LOW transition on SDA while SCL is HIGH. The START acts as a ‘wake−up’ call to all Slaves. Absent a START, a Slave will not respond to commands.

STOP

The STOP condition completes all commands. It consists of a LOW to HIGH transition on SDA while SCL is HIGH. The STOP tells the Slave that no more data will be written to or read from the Slave.

Device Addressing

The Master initiates data transfer by creating a START condition on the bus. The Master then broadcasts an 8−bit serial Slave address. The first 4 bits of the Slave address (the preamble) select the Temperature Sensor (TS preamble = 0011) as shown in Figure 9. The next 3 bits, A2, A1 and A0, select one of 8 possible TS Slave devices. The last bit, R/$\overline{\text{W}}$, specifies whether a Read (1) or Write (0) operation is being performed.

Acknowledge

A matching Slave address is acknowledged (ACK) by the Slave by pulling down the SDA line during the 9^{th} clock cycle (Figure 10). After that, the Slave will acknowledge all data bytes sent to the bus by the Master. When the Slave is the transmitter, the Master will in turn acknowledge data bytes in the 9^{th} clock cycle. The Slave will stop transmitting after the Master does not respond with acknowledge (NoACK) and then issues a STOP. Bus timing is illustrated in Figure 11.

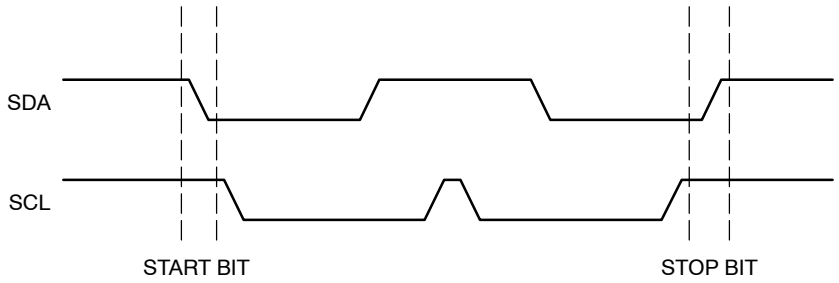


Figure 8. Start/Stop Timing

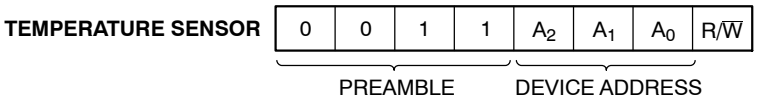


Figure 9. Slave Address Bits

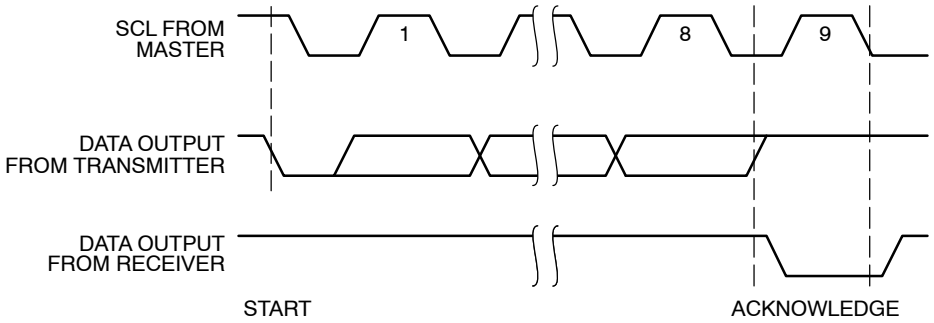


Figure 10. Acknowledge Timing

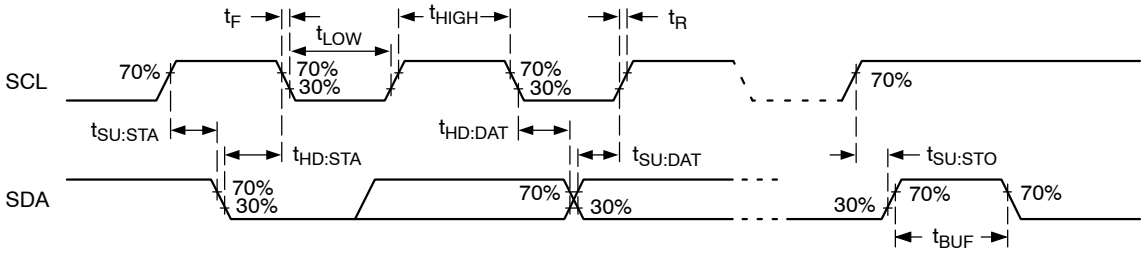


Figure 11. Bus Timing

Write Operations

Temperature Sensor Register Write

To write data to a TS register the Master creates a START condition on the bus, and then sends out the appropriate Slave address (with the R/$\overline{W}$ bit set to '0'), followed by an address byte and two data bytes. The matching Slave will acknowledge the Slave address, TS register address and the TS register data (Figure 12). The Master then ends the session by creating a STOP condition on the bus. The STOP completes the TS register update. Note that all registers in the TS are 'volatile' meaning any data contained in them is lost when power is removed from the chip.

Read Operations

Immediate Read

Upon power-up, the Temperature Sensor (TS) address counter is initialized to 00h. The TS address counter will thus point to the Capability Register. This address counter may be updated by subsequent operations.

A CAT6095 presented with a Slave address containing a '1' in the R/$\overline{W}$ position will acknowledge the Slave address and will then start transmitting data being pointed at by the current TS register address counter. The Master stops this transmission by responding with NoACK, followed by a STOP (Figure 13).

Selective Read

The Read operation can be started at an address different from the one stored in the address counter, by preceding the Immediate Read sequence with a 'data less' Write operation. The Master sends out a START, Slave address and address byte, but rather than following up with data (as in a Write operation), the Master then issues another START and continuous with an Immediate Read sequence (Figure 14).

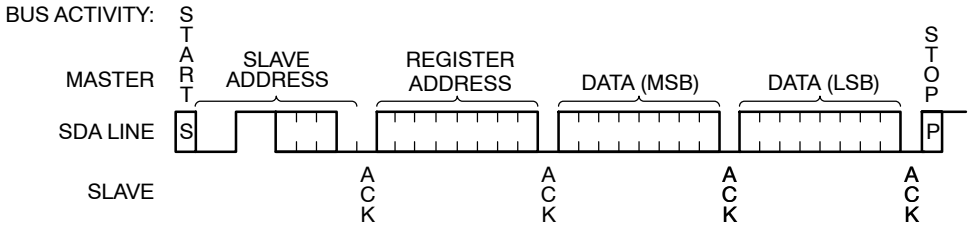


Figure 12. Temperature Sensor Register Write

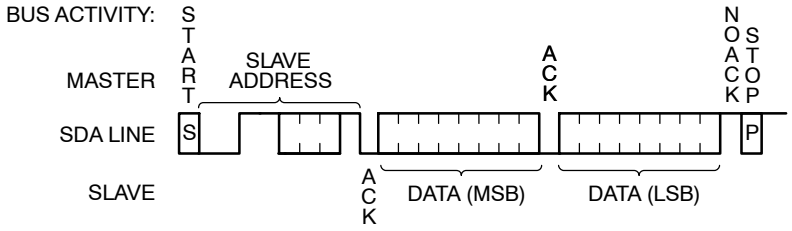


Figure 13. Immediate Read

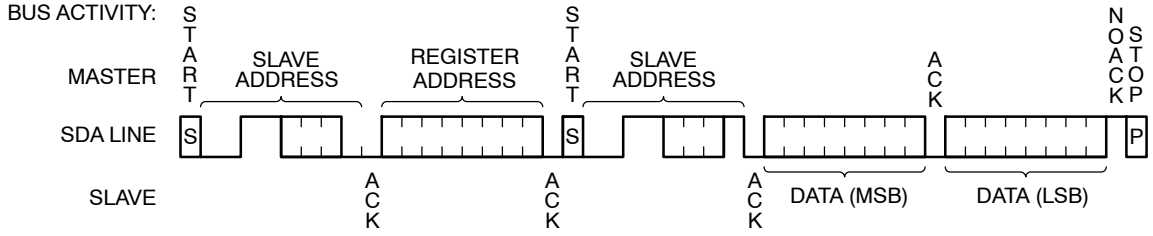


Figure 14. Selective Read

Temperature Sensor Operation

The CAT6095 temperature sensor (TS) combines a Proportional to Absolute Temperature (PTAT) sensor with a Σ−Δ modulator, yielding a 12 bit plus sign digital temperature representation.

The TS runs on an internal clock, and starts a new conversion cycle at least every 100 ms. The result of the most recent conversion is stored in the **Temperature Data Register (TDR)**, and remains there following a TS Shut−Down. Reading from the **TDR** does not interfere with the conversion cycle.

The value stored in the **TDR** is compared against limits stored in the **High Limit Register (HLR),** the **Low Limit Register (LLR)** and/or **Critical Temperature Register (CTR)**. If the measured value is outside the alarm limits or above the critical limit, then the $\overline{\text{EVENT}}$ pin may be asserted. The $\overline{\text{EVENT}}$ output function is programmable, via the **Configuration Register** for interrupt mode, comparator mode and polarity.

The temperature limit registers can be Read or Written by the host, via the serial interface. At power−on, all the (writable) internal registers default to 0x0000, and should therefore be initialized by the host to the desired values. The $\overline{\text{EVENT}}$ output starts out disabled (corresponding to polarity active low); thus preventing irrelevant event bus activity before the limit registers are initialized. While the TS is enabled (not shut−down), event conditions are normally generated by a change in measured temperature as recorded in the TDR, but limit changes can also trigger events as soon as the new limit creates an event condition, i.e. asynchronously with the temperature sampling activity.

In order to minimize the thermal resistance between sensor and PCB, it is recommended that the exposed backside die attach pad (DAP) be soldered to the PCB ground plane.

Registers

The CAT6095 contains eight 16−bit wide registers allocated to TS functions, as shown in Table 6. Upon power−up, the internal address counter points to the capability register.

Capability Register (User Read Only)

This register lists the capabilities of the TS, as detailed in the corresponding bit map.

Configuration Register (Read/Write)

This register controls the various operating modes of the TS, as detailed in the corresponding bit map.

Temperature Trip Point Registers (Read/Write)

The CAT6095 features 3 temperature limit registers, the **HLR**, **LLR** and **CLR** mentioned earlier. The temperature value recorded in the **TDR** is compared to the various limit values, and the result is used to activate the $\overline{\text{EVENT}}$ pin. To avoid undesirable $\overline{\text{EVENT}}$ pin activity, this pin is automatically disabled at power−up to allow the host to initialize the limit registers and the converter to complete the first conversion cycle under nominal supply conditions. Data format is two's complement with the LSB representing 0.25°C, as detailed in the corresponding bit maps.

Temperature Data Register (User Read Only)

This register stores the measured temperature, as well as trip status information. B15, B14 and B13 are the trip status bits, representing the relationship between measured temperature and the 3 limit values; these bits are not affected by EVENT status or by Configuration register settings. Measured temperature is represented by bits B12 to B0. Data format is two's complement, where B12 represents the sign, B11 represents 128°C, etc. and B0 represents 0.0625°C.

Manufacturer ID Register (Read Only)

The manufacturer ID assigned by the PCI−SIG trade organization to the CAT6095 device is 0x1B09.

Device ID and Revision Register (Read Only)

This register contains manufacturer specific device ID and device revision information.

Table 6. TEMPERATURE SENSOR REGISTERS

Register Address	Register Name	Power−On Default	Read/Write
0x00	Capability Register	0x007F	Read
0x01	Configuration Register	0x0000	Read/Write
0x02	High Limit Register	0x0000	Read/Write
0x03	Low Limit Register	0x0000	Read/Write
0x04	Critical Limit Register	0x0000	Read/Write
0x05	Temperature Data Register	Undefined	Read
0x06	Manufacturer ID Register	0x1B09	Read
0x07	Device ID/Revision Register	0x0813	Read
0x08 −	Reserved	−	−

Table 7. CAPABILITY REGISTER

B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
EVSD	TMOUT	RFU	TRES [1:0]		RANGE	ACC	EVENT

Bit	Description
B15:B8	Reserved for future use; can not be written; should be ignored; will typically read as 0
B7 (Note 8)	0: Configuration register bit 4 is frozen upon setting Configuration register bit 8 (i.e. a TS shut−down freezes the $\overline{\text{EVENT}}$ output) 1: Configuration register bit 4 is cleared upon setting Configuration register bit 8 (i.e. a TS shut−down de−asserts the $\overline{\text{EVENT}}$ output)
B6	0: The TS implements SMBus time−out within the range 10 to 60 ms 1: The TS implements SMBus time−out within the range 25 to 35 ms
B5	0: Pin A_0 V_{HV} compliance required for RSWP/SPD compatibility not explicitly stated 1: Pin A_0 V_{HV} compliance required for RSWP/SPD compatibility explicitly stated
B4:B3	00: LSB = 0.50°C (9 bit resolution) 01: LSB = 0.25°C (10 bit) 10: LSB = 0.125°C (11 bit) 11: LSB = 0.0625°C (12 bit)
B2	0: Positive Temperature Only 1: Positive and Negative Temperature
B1	0: ±2°C over the active range and ±3°C over the operating range (Class C) 1: ±1°C over the active range and ±2°C over the monitor range (Class B)
B0	0: Critical Temperature only 1: Alarm and Critical Temperature

8. Configuration Register bit 4 can be cleared (but not set) after Configuration Register bit 8 is set, by writing a “1” to Configuration Register bit 5 (i.e. the $\overline{\text{EVENT}}$ output can be de-asserted during TS shut-down periods)

Table 8. CONFIGURATION REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
RFU	RFU	RFU	RFU	RFU	HYST [1:0]		SHDN
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
TCRIT_LOCK	EVENT_LOCK	CLEAR	EVENT_STS	EVENT_CTRL	TCRIT_ONLY	EVENT_POL	EVENT_MODE

Bit	Description	
B15:B11	Reserved for future use; can not be written; should be ignored; will typically read as 0	
B10:B9 (Note 9)	00: 01: 10: 11:	Disable hysteresis Set hysteresis at 1.5°C Set hysteresis at 3°C Set hysteresis at 6°C
B8 (Note 13)	0: 1:	Thermal Sensor is enabled; temperature readings are updated at sampling rate Thermal Sensor is shut down; temperature reading is frozen to value recorded before SHDN
B7 (Note 12)	0: 1:	Critical trip register can be updated Critical trip register cannot be modified; this bit can be cleared only at POR
B6 (Note 12)	0: 1:	Alarm trip registers can be updated Alarm trip registers cannot be modified; this bit can be cleared only at POR
B5 (Note 11)	0: 1:	Always reads as 0 (self−clearing) Writing a 1 to this position clears an event recording in interrupt mode only
B4 (Note 10)	0: 1:	EVENT output pin is not being asserted EVENT output pin is being asserted
B3 (Note 9)	0: 1:	EVENT output disabled; *polarity dependent*: open−drain for bit **B1** = 0 and grounded for **B1** = 1 EVENT output enabled
B2 (Note 15)	0: 1:	event condition triggered by alarm or critical temperature limit crossing event condition triggered by critical temperature limit crossing only
B1 (Notes 9, 14)	0: 1:	EVENT output active low EVENT output active high
B0 (Note 9)	0: 1:	Comparator mode Interrupt mode

9. Can not be altered (set or cleared) as long as either one of the two lock bits, B6 or B7 is set.
10. This bit is a *polarity independent* ‘software’ copy of the $\overline{\text{EVENT}}$ pin, i.e. it is under the control of B3.
11. Writing a ‘1’ to this bit clears an event condition in Interrupt mode, but has no effect in comparator mode. When read, this bit always returns 0. Once the measured temperature exceeds the critical limit, setting this bit has no effect (see Figure 12).
12. Cleared at power-on reset (POR). Once set, this bit can only be cleared by a POR condition.
13. The TS powers up into active mode, i.e. this bit is cleared at power-on reset (POR). When the TS is shut down the ADC is disabled and the temperature reading is frozen to the most recently recorded value. The TS can not be shut down (B8 can not be set) as long as either one of the two lock bits, B6 or B7 is set. However, the bit can be cleared at any time.
14. The $\overline{\text{EVENT}}$ output is “open-drain” and requires an external pull-up resistor for either polarity. The “natural” polarity is “active low”, as it allows “wired-or” operation on the EVENT bus.
15. Can not be set as long as lock bit B6 is set.

Table 9. HIGH LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 10. LOW LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 11. TCRIT LIMIT REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
0	0	0	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Table 12. TEMPERATURE DATA REGISTER

B15	B14	B13	B12	B11	B10	B9	B8
TCRIT	HIGH	LOW	Sign	128°C	64°C	32°C	16°C
B7	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
8°C	4°C	2°C	1°C	0.5°C	0.25°C (Note 16)	0.125°C (Note 16)	0.0625°C (Note 16)

16. When applicable (as defined by Capability bit TRES), unsupported bits will read as 0

Bit	Description
B15	0: Temperature is below the TCRIT limit 1: Temperature is equal to or above the TCRIT limit
B14	0: Temperature is equal to or below the High limit 1: Temperature is above the High limit
B13	0: Temperature is equal to or above the Low limit 1: Temperature is below the Low limit

Register Data Format

The values used in the temperature data register and the 3 temperature trip point registers are expressed in two's complement format. The measured temperature value is expressed with 12−bit resolution, while the 3 trip temperature limits are set with 10−bit resolution. The total temperature range is arbitrarily defined as 256°C, thus yielding an LSB of 0.0625°C for the measured temperature and 0.25°C for the 3 limit values. Bit B12 in all temperature registers represents the sign, with a '0' indicating a positive, and a '1' a negative value. In two's complement format, negative values are obtained by complementing their positive counterpart and adding a '1', so that the sum of opposite signed numbers, but of equal absolute value, adds up to zero.

Note that trailing '0' bits, are '0' irrespective of polarity. Therefore the don't care bits (B1 and B0) in the 10−bit resolution temperature limit registers, are always '0'.

Table 13. 12−BIT TEMPERATURE DATA FORMAT

Binary (B12 to B0)	Hex	Temperature
1 1100 1001 0000	1C90	−55°C
1 1100 1110 0000	1CE0	−50°C
1 1110 0111 0000	1E70	−25°C
1 1111 1111 1111	1FFF	−0.0625°C
0 0000 0000 0000	000	0°C
0 0000 0000 0001	001	+0.0625°C
0 0001 1001 0000	190	+25°C
0 0011 0010 0000	320	+50°C
0 0111 1101 0000	7D0	+125°C

Event Pin Functionality

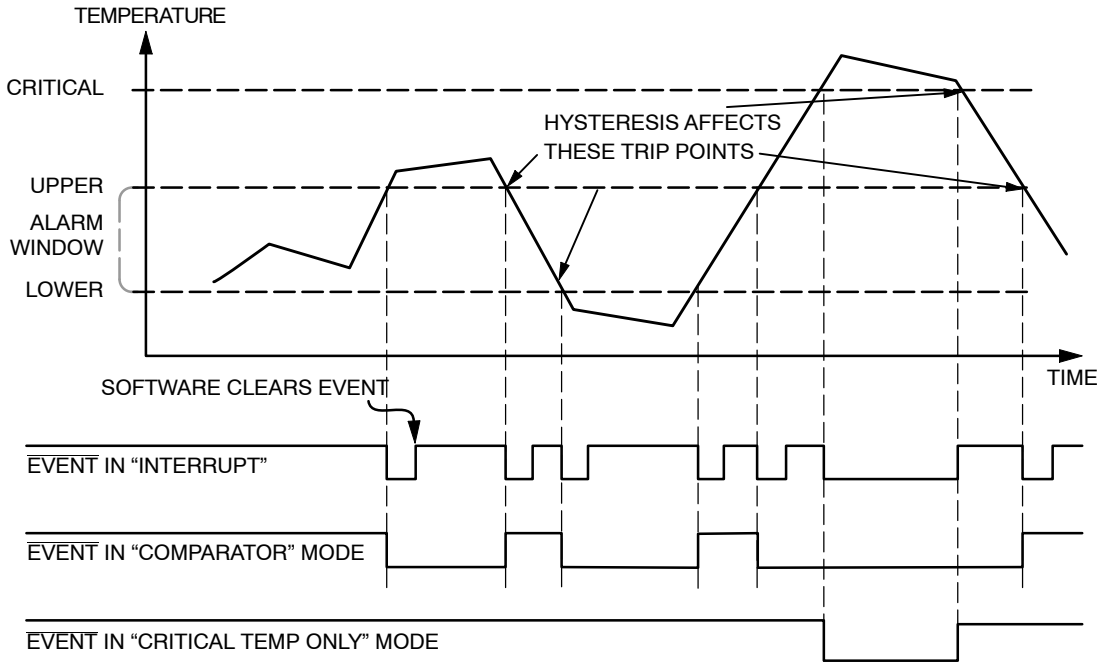
The $\overline{\text{EVENT}}$ output reacts to temperature changes as illustrated in Figure 15, and according to the operating mode defined by the Configuration register.

In **Interrupt Mode**, the enabled $\overline{\text{EVENT}}$ output will be asserted every time the temperature crosses one of the alarm window limits, and can be de−asserted by writing a '1' to the clear event bit (B5) in the configuration register. When the temperature exceeds the critical limit, the event remains asserted as long as the temperature stays above the critical limit and can not be cleared.

In **Comparator Mode**, the $\overline{\text{EVENT}}$ output is asserted outside the alarm window limits, while in **Critical Temperature Mode**, $\overline{\text{EVENT}}$ is asserted only above the critical limit. The exact trip limits are determined by the 3 temperature limit settings and the hysteresis offsets, as illustrated in Figure 16.

Following a TS shut−down request, the converter is stopped and the most recently recorded temperature value present in the TDR is frozen; the $\overline{\text{EVENT}}$ output will continue to reflect the state immediately preceding the shut−down command. Therefore, if the state of the $\overline{\text{EVENT}}$ output creates an undesirable bus condition, appropriate action must be taken either before or after shutting down the TS. This may require clearing the event, disabling the $\overline{\text{EVENT}}$ output or perhaps changing the $\overline{\text{EVENT}}$ output polarity.

In normal use, events are triggered by a change in recorded temperature, but the CAT6095 will also respond to limit register changes. Whereas recorded temperature values are updated at sampling rate frequency, limits can be modified at any time. The enabled $\overline{\text{EVENT}}$ output will react to limit changes as soon as the respective registers are updated. This feature may be useful during testing.



*EVENT cannot be cleared once the DUT temperature is greater than the critical temperature

Figure 15. Event Detail

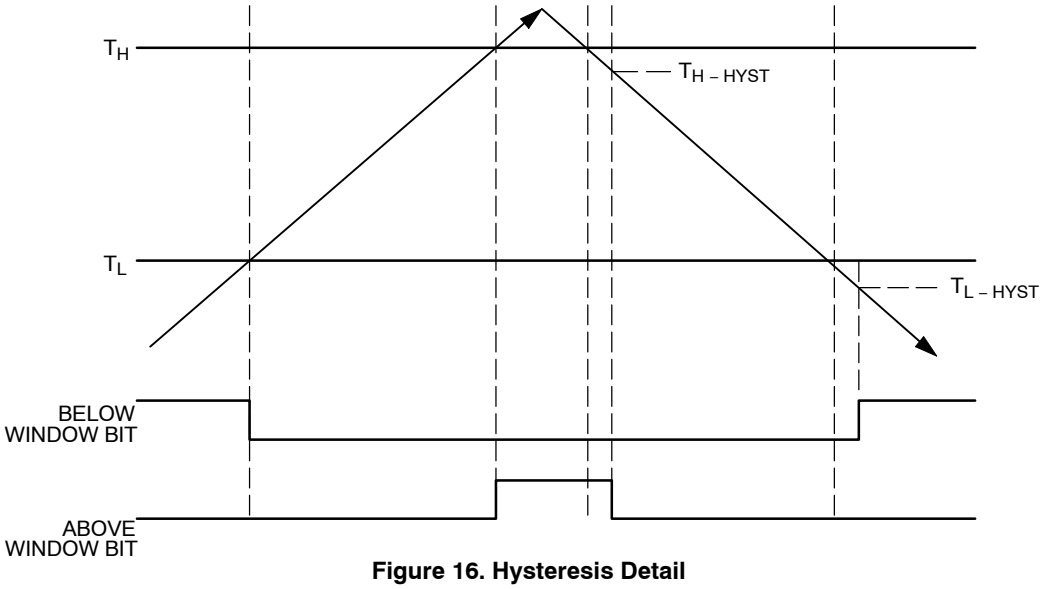
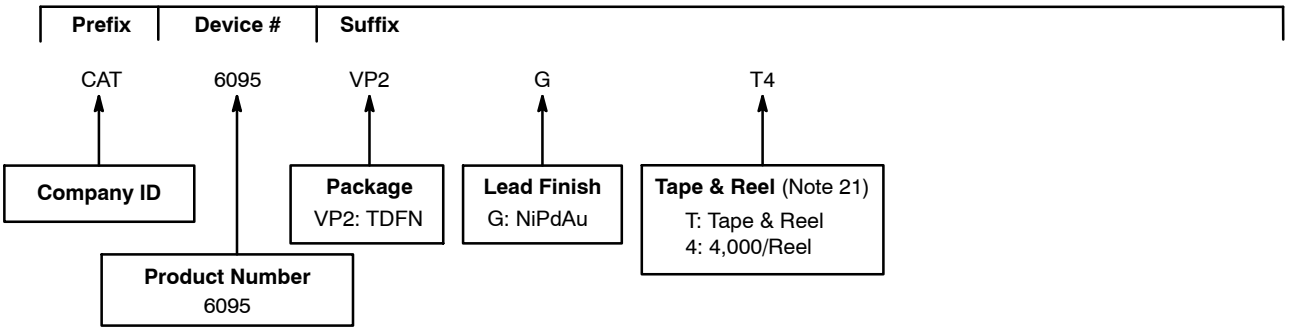


Figure 16. Hysteresis Detail

Example of Ordering Information



17. All packages are RoHS−compliant (Lead−free, Halogen−free)
18. The standard lead finish is NiPdAu.
19. This device used in the above example is a CAT6095, in TDFN, NiPdAu Lead Frame, Tape & Reel, 4,000/Reel.
20. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
21. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

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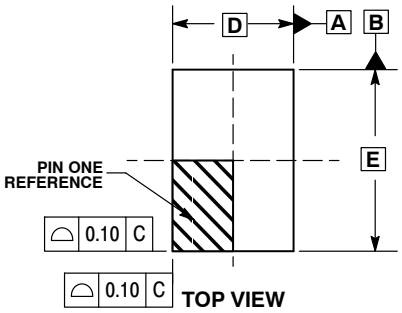
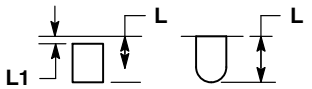
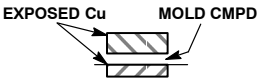
TDFN8, 2x3, 0.5P
CASE 511AK
ISSUE B

DATE 18 MAR 2015

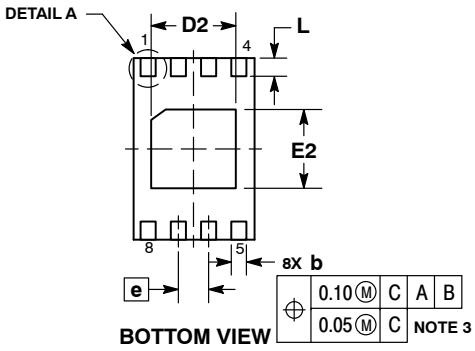




DETAIL A
ALTERNATE CONSTRUCTIONS



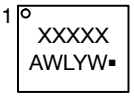
DETAIL B
ALTERNATE CONSTRUCTION



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.30	1.50
E	3.00 BSC	
E2	1.20	1.40
e	0.50 BSC	
L	0.20	0.40
L1	---	0.15

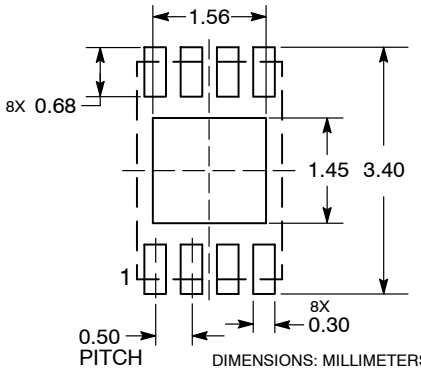
GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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