

Hall Effect Latch

High Precision Automotive Hall Effect Latch

TLE4961-1L

SP000848038

TLE4961-1L

Data Sheet

Revision 1.2, 2019-12-20

Sense & Control

Table of contents

	Table of contents	2
	List of tables	3
	List of figures	4
1	Product description	5
1.1	Overview	5
1.2	Features	5
1.3	Target applications	6
1.4	Product validation	6
2	Functional description	7
2.1	General	7
2.2	Pin configuration (top view)	7
2.3	Pin description	7
2.4	Block diagram	8
2.5	Functional block description	9
2.6	Default start-up behavior	10
3	Specification	11
3.1	Application circuit	11
3.2	Absolute maximum ratings	12
3.3	Operating range	13
3.4	Electrical and magnetic characteristics	14
3.5	Electro magnetic compatibility	16
4	Package information	18
4.1	Package outline PG-SSO-3-2	18
4.2	PG-SSO-3-2 distance between chip and package	19
4.3	Package marking	19
5	Graphs of the magnetic parameters	20
6	Graphs of the electrical parameters	21
7	Revision history	26

List of tables

Table 1	Ordering information	5
Table 2	Pin description PG-SSO-3-2	7
Table 3	Absolute maximum rating parameters	12
Table 4	ESD protection ($T_A = 25^\circ\text{C}$)	13
Table 5	Operating conditions parameters	13
Table 6	General electrical characteristics	14
Table 7	Magnetic characteristics	15
Table 8	Magnetic compatibility	16
Table 9	Electro magnetic compatibility	17

List of figures

Figure 1	TLE4961-1L in the PG-SSO-3-2 package.....	5
Figure 2	Pin configuration and center of sensitive area.....	7
Figure 3	Functional block diagram TLE4961-1L.....	8
Figure 4	Timing diagram TLE4961-1L.....	9
Figure 5	Output signal TLE4961-1L.....	9
Figure 6	Start-up behavior of the TLE4961-1L.....	10
Figure 7	Application circuit 1: with external resistor.....	11
Figure 8	Application circuit 2: without external resistor.....	11
Figure 9	Definition of magnetic field direction PG-SSO-3-2.....	15
Figure 10	EMC test circuit.....	16
Figure 11	PG-SSO-3-2 package outline (all dimensions in mm).....	18
Figure 12	Distance between chip and package.....	19
Figure 13	Marking of TLE4961-1L.....	19
Figure 14	Operating point (B_{OP}) of the TLE4961-1L over temperature.....	20
Figure 15	Release point (B_{RP}) of the TLE4961-1L over temperature.....	20
Figure 16	Hysteresis (B_{HYS}) of the TLE4961-1L over temperature.....	20
Figure 17	Power on time t_{PON} of the TLE4961-1L over temperature.....	21
Figure 18	Signal delay time of the TLE4961-1L over temperature.....	21
Figure 19	Supply current of the TLE4961-1L over temperature.....	21
Figure 20	Supply current of the TLE4961-1L over supply voltage.....	22
Figure 21	Output current limit of the TLE4961-1L over temperature.....	22
Figure 22	Output current limit of the TLE4961-1L over applied pull-up voltage.....	22
Figure 23	Output fall time of the TLE4961-1L over temperature.....	23
Figure 24	Output fall time of the TLE4961-1L over applied pull-up voltage.....	23
Figure 25	Output rise time of the TLE4961-1L over temperature.....	23
Figure 26	Output rise time of the TLE4961-1L over applied pull-up voltage.....	24
Figure 27	Output leakage current of the TLE4961-1L over temperature.....	24
Figure 28	Saturation voltage of the TLE4961-1L over temperature.....	24
Figure 29	Saturation voltage of the TLE4961-1L over output current.....	25
Figure 30	Effective noise of the TLE4961-1L thresholds over temperature.....	25
Figure 31	Output signal jitter of the TLE4961-1L over temperature.....	25

Product description

1 Product description



RoHS



1.1 Overview

Characteristic	Supply Voltage	Supply Current	Sensitivity	Interface	Temperature
Bipolar Hall Effect Latch	3.0 V ~ 32 V	1.6 mA	High B_{OP} : 2 mT B_{RP} : -2 mT	Open Drain Output	-40°C to 170°C

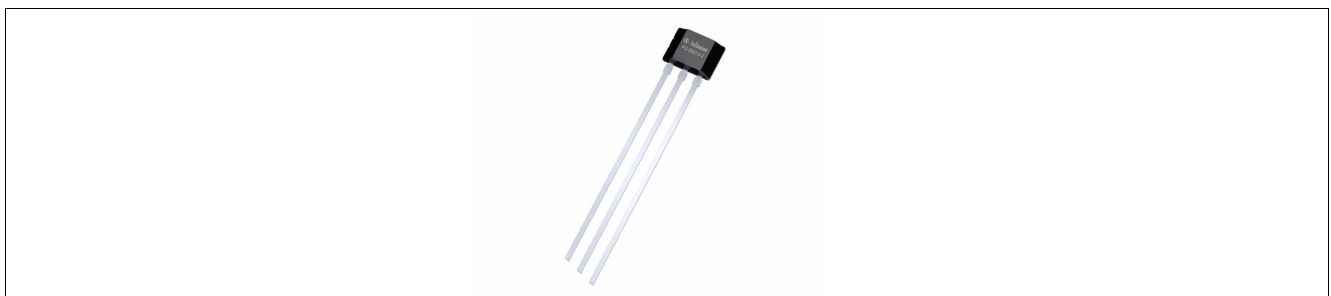


Figure 1 TLE4961-1L in the PG-SSO-3-2 package

1.2 Features

- 3.0 V to 32 V operating supply voltage
- Operation from unregulated power supply
- Reverse polarity protection (-18 V)
- Overvoltage capability up to 42 V without external resistor
- Output overcurrent and overtemperature protection
- Active error compensation
- High stability of magnetic thresholds
- Low jitter (typ. 0.35 μ s)
- High ESD performance
- Leaded package PG-SSO-3-2

Table 1 Ordering information

Product name	Product type	Ordering code	Package
TLE4961-1L	Hall Effect Latch	SP000848038	PG-SSO-3-2

Product description**1.3 Target applications**

Target applications for the TLE496x Hall Latch family are all applications which require a high precision Hall Latch with an operating temperature range from -40°C to 170°C. Its superior supply voltage range from 3.0 V to 32 V with overvoltage capability (e.g. load-dump) up to 42 V without external resistor makes it ideally suited for automotive and industrial applications.

The magnetic behavior as a latch and switching thresholds of typical ± 2 mT make the device especially suited for the use with a pole wheel for index counting applications, e.g. power closing and window lifter.

1.4 Product validation

Qualified for automotive applications. Product validation according to AEC-Q100.

Functional description

2 Functional description

2.1 General

The TLE4961-1L is an integrated Hall effect latch designed specifically for highly accurate applications with superior supply voltage capability, operating temperature range and temperature stability of the magnetic thresholds.

2.2 Pin configuration (top view)

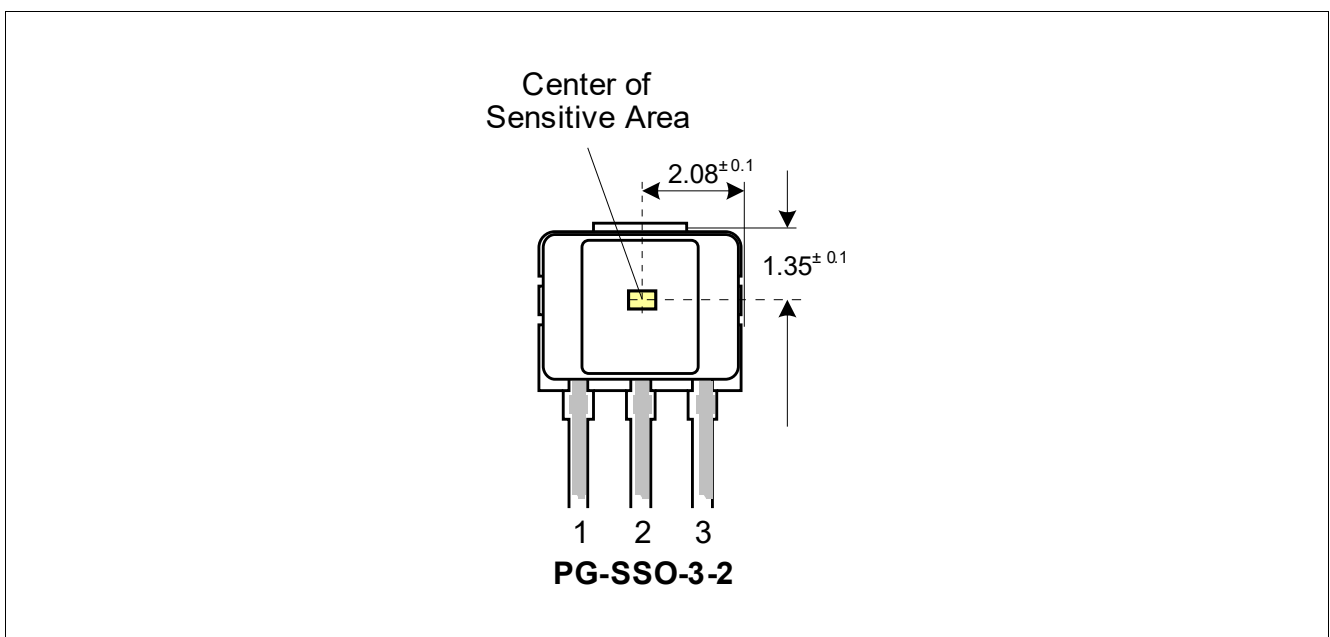


Figure 2 Pin configuration and center of sensitive area

2.3 Pin description

Table 2 Pin description PG-SSO-3-2

Pin no.	Symbol	Function
1	VDD	Supply voltage
2	GND	Ground
3	Q	Output

Functional description

2.4 Block diagram



Figure 3 Functional block diagram TLE4961-1L

Functional description

2.5 Functional block description

The chopped Hall IC switch comprises a Hall probe, bias generator, compensation circuits, oscillator and output transistor.

The bias generator provides currents for the Hall probe and the active circuits. Compensation circuits stabilize the temperature behavior and reduce influence of technology variations.

The active error compensation (chopping technique) rejects offsets in the signal path and the influence of mechanical stress to the Hall probe caused by molding and soldering processes and other thermal stress in the package. The chopped measurement principle together with the threshold generator and the comparator ensures highly accurate and temperature stable magnetic thresholds.

The output transistor has an integrated overcurrent and overtemperature protection.



Figure 4 Timing diagram TLE4961-1L

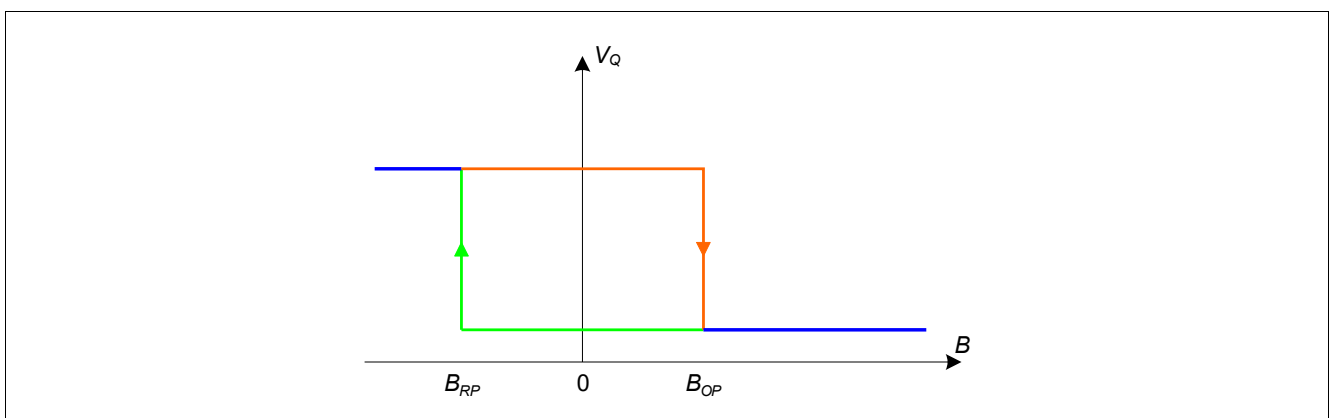


Figure 5 Output signal TLE4961-1L

Functional description

2.6 Default start-up behavior

The magnetic thresholds exhibit a hysteresis $B_{HYS} = B_{OP} - B_{RP}$. In case of a power-on with a magnetic field B within hysteresis ($B_{OP} > B > B_{RP}$) the output of the sensor is set to the pull up voltage level (V_Q) per default. After the first crossing of B_{OP} or B_{RP} of the magnetic field the internal decision logic is set to the corresponding magnetic input value.

V_{DDA} is the internal supply voltage which is following the external supply voltage V_{DD} .

This means for $B > B_{OP}$ the output is switching, for $B < B_{RP}$ and $B_{OP} > B > B_{RP}$ the output stays at V_Q .

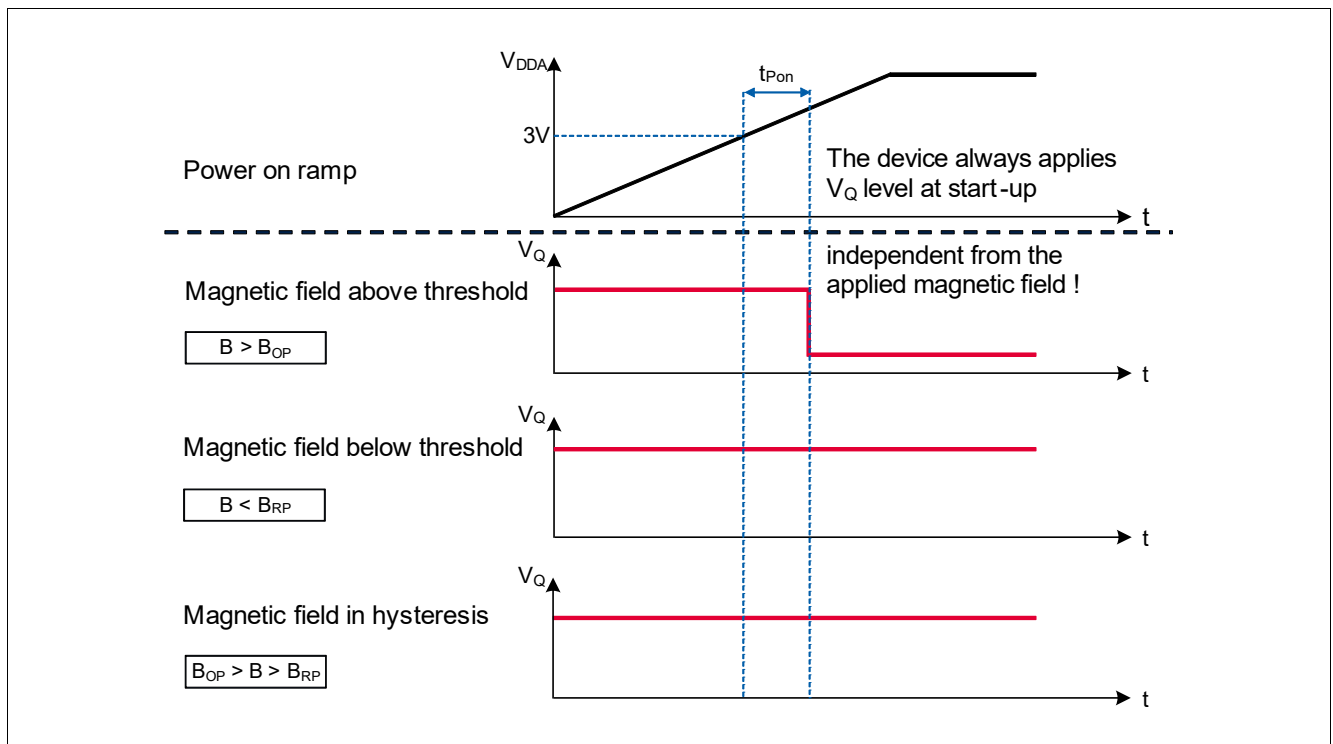


Figure 6 Start-up behavior of the TLE4961-1L

Specification

3 Specification

3.1 Application circuit

The following **Figure 7** shows one option of an application circuit. As explained above the resistor R_S can be left out (see **Figure 8**). The resistor R_Q has to be in a dimension to match the applied V_S to keep I_Q limited to the operating range of maximum 25 mA.

e.g.: $V_S = 12\text{ V}$; $I_Q = 12\text{ V}/1200\ \Omega = 10\text{ mA}$

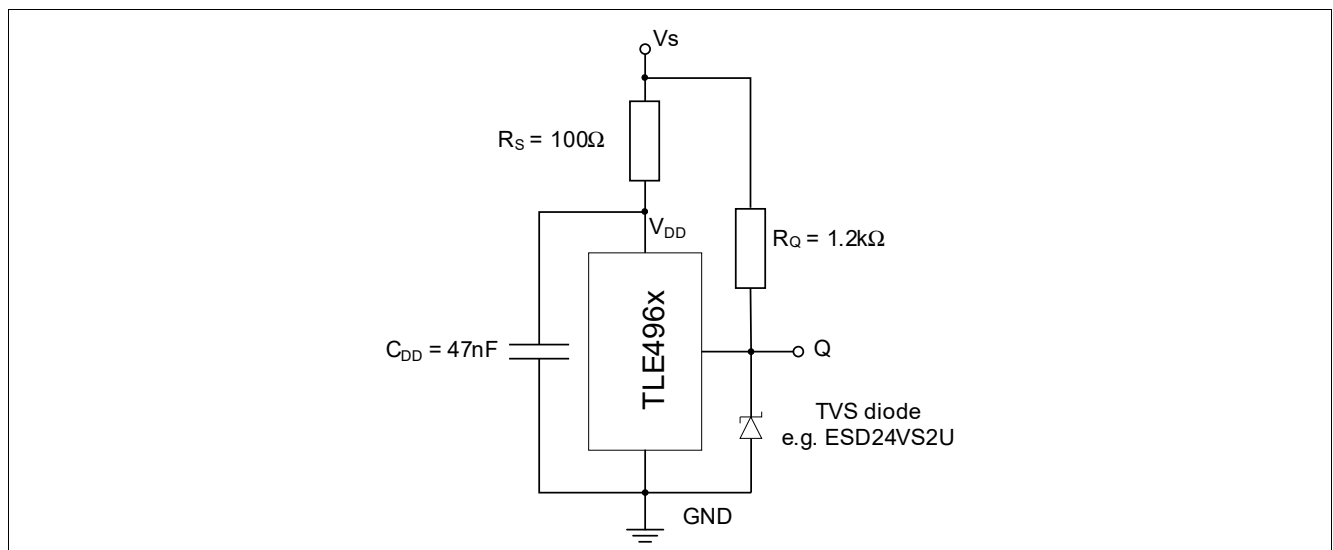


Figure 7 Application circuit 1: with external resistor

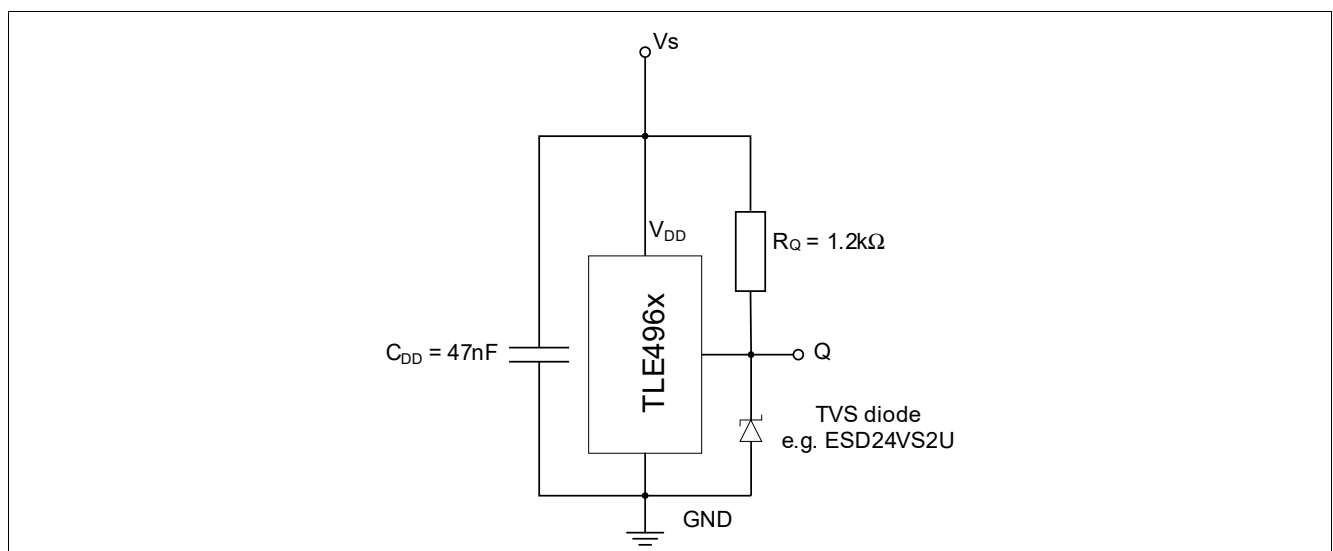


Figure 8 Application circuit 2: without external resistor

Specification

3.2 Absolute maximum ratings

Table 3 Absolute maximum rating parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage ¹⁾	V_{DD}	-18	–	32 42	V	– 10h, no external resistor required
Output voltage	V_Q	-0.5	–	32	V	–
Reverse output current	I_Q	-70	–	–	mA	–
Junction temperature ¹⁾	T_J	-40	–	155 165 175 195	°C	for 2000h (not additive) for 1000h (not additive) for 168h (not additive) for 3 x 1h (additive)
Storage temperature	T_S	-40	–	150	°C	–
Thermal resistance Junction ambient	R_{thJA}	–	–	200	K/W	for PG-SSO-3-2 (2s2p)
Thermal resistance Junction lead	R_{thJL}	–	–	150	K/W	for PG-SSO-3-2

1) This lifetime statement is an anticipation based on an extrapolation of Infineon's qualification test results. The actual lifetime of a component depends on its form of application and type of use etc. and may deviate from such statement. The lifetime statement shall in no event extend the agreed warranty period.

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Calculation of the dissipated power P_{DIS} and junction temperature T_J of the chip (SSO3 example):

e.g. for: $V_{DD} = 12\text{ V}$, $I_S = 2.5\text{ mA}$, $V_{QSAT} = 0.5\text{ V}$, $I_Q = 20\text{ mA}$

Power dissipation: $P_{DIS} = 12\text{ V} \times 2.5\text{ mA} + 0.5\text{ V} \times 20\text{ mA} = 30\text{ mW} + 10\text{ mW} = 40\text{ mW}$

Temperature $\Delta T = R_{thJA} \times P_{DIS} = 200\text{ K/W} \times 40\text{ mW} = 8\text{ K}$

For $T_A = 150^\circ\text{C}$: $T_J = T_A + \Delta T = 150^\circ\text{C} + 8\text{ K} = 158^\circ\text{C}$

Specification

Table 4 ESD protection¹⁾ ($T_A = 25^\circ\text{C}$)

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
ESD voltage (HBM) ²⁾	V_{ESD}	-7	-	7	kV	$R = 1.5 \text{ k}\Omega$, $C = 100 \text{ pF}$
ESD voltage (CDM) ³⁾	V_{ESD}	-1	-	1	kV	-
ESD voltage (system level) ⁴⁾	V_{ESD}	-15	-	15	kV	with circuit shown in Figure 7 and Figure 8

1) Characterization of ESD is carried out on a sample basis, not subject to production test.

2) Human Body Model (HBM) tests according to ANSI/ESDA/JEDEC JS-001.

3) Charge device model (CDM) tests according to JESD22-C101.

4) Gun test (2 k Ω / 330 pF or 330 Ω / 150 pF) according to ISO 10605-2008.

3.3 Operating range

The following operating conditions must not be exceeded in order to ensure correct operation of the TLE4961-1L.

All parameters specified in the following sections refer to these operating conditions unless otherwise mentioned.

The maximum tested magnetic field is 600 mT.

Table 5 Operating conditions parameters

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	3.0	-	32 ¹⁾	V	-
Output voltage	V_{Q}	-0.3	-	32	V	-
Junction temperature	T_{J}	-40	-	170	$^\circ\text{C}$	-
Output current	I_{Q}	0	-	25	mA	-
Magnetic signal input frequency ²⁾	f_{SW}	0	-	10	kHz	-

1) Latch-up test with factor 1.5 is not covered. Please see max ratings also.

2) For operation at the maximum switching frequency the magnetic input signal must be 1.4 times higher than for static fields. This is due to the -3 dB corner frequency of the internal low-pass filter in the signal path.

Specification

3.4 Electrical and magnetic characteristics

Product characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production and correspond to $V_{DD} = 12\text{ V}$ and $T_A = 25^\circ\text{C}$. The below listed specification is valid in combination with the application circuit shown in [Figure 7](#) and [Figure 8](#).

Table 6 General electrical characteristics

Parameter	Symbol	Values			Unit	Note or Test Condition
		Min.	Typ.	Max.		
Supply current	I_S	1.1	1.6	2.5	mA	–
Reverse current	I_{SR}	–	0.05	1	mA	for $V_{DD} = -18\text{ V}$
Output saturation voltage	V_{QSAT}	–	0.2	0.5	V	$I_Q = 20\text{ mA}$
		–	0.24	0.6	V	$I_Q = 25\text{ mA}$
Output leakage current	I_{QLEAK}	–	–	10	μA	–
Output current limitation	I_{QLIMIT}	30	56	70	mA	internally limited and thermal shutdown
Output fall time ¹⁾	t_f	0.17	0.4	1	μs	1.2 k Ω / 50 pF, see Figure 4
Output rise time ¹⁾	t_r	0.4	0.5	1	μs	1.2 k Ω / 50 pF, see Figure 4
Output jitter ¹⁾²⁾	t_{QJ}	–	0.35	1	μs	for square wave signal with 1 kHz
Delay time ¹⁾³⁾	t_d	12	15	30	μs	see Figure 4
Power-on time ¹⁾⁴⁾	t_{PON}	–	80	150	μs	$V_{DD} = 3\text{ V}$, $B \leq B_{RP} - 0.5\text{ mT}$ or $B \geq B_{OP} + 0.5\text{ mT}$
Chopper frequency ¹⁾	f_{OSC}	–	350		kHz	–

1) Not subject to production test, verified by design/characterization.

2) Output jitter is the 1 σ value of the output switching distribution.

3) Systematic delay between magnetic threshold reached and output switching.

4) Time from applying $V_{DD} = 3.0\text{ V}$ to the sensor until the output is valid.

Specification

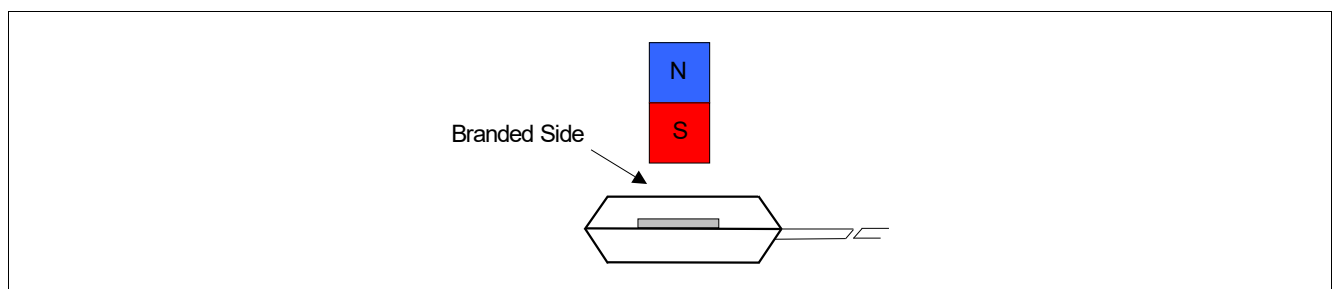
Table 7 Magnetic characteristics

Parameter	Symbol	T (°C)	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Operating point	B_{OP}	-40	0.6	2.1	3.6	mT	-
		25	0.5	2.0	3.5		
		170	0.2	1.6	3.1		
Release point	B_{RP}	-40	-3.6	-2.1	-0.6	mT	-
		25	-3.5	-2.0	-0.5		
		170	-3.1	-1.6	-0.2		
Hysteresis	B_{HYS}	-40	2.7	4.2	5.7	mT	-
		25	2.6	4.0	5.4		
		170	2.0	3.2	4.4		
Effective noise value of the magnetic switching points ¹⁾	B_{Neff}	25	-	62	-	μT	-
Temperature compensation of magnetic thresholds ²⁾	T_C	-	-	-1200	-	ppm/K	-

- 1) The magnetic noise is normal distributed and can be assumed as nearly independent to frequency without sampling noise or digital noise effects. The typical value represents the rms-value and corresponds therefore to a 1σ probability of normal distribution. Consequently a 3σ value corresponds to 99.7% probability of appearance.
- 2) Not subject to production test, verified by design/characterization.

Field direction definition

Positive magnetic fields are defined with the south pole of the magnet to the branded side of package.


Figure 9 Definition of magnetic field direction PG-SSO-3-2

Specification

3.5 Electro magnetic compatibility

Characterization of electro magnetic compatibility is carried out on a sample basis from one qualification lot. Not all specification parameters have been monitored during EMC exposure.

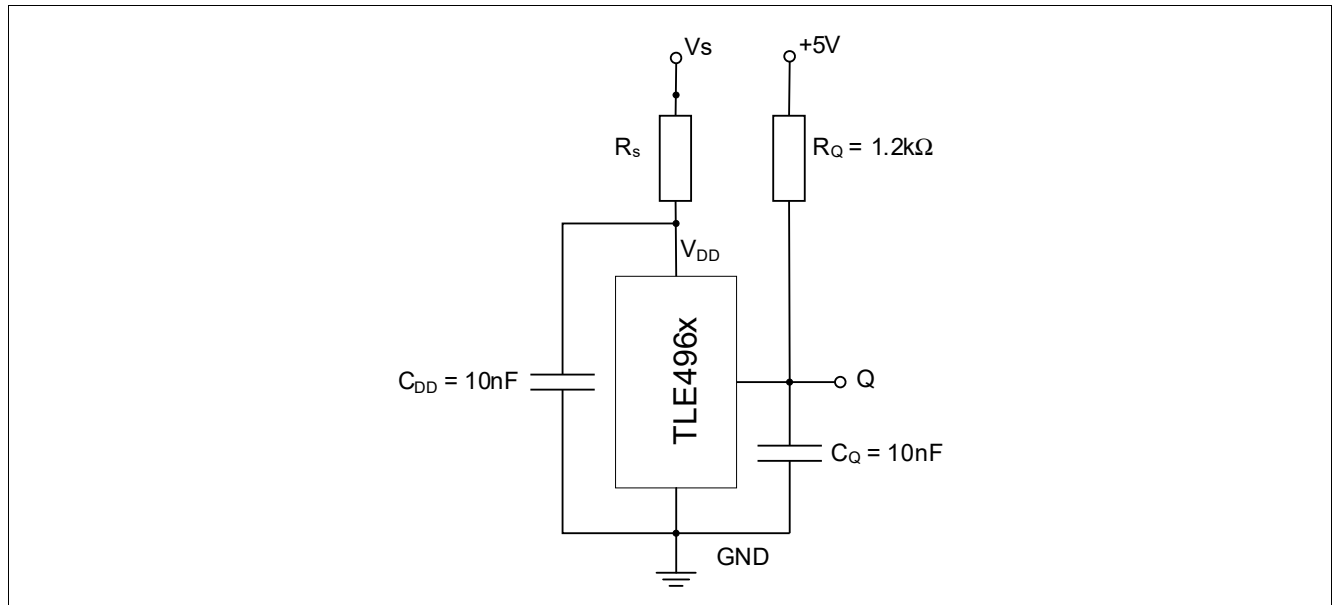


Figure 10 EMC test circuit

Ref: ISO 7637-2 (Version 2004), test circuit [Figure 10](#) (with external resistor, $R_S = 100 \Omega$)

Table 8 Magnetic compatibility

Parameter	Symbol	Level / Type	Status
Testpulse 1	V_{EMC}	-100 V	C
Testpulse 2a ¹⁾		60 V/110 V	A/C
Testpulse 2b		10 V	C
Testpulse 3a		-150 V	A
Testpulse 3b		100 V	A
Testpulse 4 ²⁾		-7 V / -5.5 V	A
Testpulse 5b ³⁾		$U_S = 86.5 \text{ V} / U_S^* = 28.5 \text{ V}$	A

1) ISO 7637-2 (2004) describes internal resistance = 2 Ω (former 10 Ω).

2) According to 7637-2 for test pulse 4 the test voltage shall be 12 V \pm 0.2 V.

3) A central load dump protection of 42 V is used. $U_S^* = 42 \text{ V} - 13.5 \text{ V}$.

Specification

Ref: ISO 7637-2 (Version 2004), test circuit [Figure 10](#) (without external resistor, $R_S = 0 \Omega$)

Table 9 Electro magnetic compatibility

Parameter	Symbol	Level / Type	Status
Testpulse 1	V_{EMC}	-50 V	C
Testpulse 2a ¹⁾		50 V	A
Testpulse 2b		10 V	C
Testpulse 3a		-150 V	A
Testpulse 3b		100 V	A
Testpulse 4 ²⁾		-7 V / 5.5 V	A
Testpulse 5b ³⁾		$U_S = 86.5 \text{ V} / U_S^* = 28.5 \text{ V}$	A

1) ISO 7637-2 (2004) describes internal resistance = 2 Ω (former 10 Ω).

2) According to 7637-2 for test pulse 4 the test voltage shall be 12 V \pm 0.2 V.

3) A central load dump protection of 42 V is used. $U_S^* = 42 \text{ V} - 13.5 \text{ V}$.

Package information

4 Package information

The TLE4961-1L is available in the through-hole leaded package PG-SSO-3-2.

4.1 Package outline PG-SSO-3-2

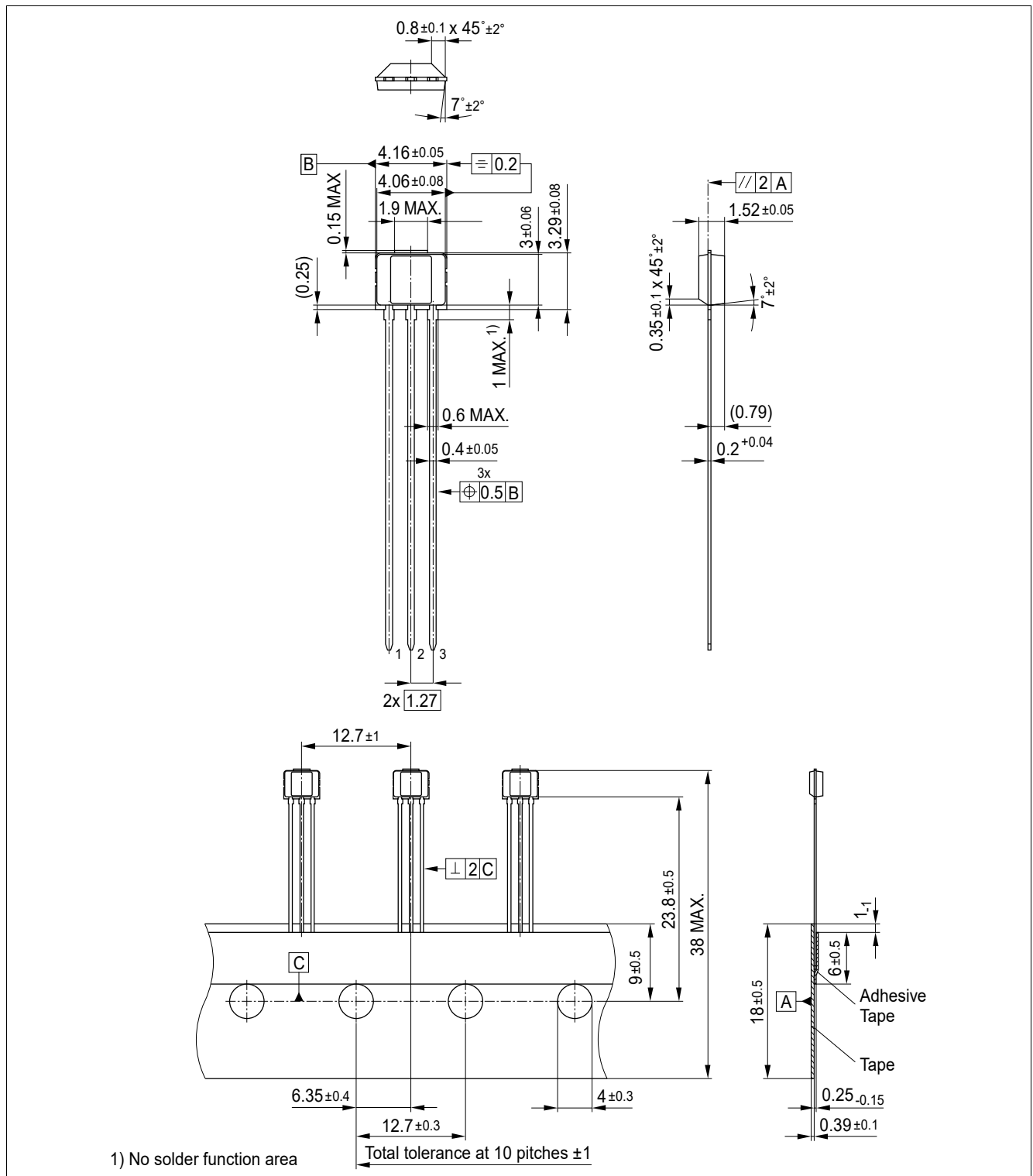


Figure 11 PG-SSO-3-2 package outline (all dimensions in mm)

Package information

4.2 PG-SSO-3-2 distance between chip and package

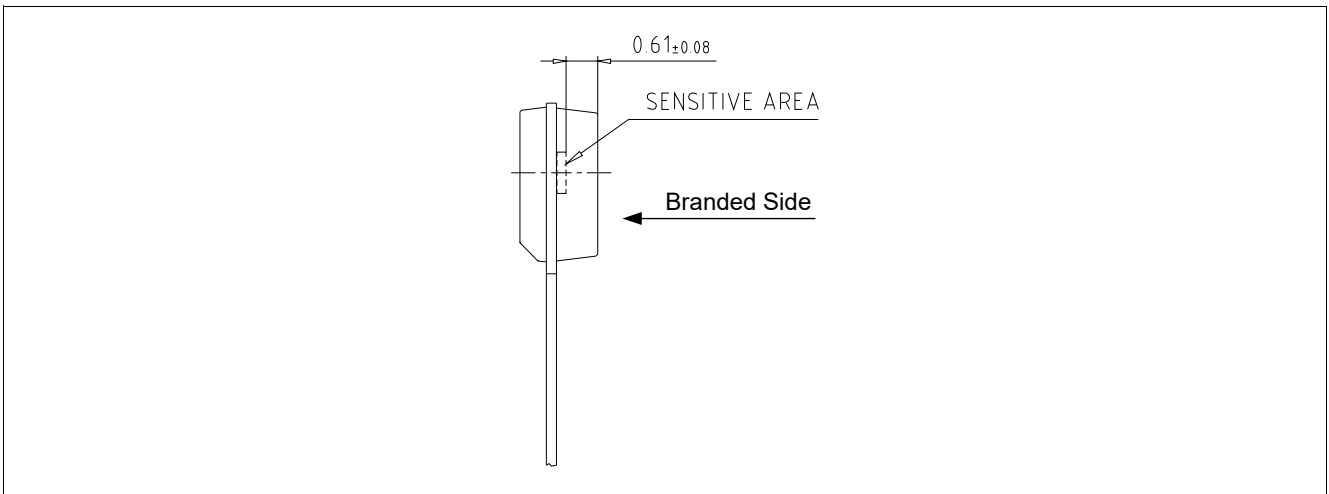


Figure 12 Distance between chip and package

4.3 Package marking

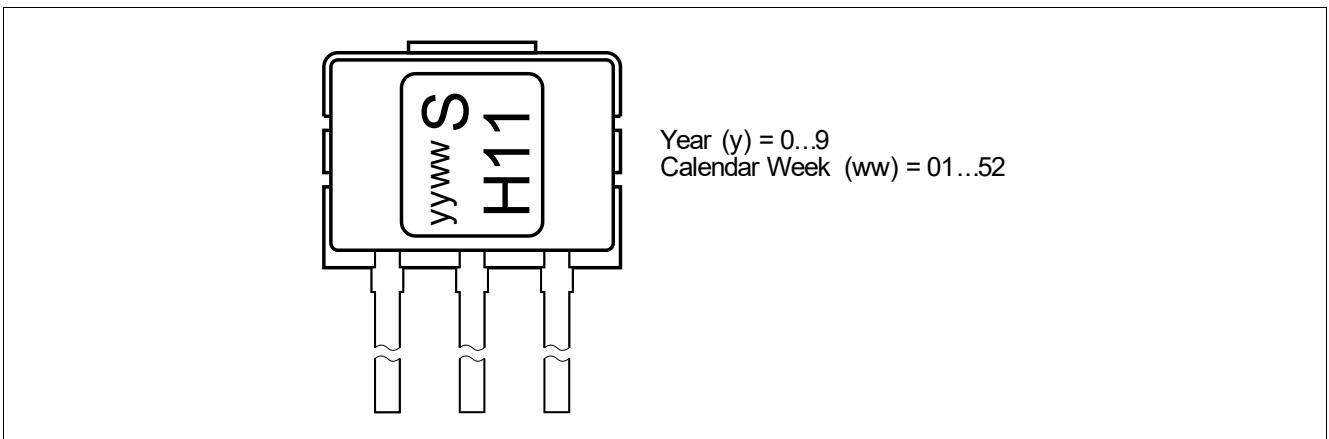


Figure 13 Marking of TLE4961-1L

Graphs of the magnetic parameters

5 Graphs of the magnetic parameters

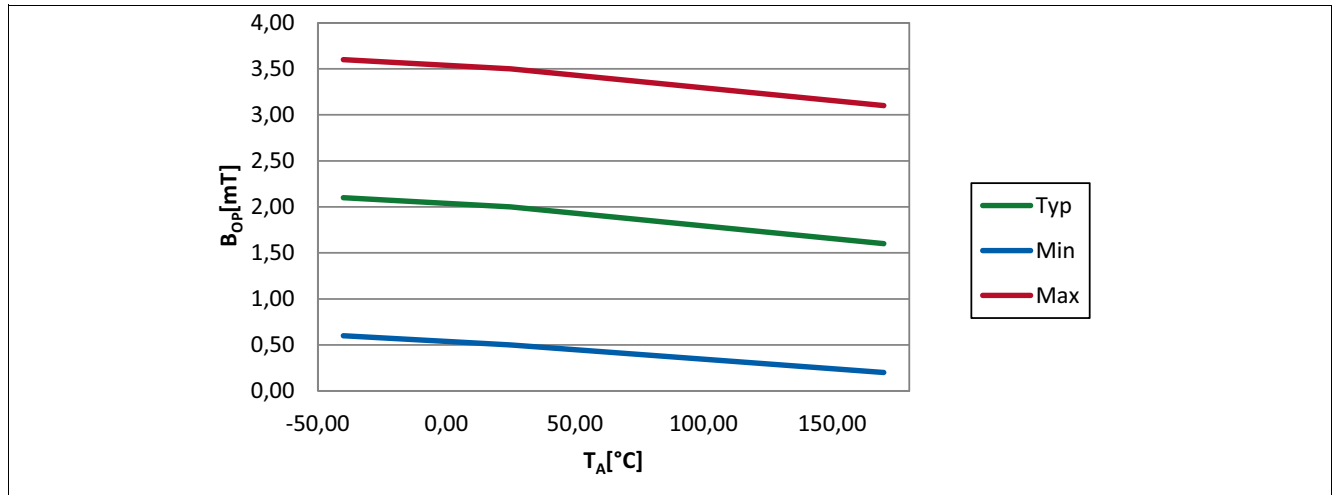


Figure 14 Operating point (B_{OP}) of the TLE4961-1L over temperature

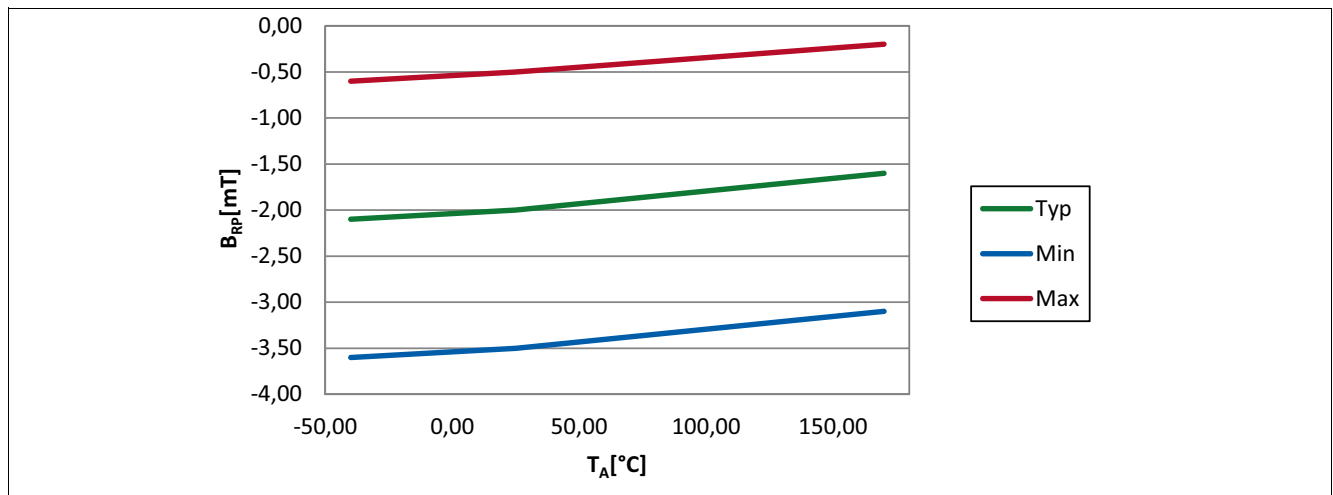


Figure 15 Release point (B_{RP}) of the TLE4961-1L over temperature

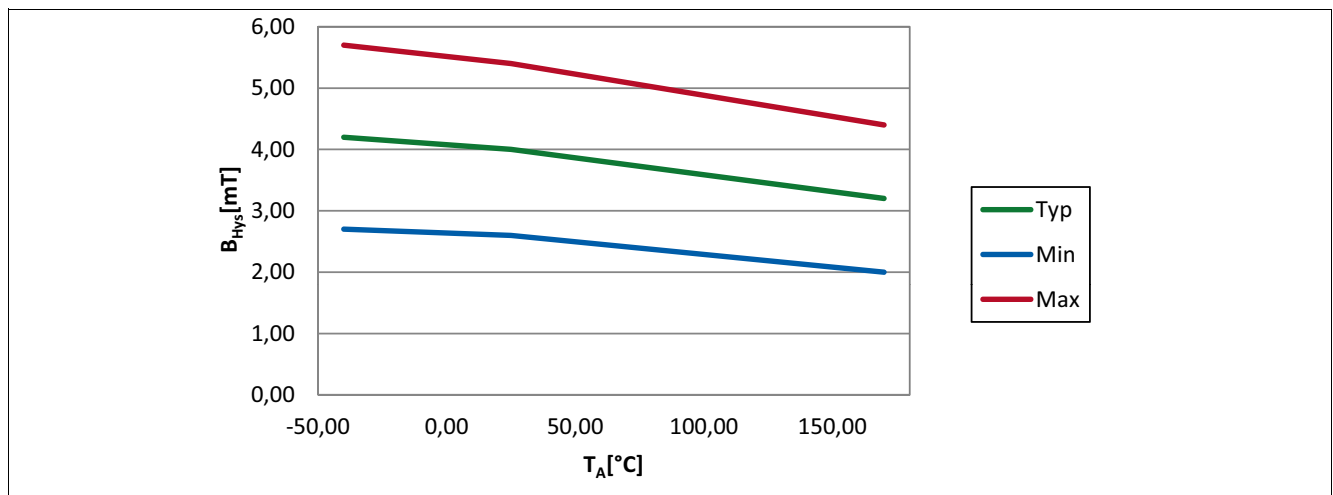


Figure 16 Hysteresis (B_{Hys}) of the TLE4961-1L over temperature

Graphs of the electrical parameters

6 Graphs of the electrical parameters

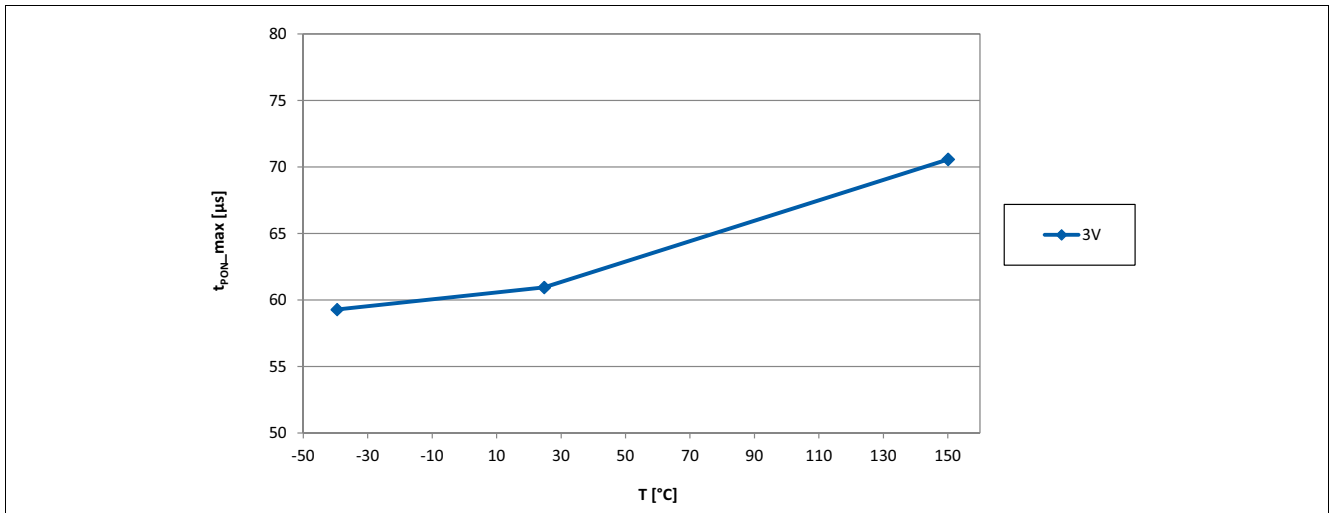


Figure 17 Power on time t_{PON} of the TLE4961-1L over temperature

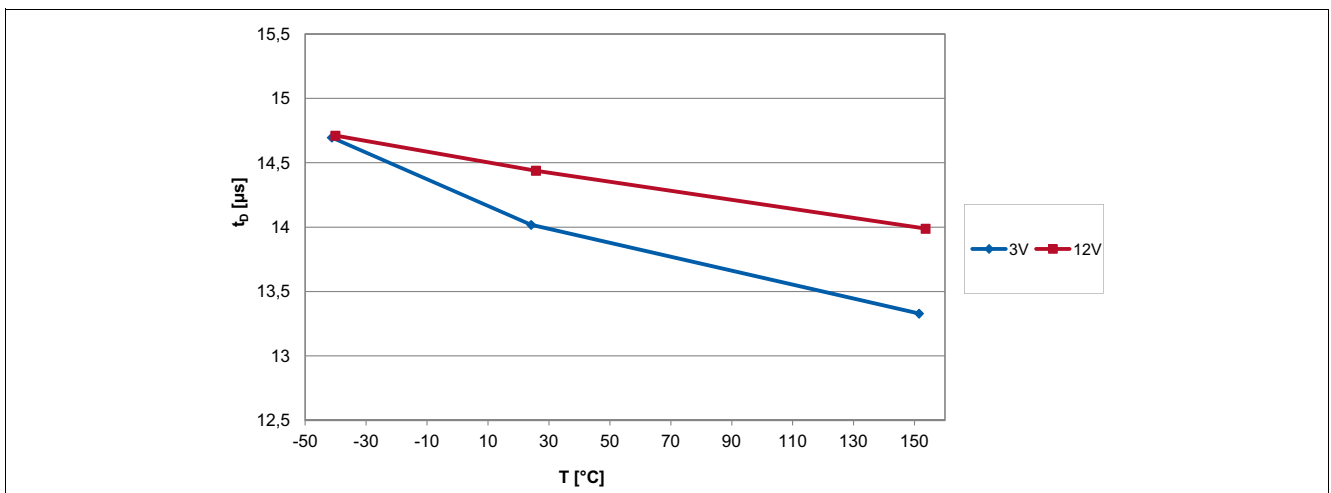


Figure 18 Signal delay time of the TLE4961-1L over temperature



Figure 19 Supply current of the TLE4961-1L over temperature

Graphs of the electrical parameters

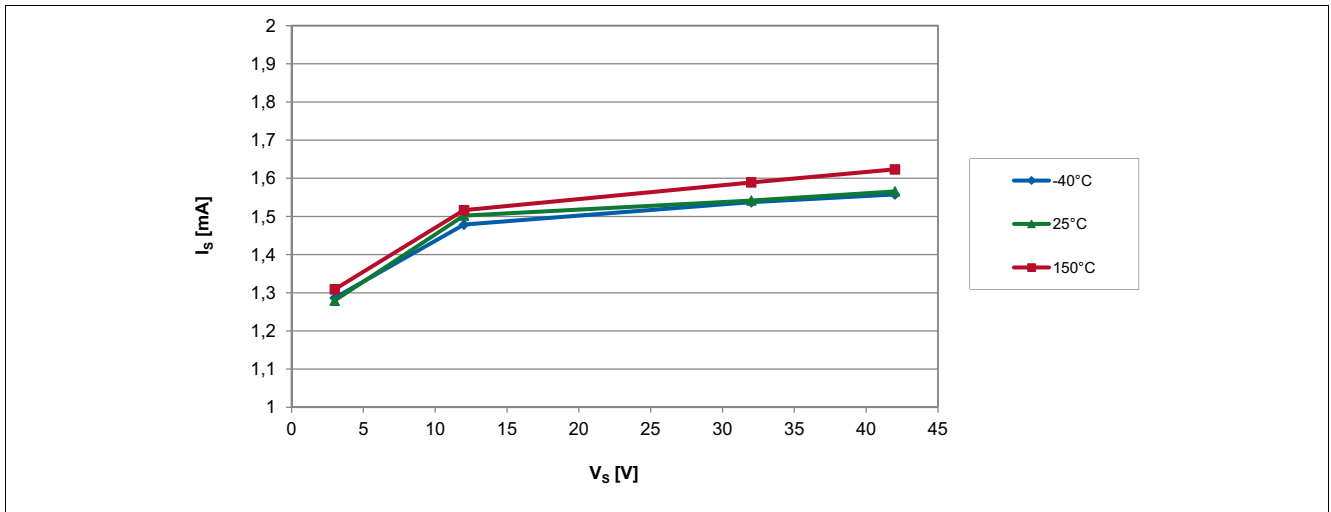


Figure 20 Supply current of the TLE4961-1L over supply voltage

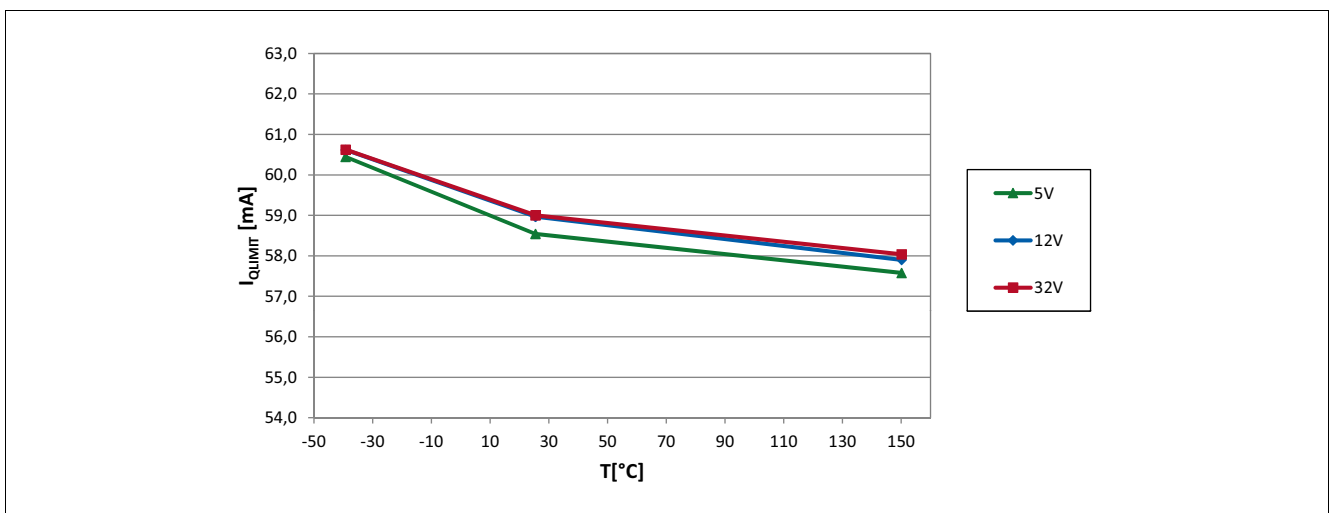


Figure 21 Output current limit of the TLE4961-1L over temperature

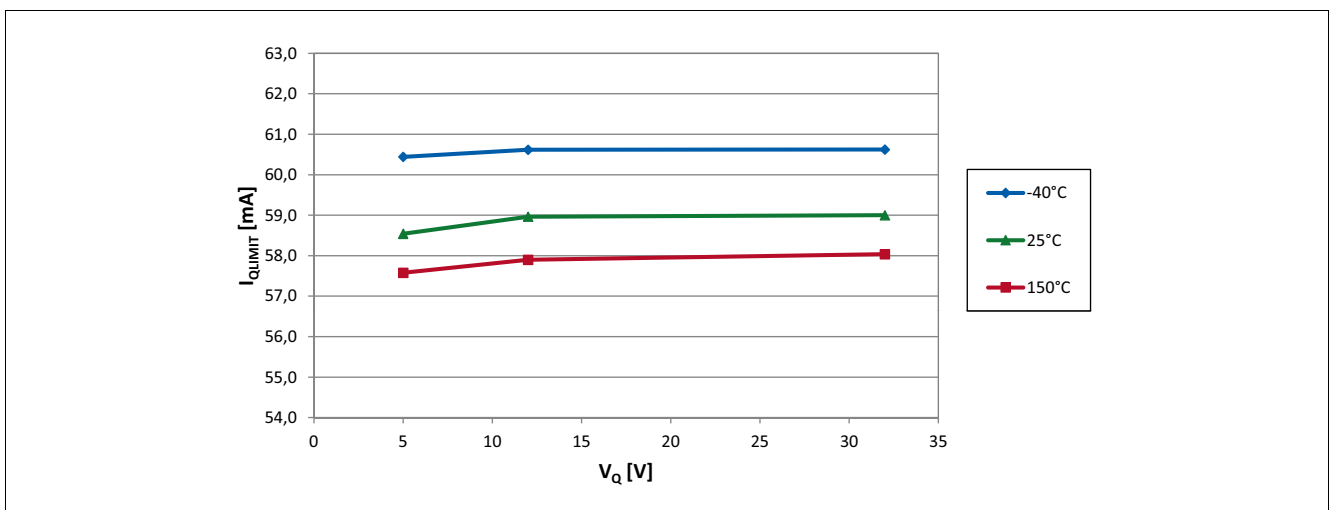


Figure 22 Output current limit of the TLE4961-1L over applied pull-up voltage

Graphs of the electrical parameters

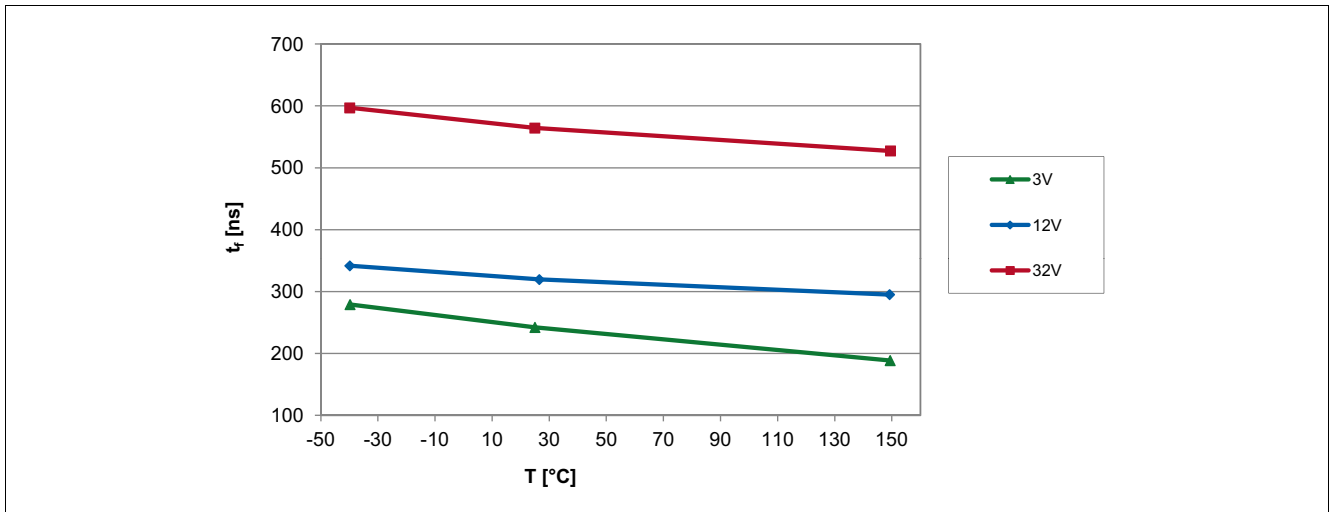


Figure 23 Output fall time of the TLE4961-1L over temperature

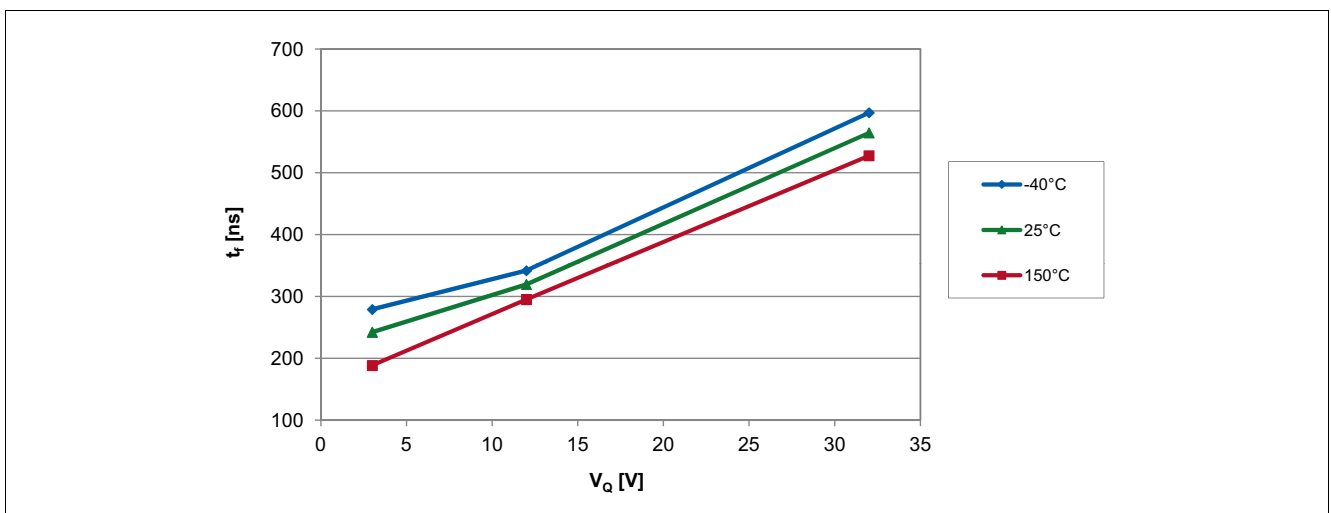


Figure 24 Output fall time of the TLE4961-1L over applied pull-up voltage

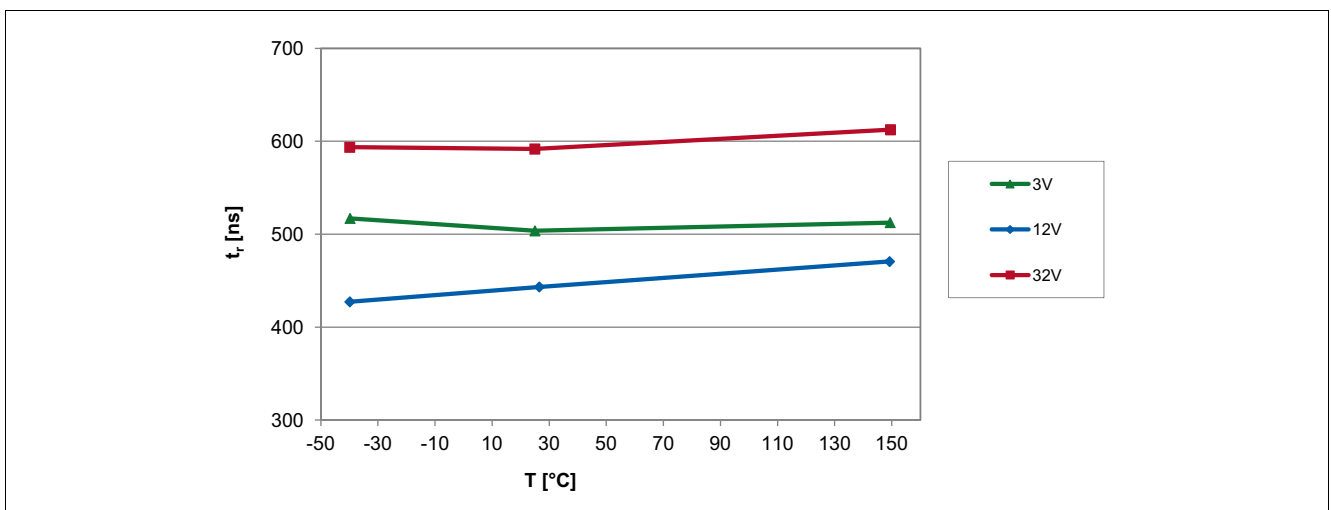


Figure 25 Output rise time of the TLE4961-1L over temperature

Graphs of the electrical parameters

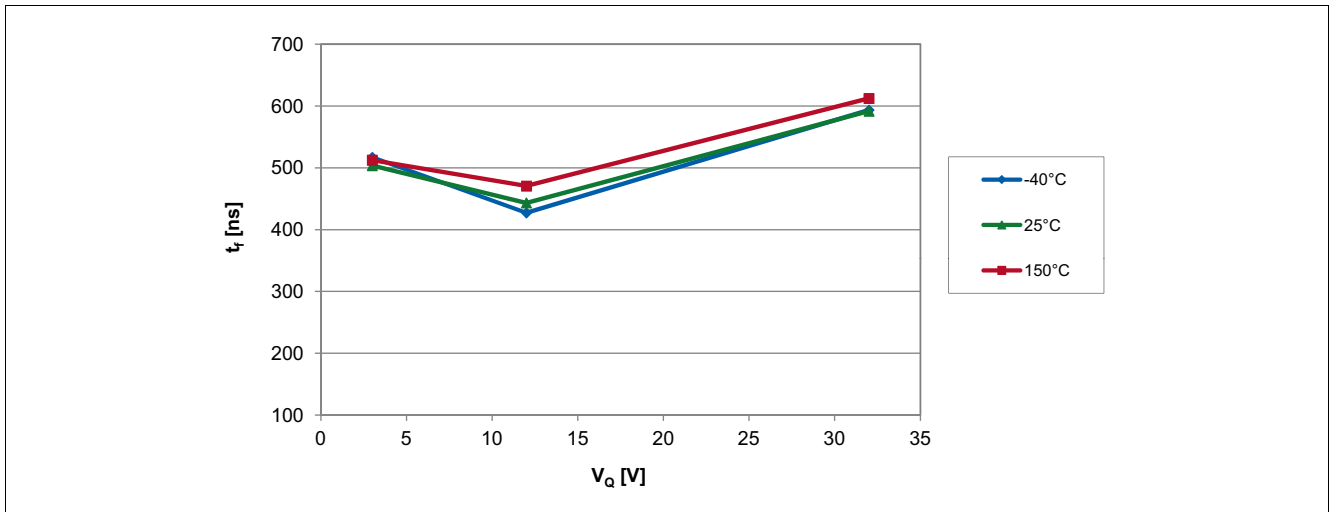


Figure 26 Output rise time of the TLE4961-1L over applied pull-up voltage



Figure 27 Output leakage current of the TLE4961-1L over temperature



Figure 28 Saturation voltage of the TLE4961-1L over temperature

Graphs of the electrical parameters

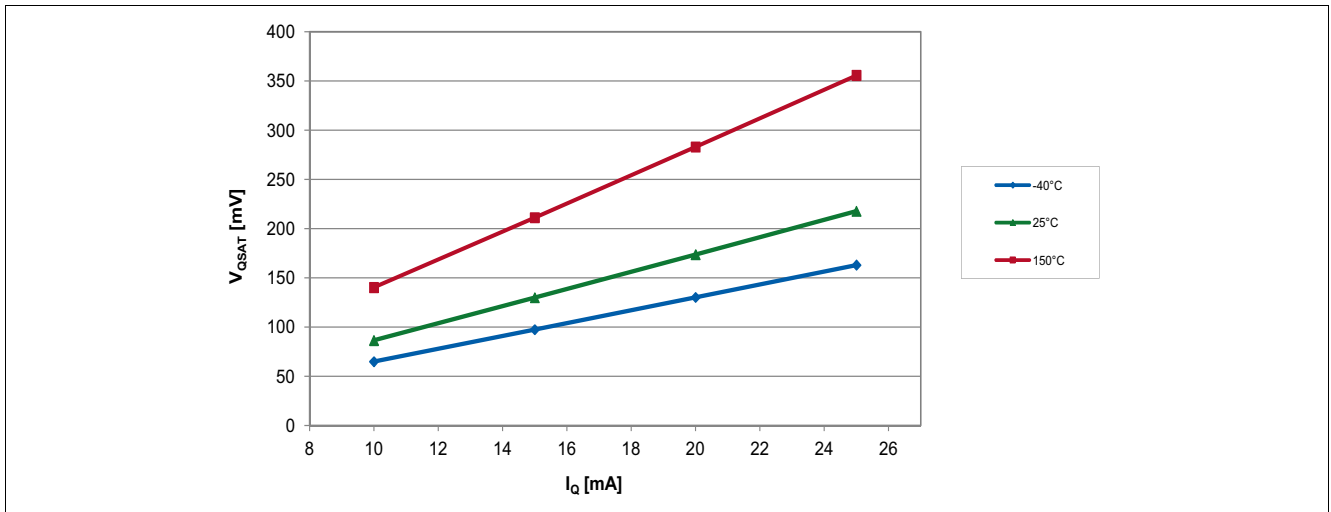


Figure 29 Saturation voltage of the TLE4961-1L over output current

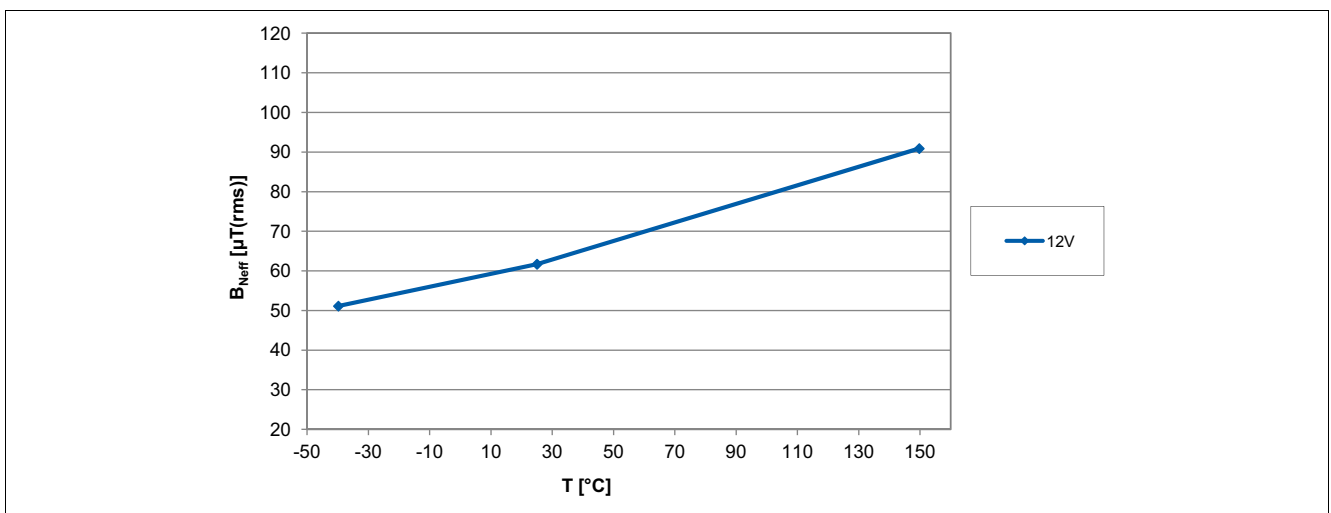


Figure 30 Effective noise of the TLE4961-1L thresholds over temperature

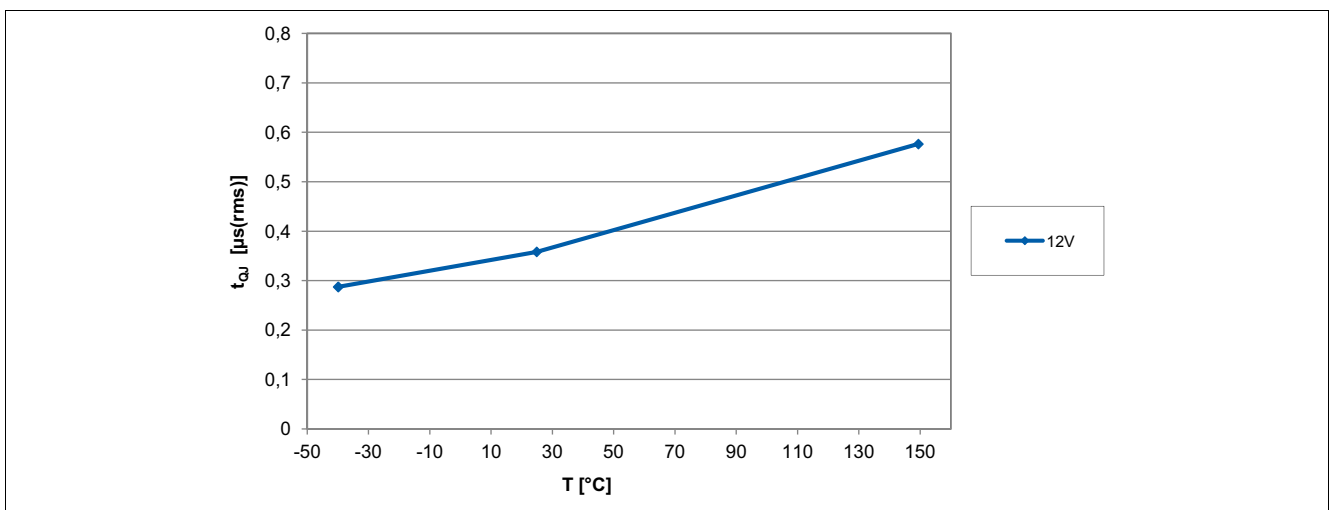


Figure 31 Output signal jitter of the TLE4961-1L over temperature

Revision history**7 Revision history**

Revision	Date	Changes
Revision 1.2	2019-12-20	Updated text and figure in Chapter 2.6 Updated standards in Table 4 Added maximum tested magnetic field in Chapter 3.3 Updated Figure 12 Editorial changes
Revision 1.0	2012-07-18	Initial release

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

www.infineon.com

Edition 2019-12-20

Published by

Infineon Technologies AG

81726 Munich, Germany

© 2019 Infineon Technologies AG.

All Rights Reserved.

Do you have a question about any aspect of this document?

Email: erratum@infineon.com

Document reference

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office. Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.