High Voltage High Current LED Driver Controller for Buck Boost or Buck-Boost Topology

General Description

The RT8452 is a current mode PWM controller designed to drive an external MOSFET for high current LED applications. With a current sense amplifier threshold of 190mV, the LED current is programmable with one external current sense resistor. With the maximum operating input voltage of 36V and output voltage up to 48V, the RT8452 is ideal for Buck, Boost or Buck-Boost operation.

With 350kHz operating frequency, the external inductor and capacitors can be small while maintaining high efficiency.

Dimming can be done by either analog or digital. A built-in clamping comparator and filter allow easy low noise analog dimming conversion from digital signal with only one external capacitor. An unique True PWM dimming control is made easy with MOSFET under LED string. A very high dimming ratio can be achieved by adopting both analog/ digital dimming and True PWM dimming together.

The RT8452 is available in WQFN-16L 3x3 and SOP-16 packages.

Ordering Information

RT8452 □□

- Package Type
  - S : SOP-16
  - QW : WQFN-16L 3x3 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

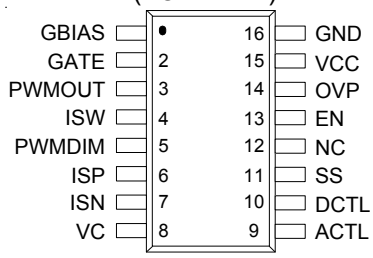
- **High Voltage Capability : V_{IN} Up to 36V, V_{OUT} Up to 48V**
- **Buck, Boost or Buck-Boost Operation**
- **Current Mode PWM with 350kHz Switching Frenquency**
- **Easy Dimming Control : Analog or Digital Converting to Analog with One External Capacitor**
- **True PWM Dimming : External FET Driver is Build-in**
- **Programmable Soft Start to Avoid Inrush Current**
- **Programmable Over Voltage Protection**
- **V_{IN} Undervoltage Lockout and Thermal Shutdown**
- **16-Lead WQFN and SOP Packages.**
- **RoHS Compliant and Halogen Free**

Applications

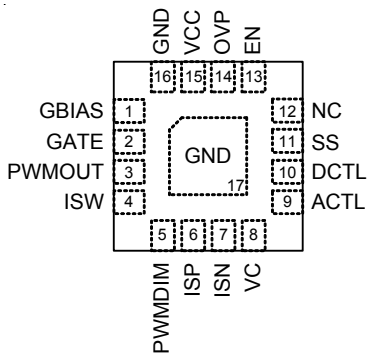
- General Industrial High Power LED Lighting
- Desk Lights and Room Lighting
- Building and Street Lighting
- Industrial Display Backlight

Pin Configuration

(TOP VIEW)



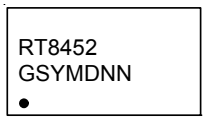
SOP-16



WQFN-16L 3x3

Marking Information

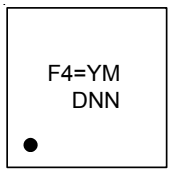
RT8452GS



RT8452GS : Product Number

YMDNN : Date Code

RT8452GQW



F4= : Product Code

YMDNN : Date Code

Typical Application Circuit

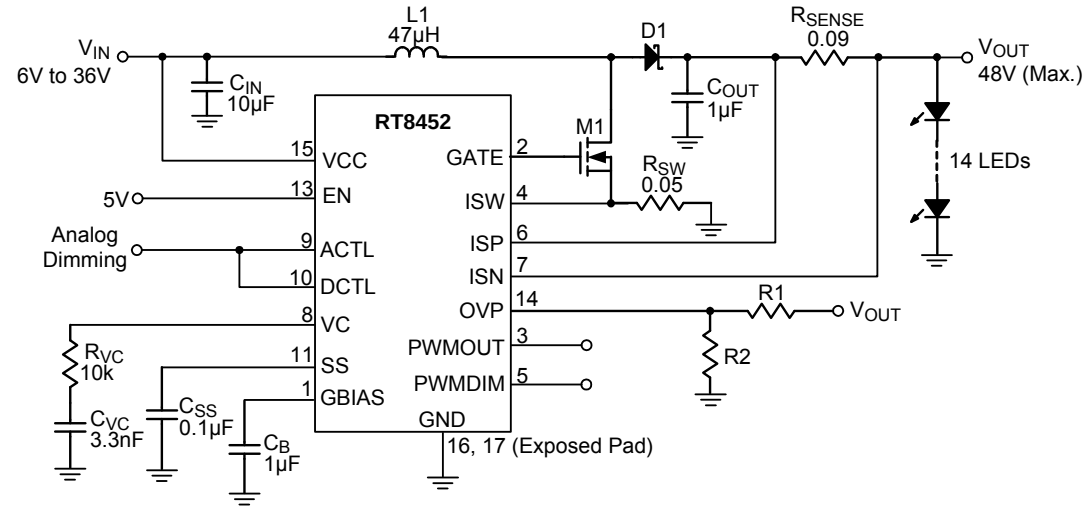


Figure 1. Analog Dimming in Boost Configuration

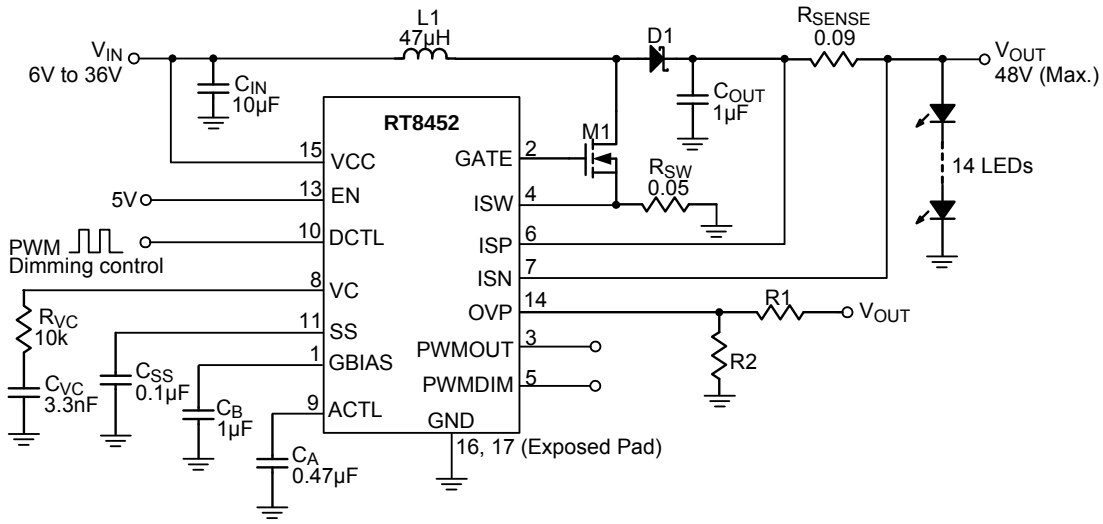


Figure 2. PWM to Analog Dimming in Boost Configuration

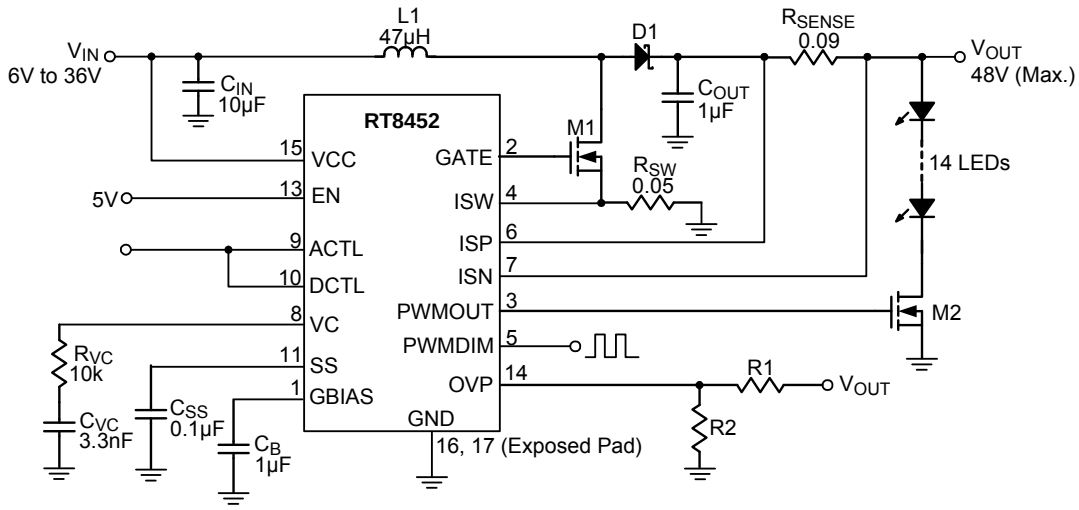


Figure 3. True PWM Dimming in Boost Configuration

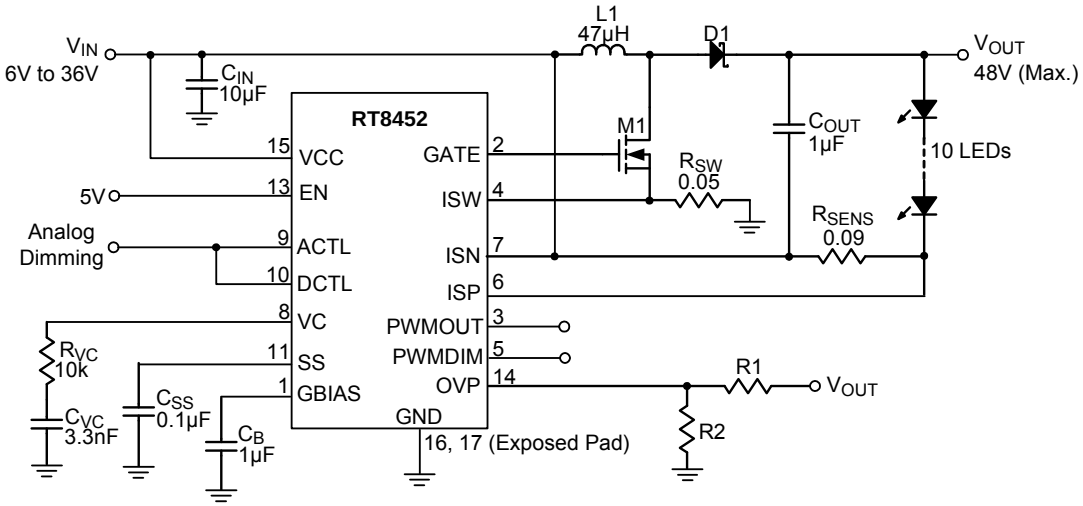


Figure 4. Analog Dimming in Buck-Boost Configuration

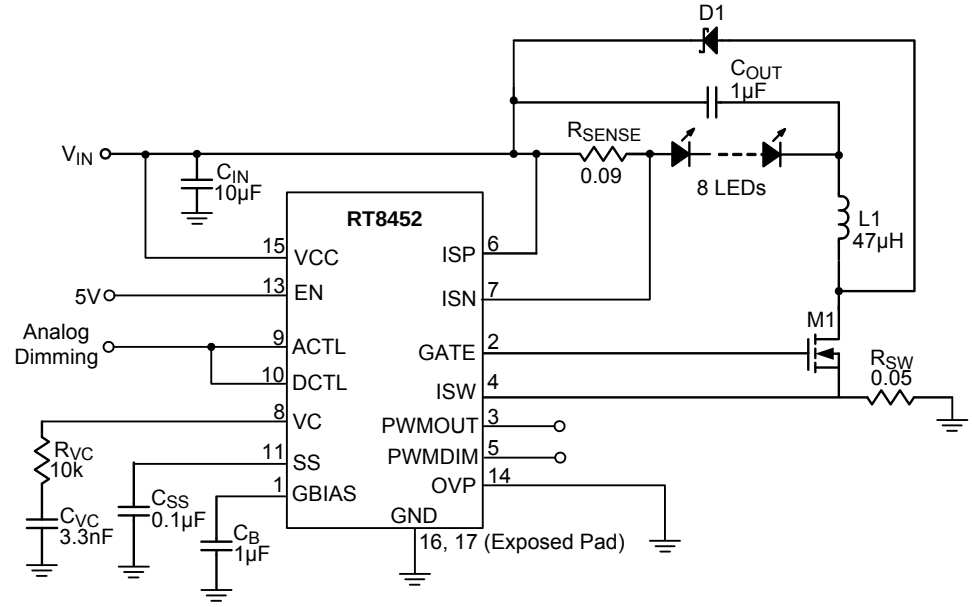
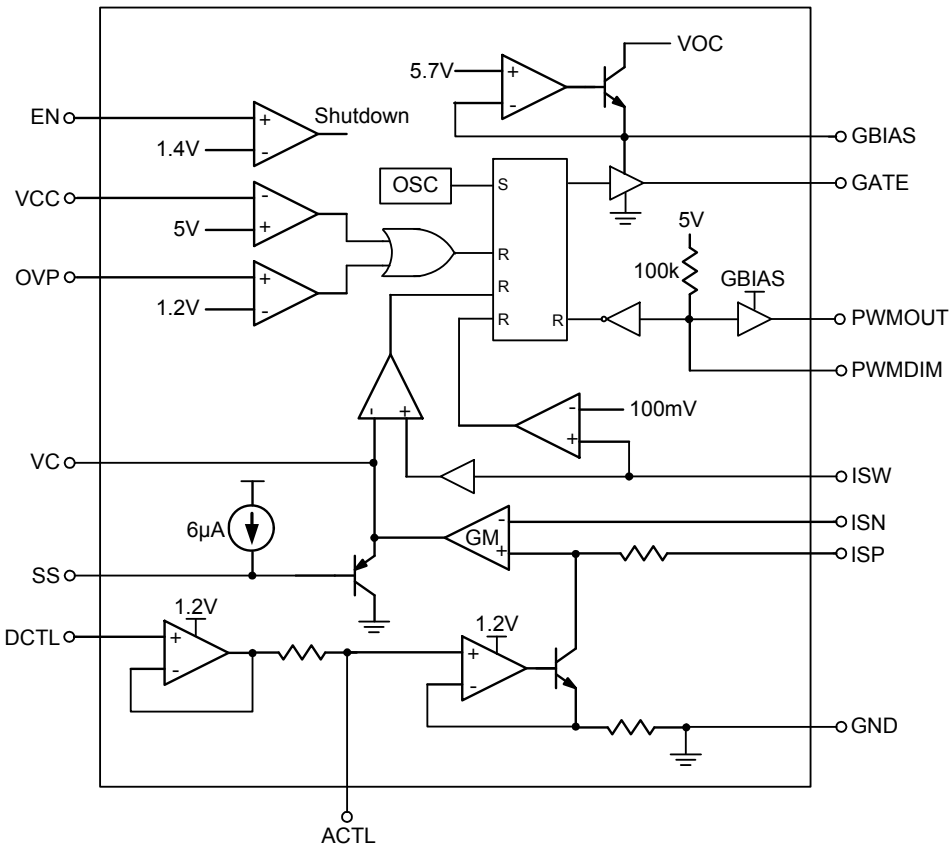


Figure 5. Analog Dimming in Buck Configuration

Functional Pin Description

Pin No.		Pin Name	Pin Function
SOP-16	WQFN-16L 3x3		
1	1	GBIAS	Internal gate driver bias. A good bypass capacitor is required.
2	2	GATE	External MOSFET switch gate driver output.
3	3	PWMOUT	Output pin for the PWM dimming fet driver.
4	4	ISW	External MOSFET switch current sense. Connect the current sense resistor between external N-MOSFET switch and the ground.
5	5	PWMDIM	Control input pin for the PWM dimming FET driver.
6	6	ISP	LED current sense amplifier positive input.
7	7	ISN	LED current sense amplifier negative input. Voltage threshold between ISP and ISN is 190mV.
8	8	VC	PWM control loop compensation.
9	9	ACTL	Analog dimming control. The effective programming voltage range of the pin is between 0.2V and 1.2V.
10	10	DCTL	By adding a 0.47μF filtering capacitor on ACTL pin, the PWM dimming signal on DCTL pin can be averaged and converted into analog dimming signal on the ACTL pin.
11	11	SS	Soft-start. A capacitor of at least 10nF is required for proper soft start.
12	12	NC	No internal connection.
13	13	EN	Chip enable (active high). When this pin voltage is low, the chip is in shutdown mode.
14	14	OVP	Over voltage protection. The PWM converter turns off when the voltage of the pin goes to higher than 1.2V.
15	15	VCC	Power supply pin of the chip. For good bypass, a low ESR capacitor is required.
16	16 17 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.

Functional Block Diagram



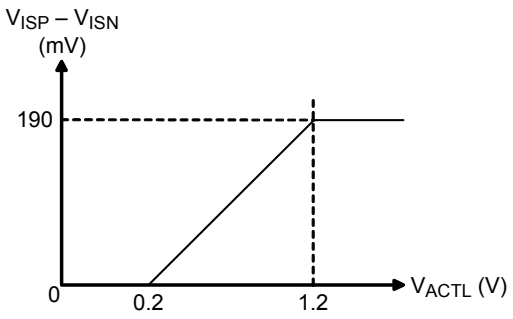


Figure 6

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VCC ---------- 38V
- GBIAS, GATE, PWMDIM, PWMOUT ---------- 10V
- ISW ---------- 1V
- ISP, ISN ---------- 54V
- DCTL, ACTL, OVP Pin Voltage ---------- 8V (Note 6)
- EN Pin Voltage ---------- 20V
- Power Dissipation, P_D @ T_A = 25°C
  - SOP-16 ---------- 1.0W
  - WQFN-16L 3x3 ---------- 1.4W
- Package Thermal Resistance (Note 2)
  - SOP-16, θ_{JA} ---------- 95°C/W
  - WQFN-16L 3x3, θ_{JA} ---------- 68°C/W
  - WQFN-16L 3x3, θ_{JC} ---------- 7.5°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ---------- 2kV
  - MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Supply Input Voltage Range, VCC ---------- 6V to 36V
- Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{CC} = 24V, No Load on any Output, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Overall							
Supply Current		I_{VCC}	VC ≤ 0.4V (Switching off)	--	6	7.2	mA
Shutdown Current		I_{SHDN}	V_{EN} ≤ 0.7V	--	12	--	μA
EN Threshold Voltage	Logic-High	V_{IH}		2	--	--	V
	Logic-Low	V_{IL}		--	--	0.5	
EN Input Current			V_{EN} ≤ 3V	--	--	1.2	μA
Current Sense Amplifier							
Input Threshold (V_{ISP} – V_{ISN})			12V ≤ common mode ≤ 36V	180	190	200	mV
ISP / ISN Input Current		I_{ISP} / I_{ISN}	6V ≤ V_{ISP} = V_{ISN} ≤ 48V	--	140	--	μA
VC Output Current		I_{VC}	V_{ISP} – V_{ISN} = 190mV, 0.5V ≤ V_C ≤ 2.4V	--	±20	--	μA
VC Threshold for PWM Switch Off				--	0.7	--	V

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
LED Dimming							
Analog Dimming ACTL Pin Input Current		I_{ACTL}	V_{ACTL} = 1.2V	–	1	--	μA
			V_{ACTL} = 0.2V	–	10	--	
LED Current Off Threshold at ACTL		V_{ACTL_Off}		–	0.3	--	V
DCTL Input Current		I_{DCTL}	0.3V ≤ V_{DCTL} ≤ 6V	–	--	0.5	μA
PWM Control							
Switching Frequency		f_{SW}		280	350	420	kHz
Minimum Off Time (Note 5)				–	250	--	ns
Switch Gate Driver							
GBIAS Voltage		V_{GBIAS}	I_{GBIAS} = 20mA	–	8.5	--	V
Gate Voltage High		V_{Gate_H}	I_{Gate} = –50mA	–	7.2	--	V
			I_{Gate} = –100μA	–	7.8	--	
Gate Voltage Low		V_{Gate_L}	I_{Gate} = 50mA	–	0.25	--	V
			I_{Gate} = 100μA	–	0.1	--	
GATE Drive Rise and Fall Time			1nF Load at GATE	–	15	--	ns
PWM Switch Current Limit Threshold		I_{SW_LIM}		–	110	--	mV
PWM Dimming Gate Driver							
PWMDIM Threshold Voltage	Logic-High	V_{PWMDIM_H}		2	--	--	V
	Logic-Low	V_{PWMDIM_L}		–	--	0.5	
PWMOUT Output Voltage		V_{PWMOUT_H}	I_{PWMOUT} = 1mA	–	7.5	--	V
		V_{PWMOUT_L}	I_{PWMOUT} = –100μA	–	0.45	--	
PWMOUT Drive Rise and Fall Time			1nF Load at PWMOUT	–	40	--	ns
OVP and Soft Start							
OVP Threshold		V_{OVP_th}		–	1.18	--	V
OVP Input Current		I_{OVP}	0.7V ≤ V_{OVP} ≤ 1.5V	–	--	0.1	μA
Soft-Start Pin Current		I_{SS}	V_{SS} ≤ 2V	–	6	--	μA
Thermal Shutdown Protection		T_{SD}		–	145	--	°C
Thermal Shutdown Hysteresis		ΔT_{SD}		–	10	--	

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. θ_{JC} is measured at the exposed pad of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

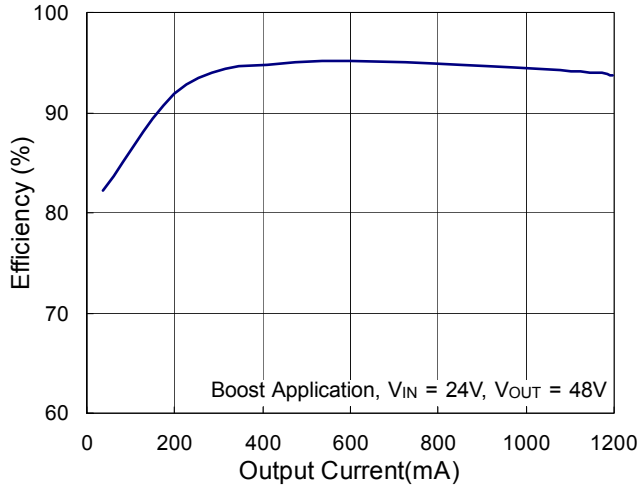
Note 4. The device is not guaranteed to function outside its operating conditions.

Note 5. When the natural maximum duty cycle of 350kHz switching frequency is reached, the switching cycle will be skipped (not reset) as the operating condition requires to effectively stretch and achieve higher on cycle than the natural maximum duty cycle set by the 350kHz switching frequency.

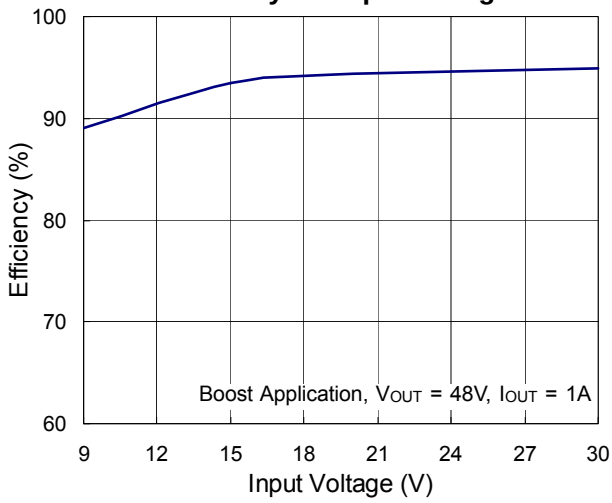
Note 6. If connected with a 20kΩ serial resistor, ACTL and DCTL can go up to 36V.

Typical Operating Characteristics

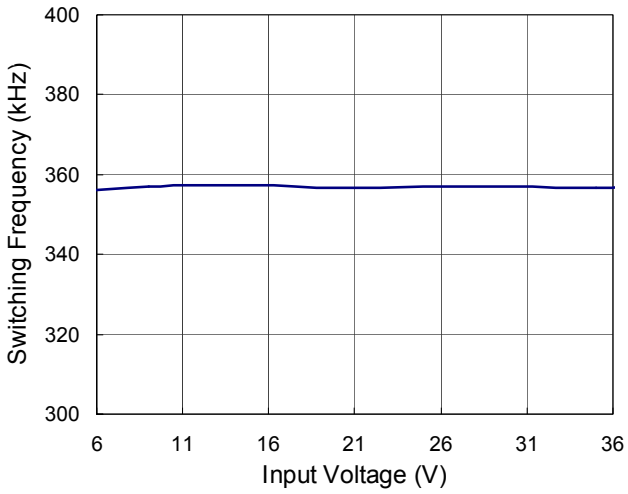
Efficiency vs. Output Current



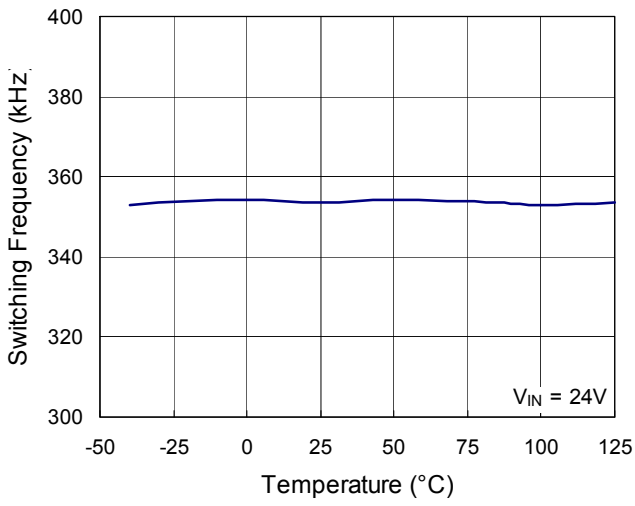
Efficiency vs. Input Voltage



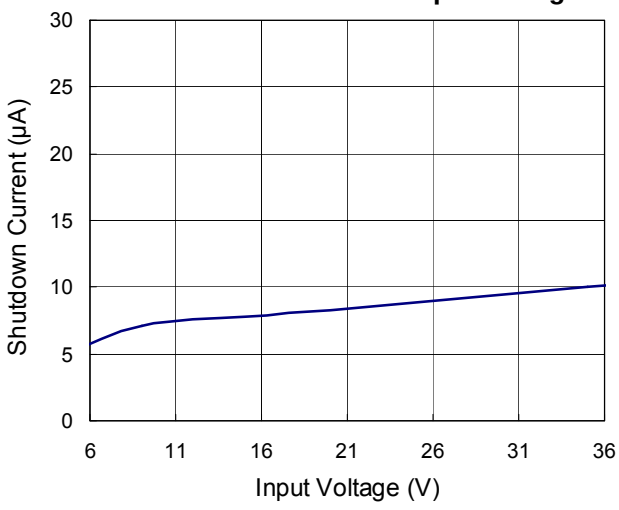
Switching Frequency vs. Input Voltage



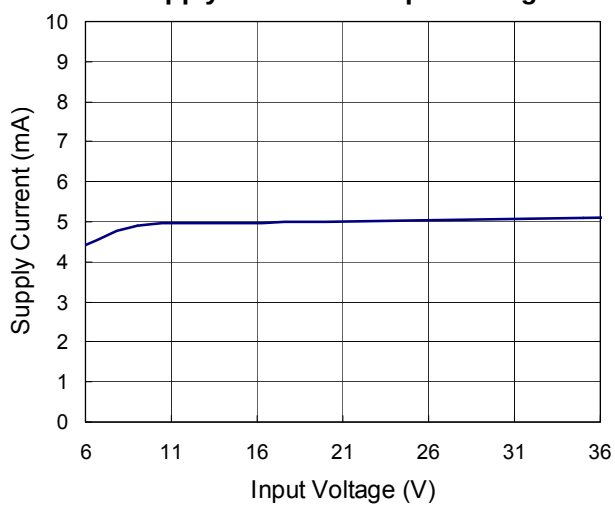
Switching Frequency vs. Temperature



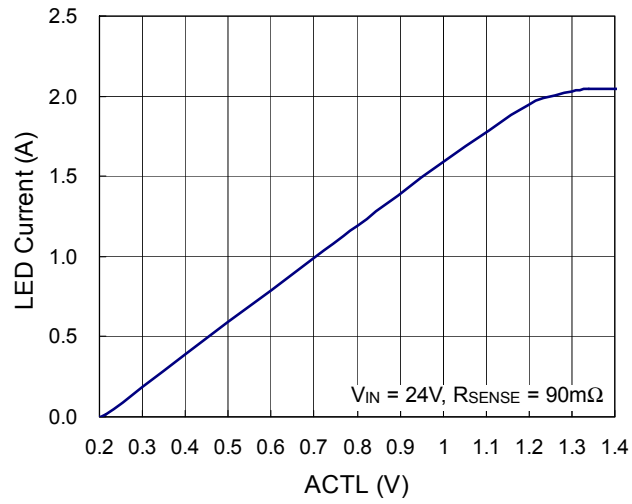
Shutdown Current vs. Input Voltage



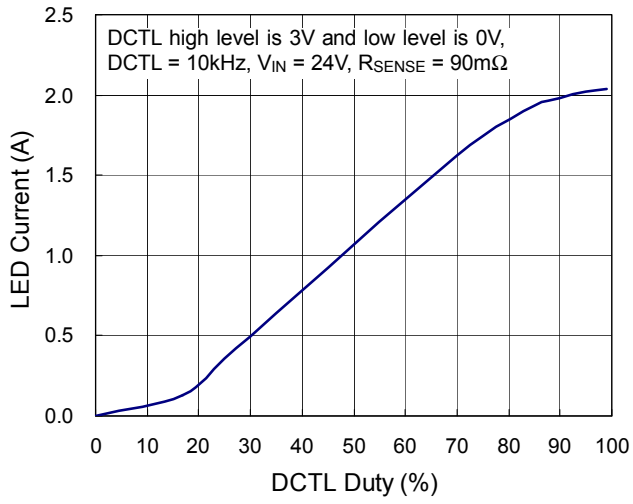
Supply Current vs. Input Voltage



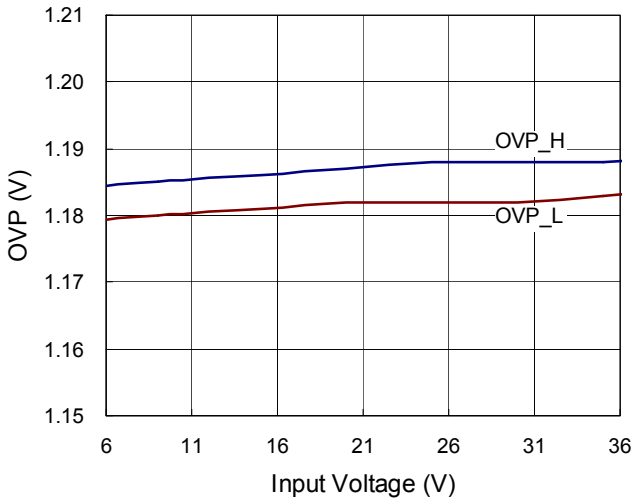
LED Current vs. ACTL



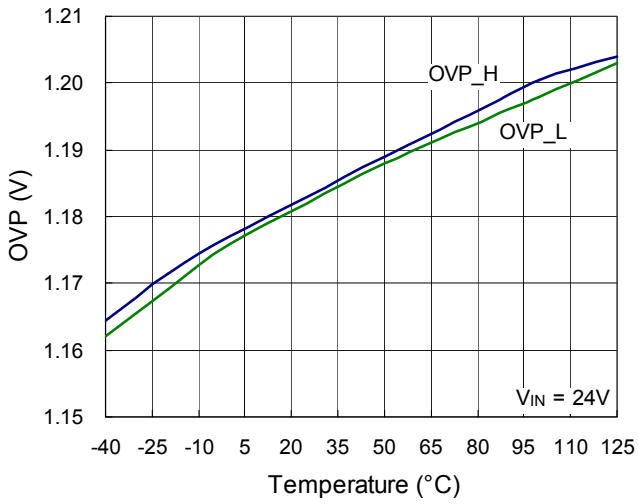
LED Current vs. DCTL Duty



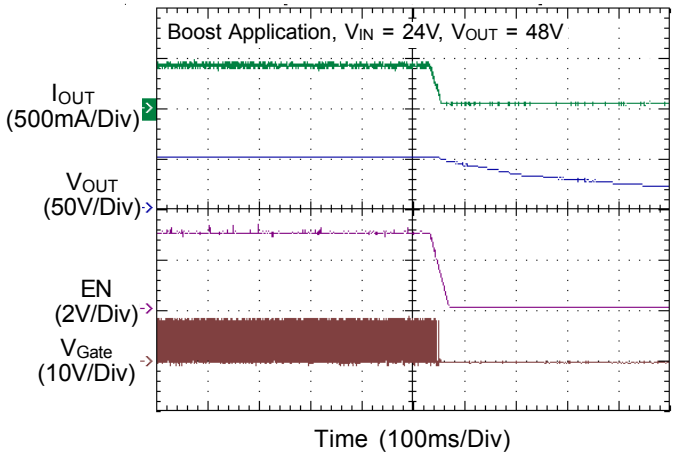
OVP vs. Input Voltage



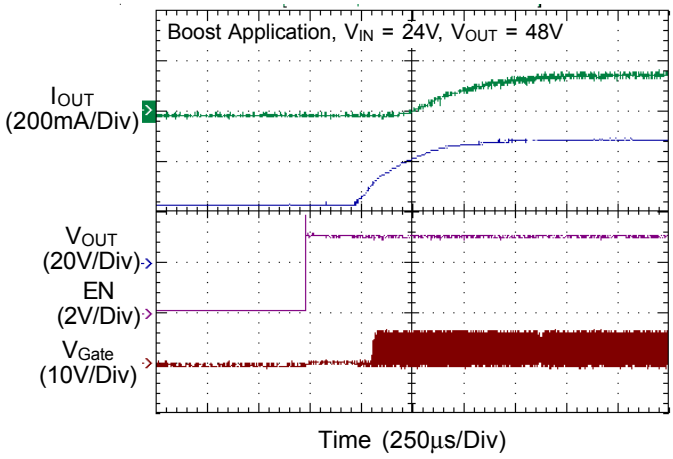
OVP vs. Temperature



Power Off from EN



Power On from EN



Applications Information

The RT8452 is a current mode PWM controller designed to drive an external MOSFET for high current LED applications. The LED current can be programmed by an external resistor. The input voltage range of the RT8452 can be up to 36V and the output voltage can be up to 48V. The RT8452 provides analog and PWM dimming to achieve LED current control.

GBIAS Regulator and Bypass Capacitor

The GBIAS pin requires a capacitor for stable operation and to store the charge for the large GATE switching currents. Choose a 10V rated low ESR, X7R or X5R ceramic capacitor for best performance. The value of a 1μF capacitor will be adequate for many applications.

Place the capacitor close to the IC to minimize the trace length to the GBIAS pin and also to the IC ground. An internal current limit on the GBIAS output protects the RT8452 from excessive on-chip power dissipation.

The GBIAS pin has its own under-voltage disable (UVLO) set to 4.3V(typical) to protect the external FETs from excessive power dissipation caused by not being fully enhanced. If the input voltage, VIN, will not exceed 8V, then the GBIAS pin should be connected to the input supply. Be aware if GBIAS supply is used to drive extra circuits besides RT8452, typically the extra GBIAS load should be limited to less than 10mA.

Loop Compensation

The RT8452 uses an internal error amplifier whose compensation pin (VC) allowing the loop response optimized for specific application. The external inductor, output capacitor and the compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor at VC are selected to optimize control loop response and stability. For typical LED applications, a 3.3nF compensation capacitor at VC is adequate, and a series resistor should always be used to increase the slew rate on the VC pin to maintain tighter regulation of LED current during fast transients on the input supply to the converter an external resistor in series with a capacitor is connected from the VC pin to GND to provide a pole and a zero for proper loop compensation. The typical compensation forthe RT8452 is 10k and 3.3nF.

Soft-Start

The soft-start of the RT8452 can be achieved by connecting a capacitor from SS pin to GND. The built-in soft-start circuit reduces the start-up current spike and output voltage overshoot. The soft-start time is determined by the external capacitor charged by an internal 6μA constant charging current. The SS pin directly limits the rate of voltage rise on the VC pin, which in turn limits the peak switch current.

The soft-start interval is set by the soft-start capacitor selection according to the equation :

$$T_{SS} = C_{SS} \times \frac{2.4V}{6\mu A}$$

A typical value for the soft-start capacitor is 0.1μF. The soft-start capacitor is discharged when EN/UVLO falls below its threshold, during an over-temperature event or during an GBIAS under-voltage event.

LED current Setting

The LED current is programmed by placing an appropriate value current sense resistor between the ISP and ISN pins. Typically, sensing of the current should be done at the top of the LED string. The ACTL pin should be tied to a voltage higher than 1.2V to get the full-scale 190mV (typical) threshold across the sense resistor. The ACTL pin can also be used to dim the LED current to zero, although relative accuracy decreases with the decreasing voltage sense threshold. When the ACTL pin voltage is less than 1.2V, the LED current is :

$$I_{LED} = \frac{(V_{ACTL} - 0.2) \times 0.19}{R_{SENSE}}$$

Where,

R_{SENSE} is the resister between ISP and ISN.

When the voltage of ACTL is higher than 1.2V, the LED current is regulated to :

$$I_{LED(MAX)} = \frac{190mV}{R_{SENSE}}$$

The ACTL pin can also be used in conjunction with a thermistor to provide over temperature protection for the LED load, or with a resistor divider to V_{IN} to reduce output power and switching current when V_{IN} is low. The presence of a time varying differential voltage signal (ripple) across ISP and ISN at the switching frequency is expected.

The amplitude of this signal is increased by high LED load current, low switching frequency and/or a smaller value output filter capacitor. The compensation capacitor on the VC pin filters the signal so the average difference between ISP and ISN is regulated on the user-programmed value.

Dimming Control

For LED applications where a wide dimming range is required, two competing methods are available : analog/ digital dimming and True PWM dimming. The easiest method is to simply vary the DC current through the LED by analog dimming.

The other better dimming method is the True PWM dimming, which switches the LED on and off by different duty cycle to control the average LED current.

The True PWM dimming offers several advantages over analog dimming and is much preferred by LED manufacturers. One advantage is the chromaticity of the LEDs remains unchanged in this scheme since the LED current is either zero or at the programmed current. Another profit of True PWM dimming over analog/digital dimming is that a wider dimming range is possible. True PWM method modulate the current source between zero and full current to achieve a precisely programmed average current. For best current accuracy, the minimum True PWM low or high time should be at least 18μS.

The maximum True PWM period is determined by the system and suggested shorter than 9ms. The maximum True PWM dimming ratio (PWM_{RATIO}) can be calculated from the maximum True PWM period (t_{MAX}) and the minimum True PWM pulse width (t_{MIN}) as follows :

$$PWM_{RATIO} = \frac{t_{MAX}}{t_{MIN}}$$

t_{MAX} = 9ms, t_{MIN} = 18μs (f_{SW} = 350kHz)

PWM_{RATIO} = 9ms / 12μs = 500 : 1

The RT8452 features both analog and digital dimming control. Analog dimming is linearly controlled by an external voltage ($0.2V < V_{ACTL} < 1.2V$). With an on chip output clamping amplifier and a resistor, digital dimming signal fed at DCTL pin can be easily low-pass filtered to an analog dimming signal with one external capacitor from ACTL pin to GND for noise-free digital dimming. A high contrast ratio digital dimming can also be achieved by driving ACTL pin with a digital signal from 100Hz to10kHz.

Output Over Voltage Setting

The RT8452 is equipped with over voltage protection (OVP) function. When the voltage at OVP pin exceeds a threshold of approximately1.18V, the power switch is turned off. The power switch can be turned on again once the voltage at OVP pin drops below 1.18V. For the Boost and Buck-Boost application, the output voltage could be clamped at a certain voltage level. The OVP voltage can be set by the following equation :

$$V_{OUT,\,OVP} = 1.18 \times \left(1 + \frac{R1}{R2}\right)$$

Where,

R1 and R2 are the voltage divider from Vout to GND with the divider center node connected to OVP pin.

ISW Sense Resistor Selection

The resistor, R_{SW}, between the source of the external N-MOSFET and GND should be selected to provide adequate switch current to drive the application without exceeding the 110mV (typical) current limit threshold on the ISW pin of RT8452. For real applications, select a resistor that gives a switch current at least 30% greater than the required LED current.

For Buck application, select a resistor according to :

$$R_{SW,\,Buck} = \left(\frac{0.08V}{I_{OUT}}\right)$$

For Buck-Boost application, select a resistor according to :

$$R_{SW,\,Buck\text{-}Boost} = \left(\frac{V_{IN} \times 0.08V}{(V_{IN} + V_{OUT}) \times I_{OUT}}\right)$$

For Boost application, select a resistor according to :

$$R_{SW,\,Boost} = \left(\frac{V_{IN} \times 0.08V}{V_{OUT} \times I_{OUT}}\right)$$

The placement of R_{SW} should be close to the source of the N-MOSFET and GND of the RT8452. The ISW pin input to RT8452 should be a Kelvin connection to the positive terminal of R_{SW}.

Over Temperature Protection

The RT8452 has over temperature protection (OTP) function to prevent the excessive power dissipation from overheating. The OTP function will shut down switching operation when the die junction temperature exceeds 150°C. The chip will automatically start to switch again when the die junction temperature cools off.

Inductor Selection

The inductor used with the RT8452 should have a saturation current rating appropriate to the maximum switch current selected with the RSW resistor. Choose an inductor value based on operating frequency, input and output voltage to provide a current mode ramp on ISW pin during the switch on-time of approximately 20mV magnitude. The following equations are useful to estimate the inductor value.

For Buck application :

$$L_{Buck} = \frac{R_{SW} \times V_{OUT} \times (V_{IN} - V_{OUT})}{0.02 \times V_{IN} \times f_{SW}}$$

For Boost application

$$L_{Boost} = \frac{R_{SW} \times V_{IN} \times (V_{OUT} - V_{IN})}{0.02 \times V_{OUT} \times f_{SW}}$$

For Buck-Boost application

$$L_{Buck-Boost} = \frac{R_{SW} \times V_{IN} \times V_{OUT}}{0.02 \times (V_{IN} + V_{OUT}) \times f_{SW}}$$

Power MOSFET Selection

For applications operating at high input or output voltages, the power N-MOS FET switch is typically chosen for drain voltage VDS rating and low gate charge. Consideration of switch on-resistance, $R_{DS(ON)}$, is usually secondary because switching losses dominate power loss. The GBIAS regulator on the RT8452 has a fixed current limit to protect the IC from excessive power dissipation at high VIN, so the N-MOSFET should be chosen so that the product of Qg at 5V and switching frequency does not exceed the GBIAS current limit.

Moreover, to obtain better conversion efficiency, GATE high level must be higher than the gate threshold voltage Vgs(th) of the power N-MOSFET. If GATE high level is lower, an external totem pole circuit has to be added.

Schottky Diode Selection

The Schottky diode, with their low forward voltage drop and fast switching speed, is necessary for the RT8452 applications. In addition, power dissipation, reverse voltage rating and pulsating peak current are the important parameters for the Schottky diode selection. Choose a suitable Schottky diode whose reverse voltage rating is greater than maximum output voltage. The diode's average current rating must exceed the average output current. The diode conducts current only when the power switch is turned off (typically less than 50% duty cycle). If using the PWM feature for dimming, it is important to consider diode leakage, which increases with the temperature, from the output during the PWM low interval. Therefore, choose the Schottky diode with sufficiently low leakage current.

Capacitor Selection

The input capacitor reduces current spikes from the input supply and minimizes noise injection to the converter. For most the RT8452 applications, a 10µF ceramic capacitor is sufficient. A value higher or lower may be used depending on the noise level from the input supply and the input current to the converter.

In Boost application, the output capacitor is typically a ceramic capacitor and is selected based on the output voltage ripple requirements. The minimum value of the output capacitor C_{OUT} is approximately given by the following equation :

$$C_{OUT} = \frac{I_{OUT} \times V_{OUT}}{V_{IN} \times V_{RIPPLE} \times f_{SW}}$$

For LED applications, the equivalent resistance of the LED is typically low and the output filter capacitor should be sized to attenuate the current ripple. Use of X7R type ceramic capacitors is recommended. Lower operating frequencies will require proportionately higher capacitor values.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a WQFN-16L 3x3 package, the thermal resistance, θ_{JA}, is 68°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. For a SOP-16 package, the thermal resistance, θ_{JA}, is 95°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (68°C/W) =1.471W for a WQFN-16L 3x3 package.

$P_{D(MAX)}$ = (125°C – 25°C) / (95°C/W) =1.053W for a SOP-16 package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 6 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

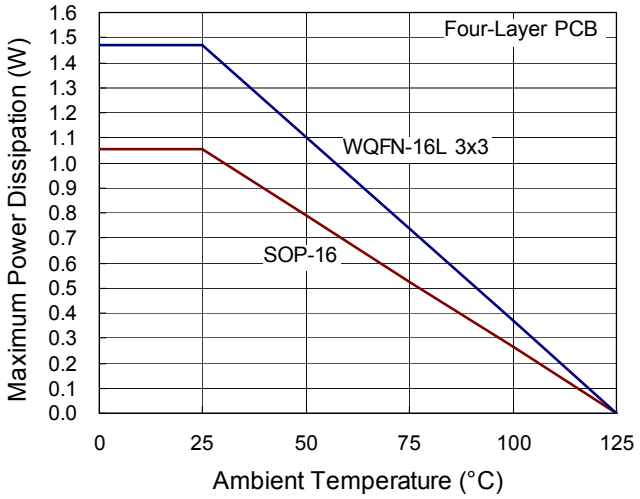


Figure 7. Derating Curve of Maximum Power Dissipation

Layout Consideration

PCB layout is very important to design power switching converter circuits. Some recommended layout guide lines are suggested as follows :

- The power components L1, D1, C_{IN}, M1 and C_{OUT} must be placed as close to each other as possible to reduce the ac current loop area. The PCB trace between power components must be as short and wide as possible due to large current flow through these traces during operation.
- The input capacitors C_{VCC} must be placed as close to VCC pin as possible.
- Place the compensation components to VC pin as close as possible to avoid noise pick up.
- Connect GND pin ane Exposed Pad to a large ground plane for maximum power dissipation and noise reduction.

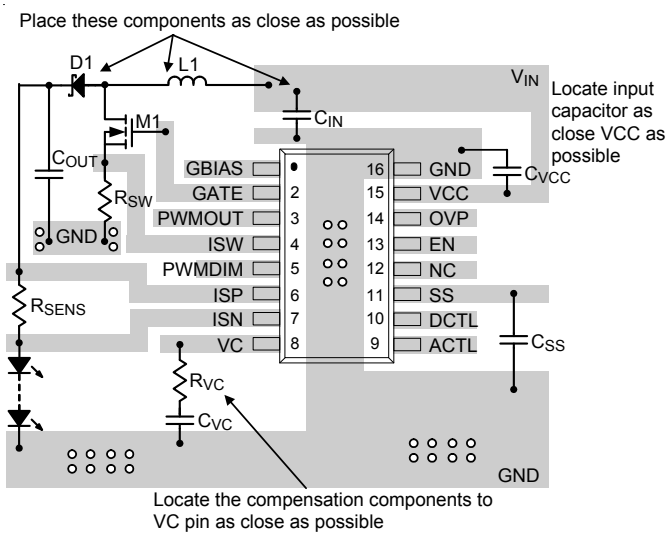
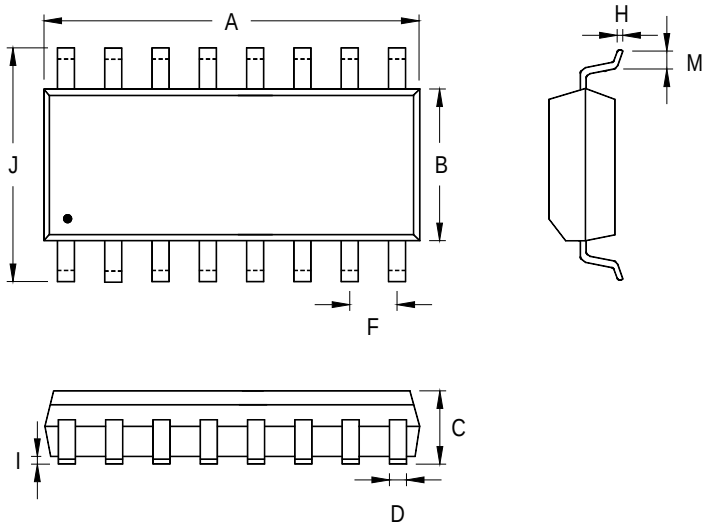


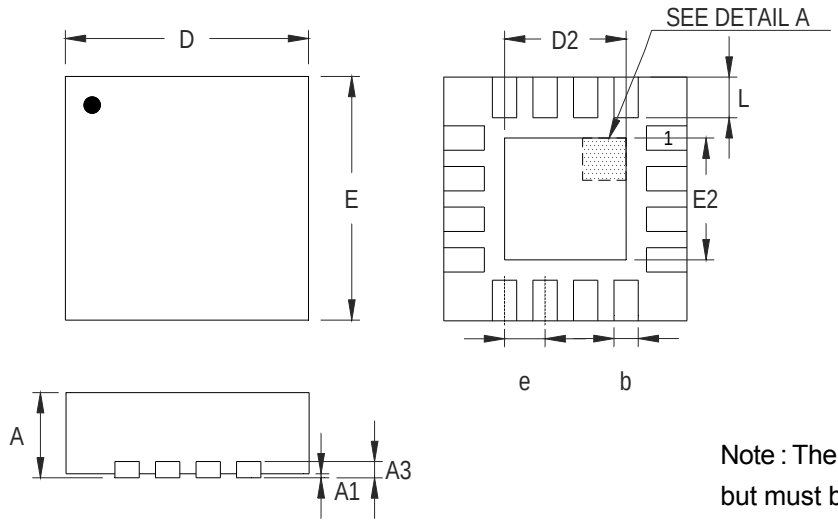
Figure 8. PCB Layout Guide

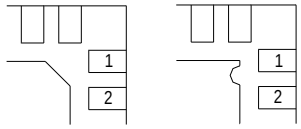
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	9.804	10.008	0.386	0.394
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.178	0.254	0.007	0.010
I	0.102	0.254	0.004	0.010
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050

16-Lead SOP Plastic Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.180	0.300	0.007	0.012
D	2.950	3.050	0.116	0.120
D2	1.300	1.750	0.051	0.069
E	2.950	3.050	0.116	0.120
E2	1.300	1.750	0.051	0.069
e	0.500		0.020	
L	0.350	0.450	0.014	0.018

W-Type 16L QFN 3x3 Package

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