

MOSFET – P-Channel, POWERTRENCH®

-30 V, -20 A, 10 mΩ

FDMC6679AZ

General Description

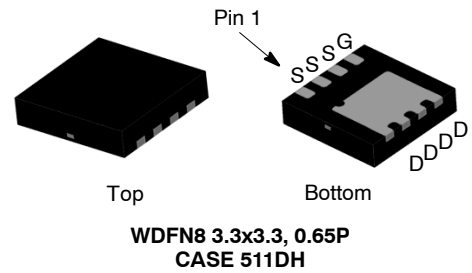
The FDMC6679AZ has been designed to minimize losses in load switch applications. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ and ESD protection.

Features

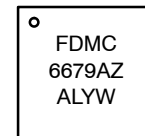
- Max $r_{DS(on)}$ = 10 mΩ at $V_{GS} = -10$ V, $I_D = -11.5$ A
- Max $r_{DS(on)}$ = 18 mΩ at $V_{GS} = -4.5$ V, $I_D = -8.5$ A
- HBM ESD Protection Level of 8 kV Typical (Note 3)
- Extended V_{GSS} range (-25 V) for Battery Applications
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability
- This Device is Pb-Free and Halide Free

Applications

- Load Switch in Notebook and Server
- Notebook Battery Pack Power Management

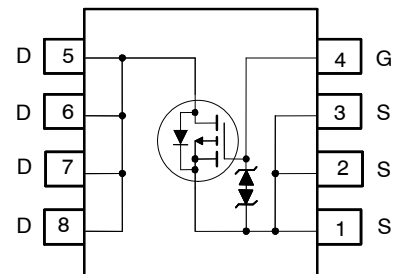


MARKING DIAGRAM



FDMC6679AZ = Specific Device Code
 A = Assembly Location
 L = Wafer Lot Number
 YW = Assembly Start Week

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

FDMC6679AZ

MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

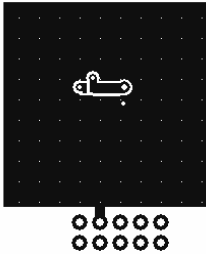
Symbol	Parameter	Rating	Unit		
V_{DS}	Drain to Source Voltage	-30	V		
V_{GS}	Gate to Source Voltage	± 25	V		
I_D	Drain Current	Continuous	$T_C = 25^\circ\text{C}$	A	
		Continuous (Note 1a)	$T_A = 25^\circ\text{C}$		-11.5
		Pulsed			-32
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	41	W	
	Power Dissipation (Note 1a)	$T_A = 25^\circ\text{C}$	2.3		
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to + 150	$^\circ\text{C}$		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $53^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0%.
- The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

FDMC6679AZ

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = -250 μA, V _{GS} = 0 V	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = -250 μA, Referenced to 25°C		29		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24 V, V _{GS} = 0 V			-1	μA
		V _{DS} = -24 V, V _{GS} = 0 V, T _J = 125°C			-100	
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±25 V, V _{DS} = 0 V			±10	μA

ON CHARACTERISTICS

V _{GS(th)}	Gate to Source Threshold Voltage	V _{GS} = V _{DS} , I _D = -250 μA	-1.0	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = -250 μA, Referenced to 25°C		-7		mV/°C
r _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = -10 V, I _D = -11.5 A		8.6	10	mΩ
		V _{GS} = -4.5 V, I _D = -8.5 A		12	18	
		V _{GS} = -10 V, I _D = -11.5 A, T _J = 125°C		12	15	
g _{FS}	Forward Transconductance	V _{DS} = -5 V, I _D = -11.5 A		46		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = -15 V, V _{GS} = 0 V, f = 1 MHz		2985	3970	pF
C _{oss}	Output Capacitance			570	755	pF
C _{rss}	Reverse Transfer Capacitance			500	750	pF

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = -15 V, I _D = -11.5 A, V _{GS} = -10 V, R _{GEN} = 6 Ω		12	21	ns
t _r	Rise Time			14	25	ns
t _{d(off)}	Turn-Off Delay Time			63	100	ns
t _f	Fall Time			46	73	ns
Q _g	Total Gate Charge	V _{GS} = 0 V to -10 V, V _{DD} = -15 V, I _D = -11.5 A		65	91	nC
		V _{GS} = 0 V to -5 V, V _{DD} = -15 V, I _D = -11.5 A		37	52	nC
Q _{gs}	Gate to Source Charge	V _{DD} = -15 V, I _D = -11.5 A		8.7		nC
Q _{gd}	Gate to Drain "Miller" Charge			17		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = -11.5 A (Note 2)		0.83	1.30	V
		V _{GS} = 0 V, I _S = -1.6 A (Note 2)		0.71	1.20	
t _{rr}	Reverse Recovery Time	I _F = -11.5 A, di/dt = 100 A/μs		31	49	ns
Q _{rr}	Reverse Recovery Charge			16	28	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

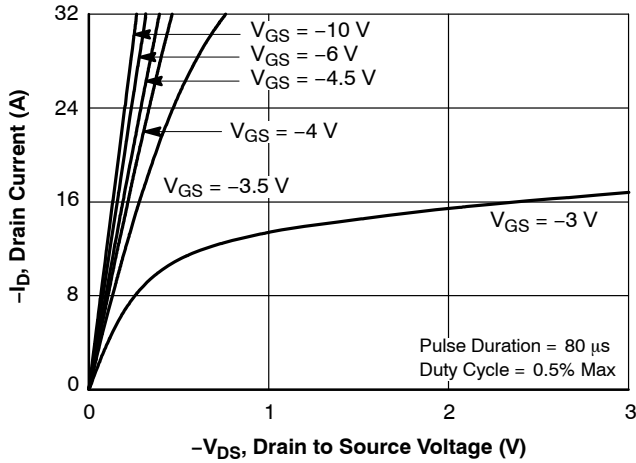


Figure 1. On Region Characteristics

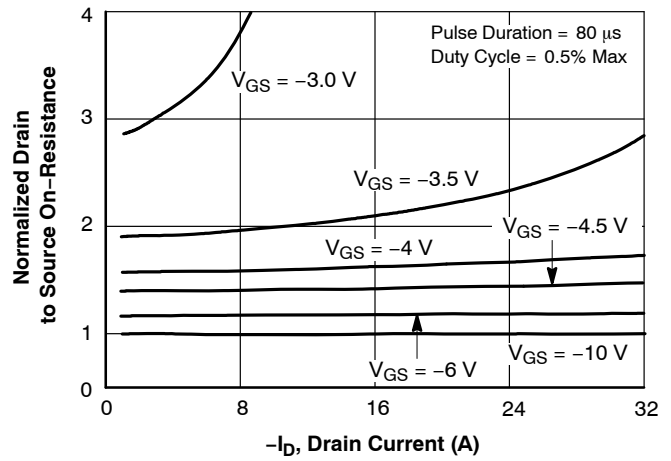


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

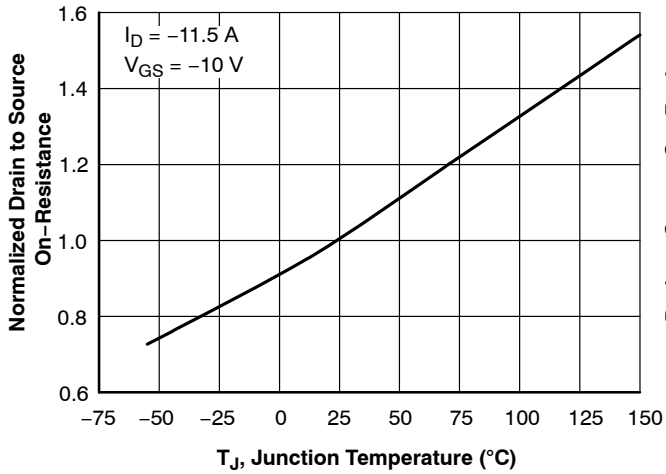


Figure 3. Normalized On Resistance vs. Junction Temperature

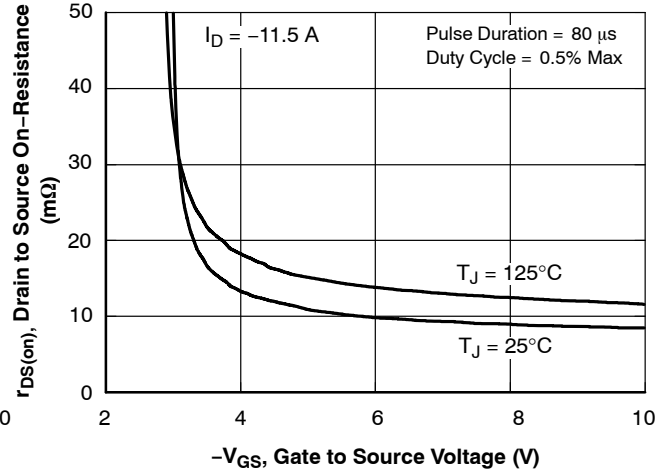


Figure 4. On-Resistance vs. Gate to Source Voltage

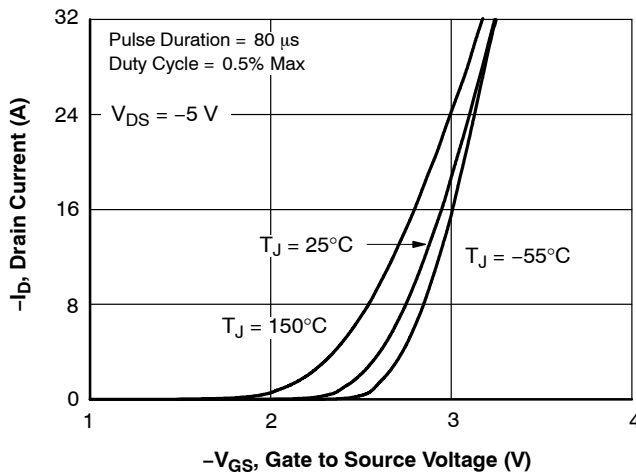


Figure 5. Transfer Characteristics

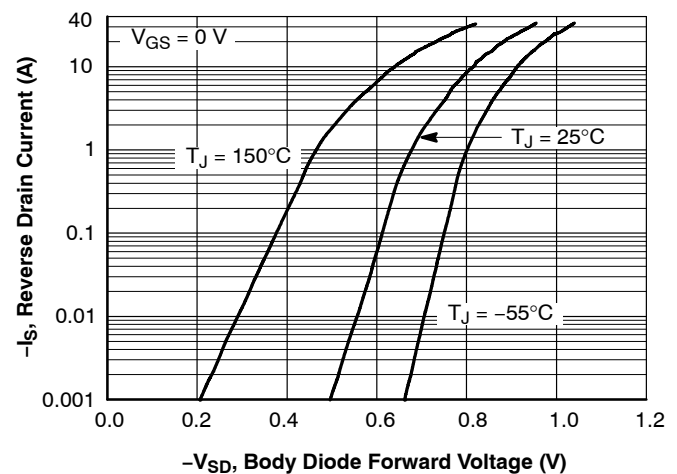


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

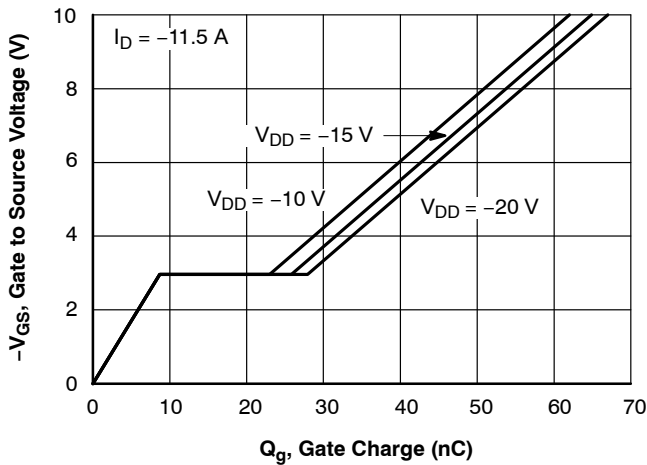


Figure 7. Gate Charge Characteristics

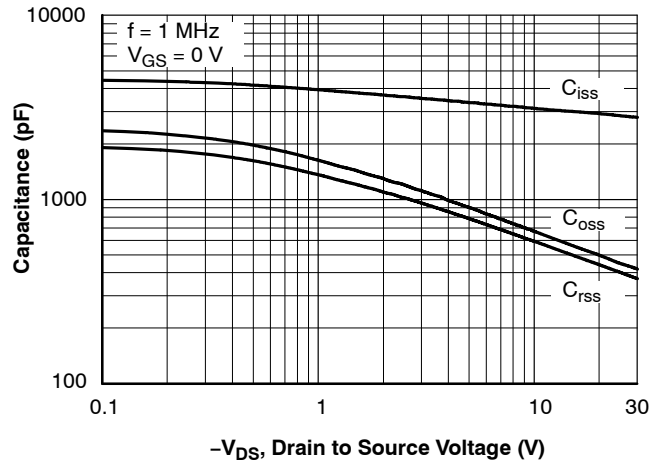


Figure 8. Capacitance vs. Drain to Source Voltage

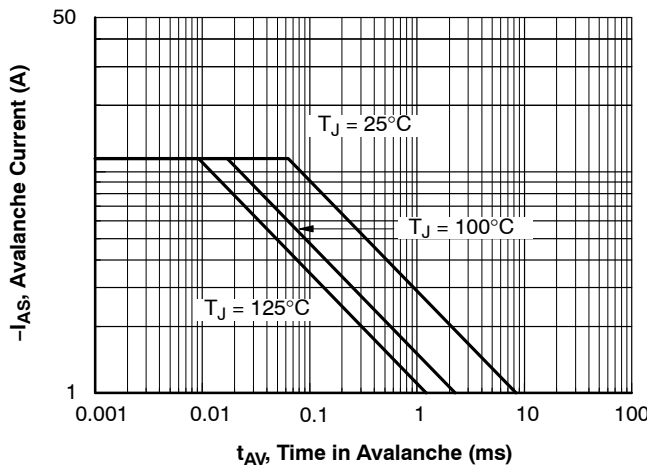


Figure 9. Unclamped Inductive Switching Capability

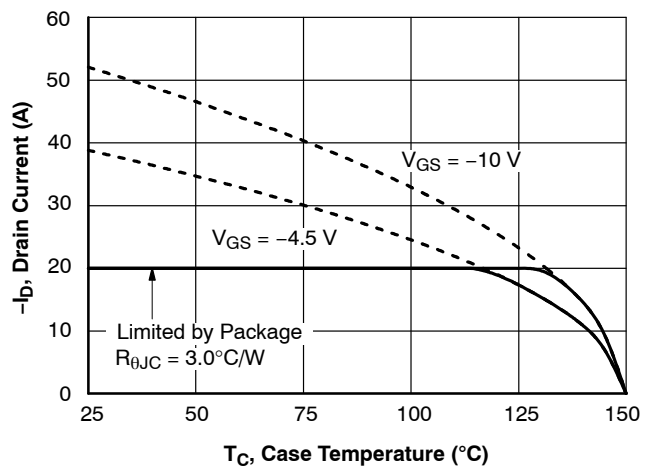


Figure 10. Maximum Continuous Drain Current vs Case Temperature

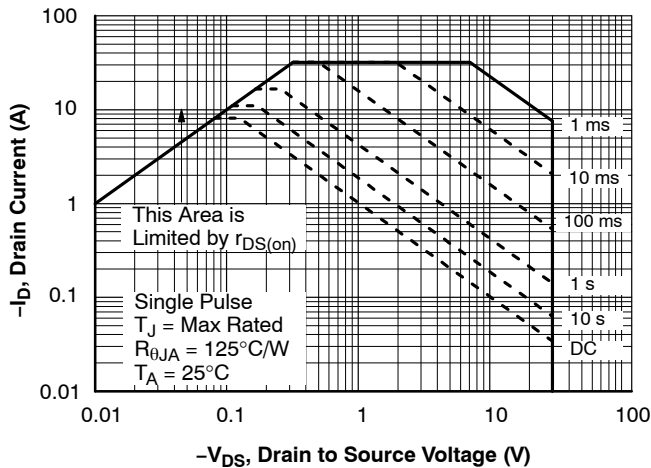


Figure 11. Forward Bias Safe Operating Area

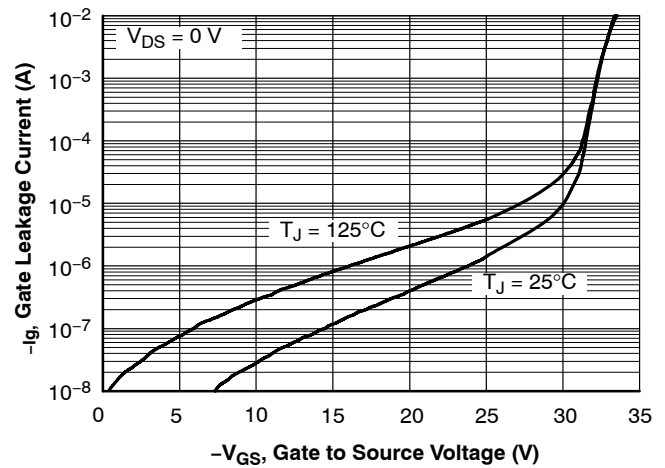


Figure 12. I_{gss} vs. V_{gss}

FDMC6679AZ

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

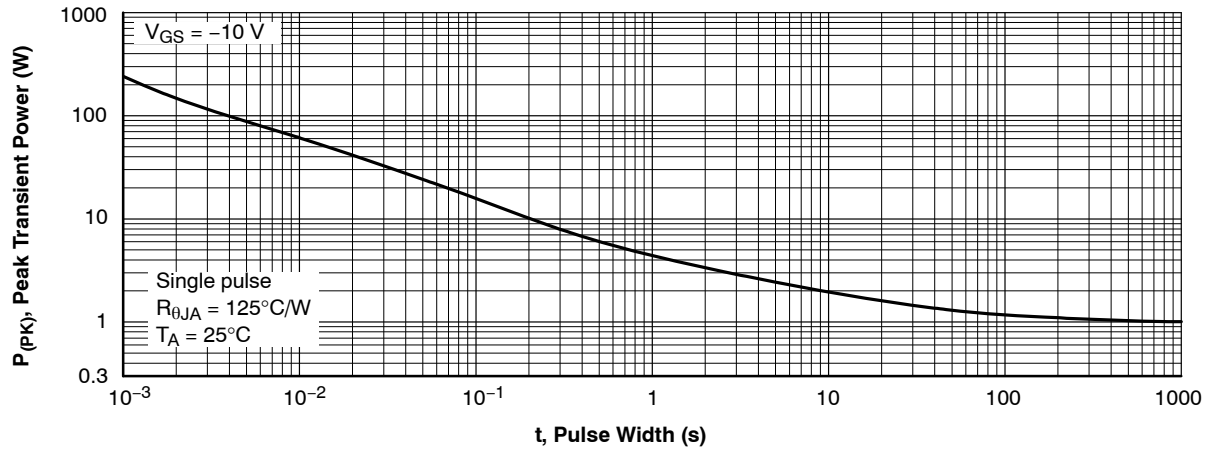


Figure 13. Single Pulse Maximum Power Dissipation

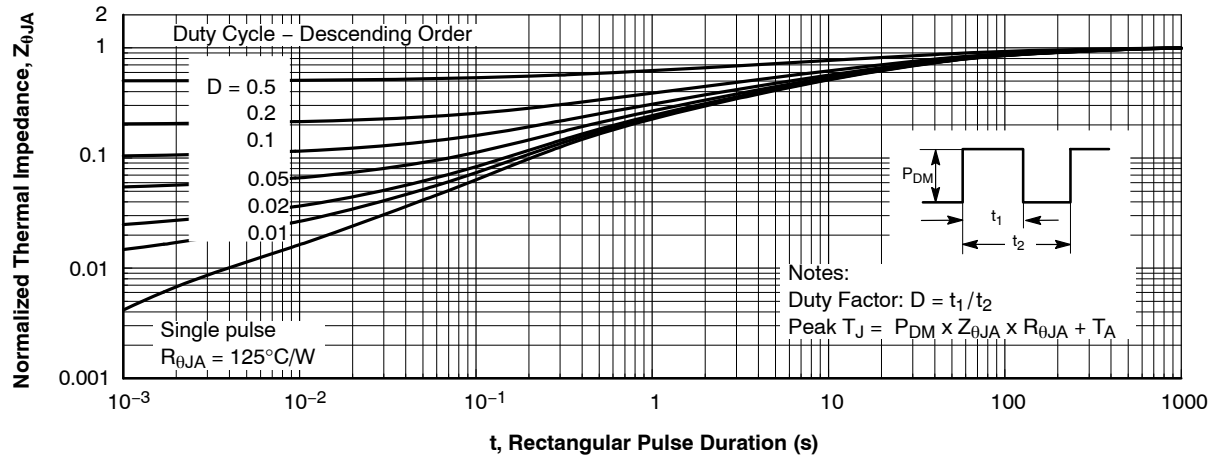


Figure 14. Junction-to-Ambient Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping [†]
FDMC6679AZ	FDMC6679AZ	WDFN8 3.3x3.3, 0.65P, Case 511DH (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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MECHANICAL CASE OUTLINE

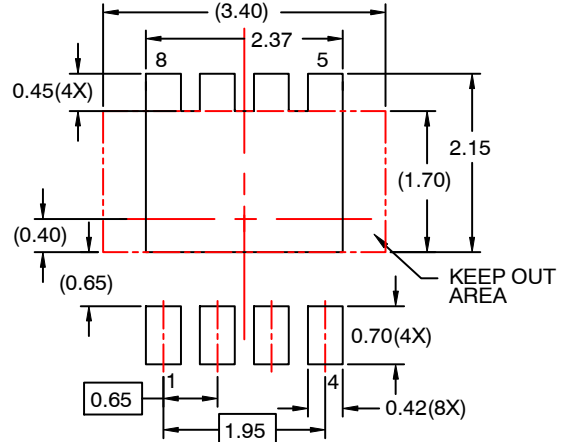
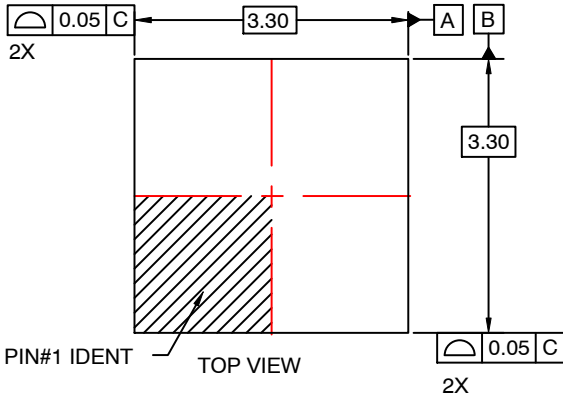
PACKAGE DIMENSIONS

ON Semiconductor®

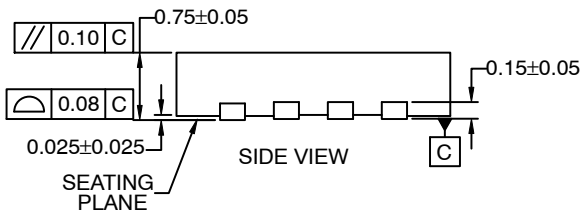


WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

DATE 31 JUL 2016

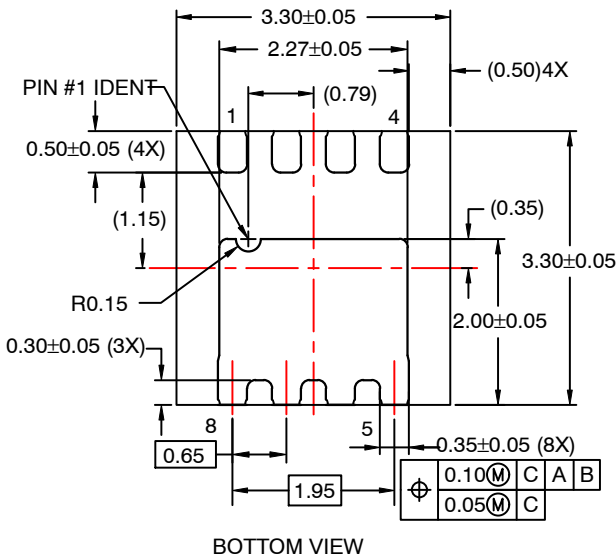


RECOMMENDED LAND PATTERN



NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



BOTTOM VIEW

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