

MOSFET - PowerTrench[®], N-Channel, Dual Cool[™], Shielded Gate

150 V, 40 A, 17 mΩ



ON Semiconductor[®]

www.onsemi.com

FDMS86200DC

General Description

This N-Channel MOSFET is produced using ON Semiconductor's advanced PowerTrench[®] process that incorporates Shielded Gate technology. Advancements in both silicon and Dual Cool[™] package technologies have been combined to offer the lowest $r_{DS(on)}$ while maintaining excellent switching performance by extremely low Junction-to-Ambient thermal resistance.

Features

- Shielded Gate MOSFET Technology
- Dual Cool[™] Top Side Cooling DFN8 Package
- Max $r_{DS(on)}$ = 17 mΩ at $V_{GS} = 10$ V, $I_D = 9.3$ A
- Max $r_{DS(on)}$ = 25 mΩ at $V_{GS} = 6$ V, $I_D = 7.8$ A
- High Performance Technology for Extremely Low $r_{DS(on)}$
- 100% UIL Tested
- RoHS Compliant

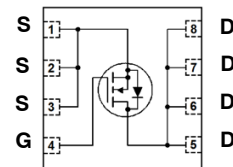
Applications

- Primary MOSFET in DC - DC Converters
- Secondary Synchronous Rectifier
- Load Switch

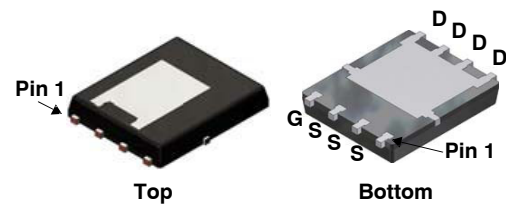
MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: Continuous, $T_C = 25^\circ\text{C}$ Continuous, $T_A = 25^\circ\text{C}$ (Note 1a) Pulsed (Note 4)	40 9.3 100	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	294	mJ
P_D	Power Dissipation: $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	125 3.2	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

ELECTRICAL CONNECTION

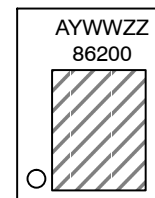


N-Channel MOSFET



DFN8, Dual Cool[™]
CASE 506EG

MARKING DIAGRAM



86200 = Specific Device Code
A = Assembly Location
Y = Year of Production, Last Number
WW = Work Week Number
ZZ = Assembly Lot Number

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMS86200DC

Table 1. THERMAL CHARACTERISTICS

Symbol	Characteristic	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	2.5	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	11	

ORDERING INFORMATION AND PACKAGE MARKING

Device	Top Marking	Package	Reel Size	Tape Width	Shipping†
FDMS86200DC	86200	DFN8	13"	12 mm	3000 Units/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	150			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		105		mV/°C
I_{BSS}	Zero Gate Voltage Drain Current	$V_{DS} = 120 \text{ V}$, $V_{GS} = 0 \text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$			± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	2.0	3.3	4.0	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		-11		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 9.3 \text{ A}$		14	17	m Ω
		$V_{GS} = 6 \text{ V}$, $I_D = 7.8 \text{ A}$		17	25	
		$V_{GS} = 10 \text{ V}$, $I_D = 9.3 \text{ A}$, $T_J = 125^\circ\text{C}$		29	35	
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}$, $I_D = 9.3 \text{ A}$		32		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 75 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		2110	2955	pF
C_{oss}	Output Capacitance			205	290	pF
C_{rss}	Reverse Transfer Capacitance			8.1	15	pF
R_g	Gate Resistance		0.1	1.5	3.0	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75 \text{ V}$, $I_D = 9.3 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_{GEN} = 6 \Omega$		16	29	ns
t_r	Rise Time			4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			23	37	ns
t_f	Fall Time			5	10	ns

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}, V_{DD} = 75\text{ V}, I_D = 9.3\text{ A}$		30	42	nC
		$V_{GS} = 0\text{ V to }5\text{ V}, V_{DD} = 75\text{ V}, I_D = 9.3\text{ A}$		19	27	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = 75\text{ V}, I_D = 9.3\text{ A}$		9.7		nC
Q_{gd}	Gate to Drain "Miller" Charge			5.6		nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 9.3\text{ A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\text{ V}, I_S = 2.6\text{ A}$ (Note 2)		0.7	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 9.3\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		79	126	ns
Q_{rr}	Reverse Recovery Charge			126	176	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

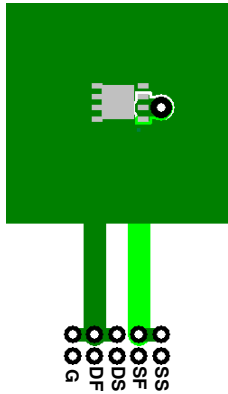
RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Top Source)	2.5	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Bottom Drain)	1.0	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	38	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	81	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	27	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	34	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1e)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1f)	19	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1g)	26	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1h)	61	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1i)	16	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1j)	23	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1k)	11	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1l)	13	

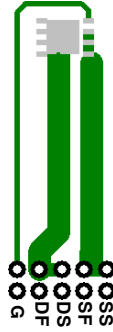
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.

FDMS86200DC

NOTES: $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 38°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 81°C/W when mounted on a 1 in² pad of 2 oz copper.

- c) Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- d) Still air, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- e) Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- f) Still air, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper
- g) 200FPM Airflow, No Heat Sink, 1 in² pad of 2 oz copper
- h) 200FPM Airflow, No Heat Sink, minimum pad of 2 oz copper
- i) 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, 1 in² pad of 2 oz copper
- j) 200FPM Airflow, 20.9x10.4x12.7mm Aluminum Heat Sink, minimum pad of 2 oz copper
- k) 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, 1 in² pad of 2 oz copper
- l) 200FPM Airflow, 45.2x41.4x11.7mm Aavid Thermalloy Part # 10-L41B-11 Heat Sink, minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0%.
- 3. E_{AS} of 294 mJ is based on starting $T_J = 25^\circ\text{C}$; N-ch: $L = 3$ mH, $I_{AS} = 14$ A, $V_{DD} = 150$ V. $V_{GS} = 10$ V, 100% tested at $L = 0.3$ mH, $I_{AS} = 31$ A.
- 4. Pulsed Id limited by junction temperature, $t_d \leq 10$ μ s, please refer to SOA curve for more details.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

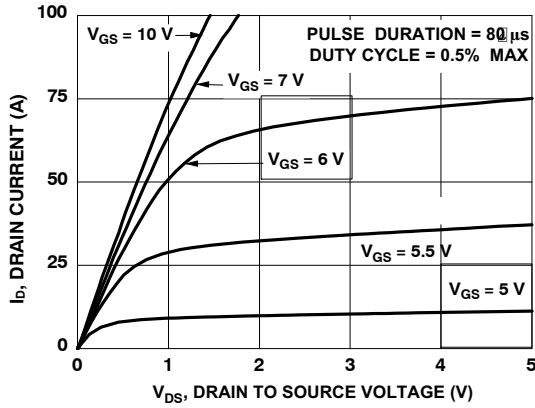


Figure 1. On-Region Characteristics

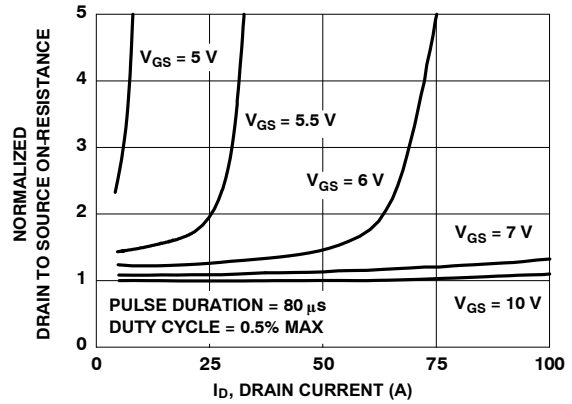


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

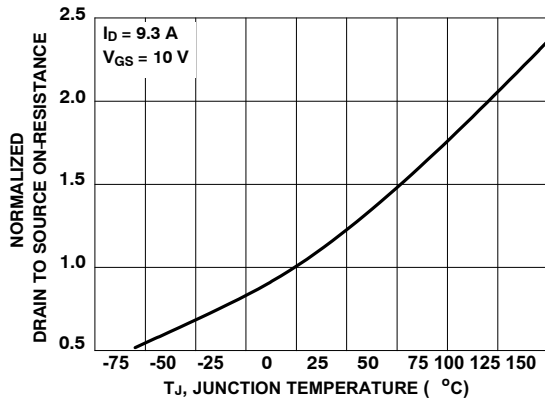


Figure 3. Normalized On-Resistance vs. Junction Temperature

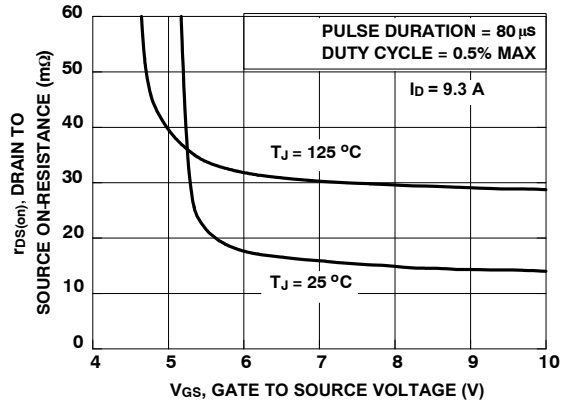


Figure 4. On-Resistance vs. Gate to Source Voltage

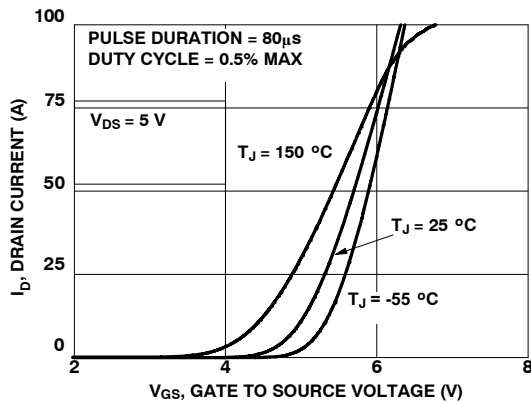


Figure 5. Transfer Characteristics

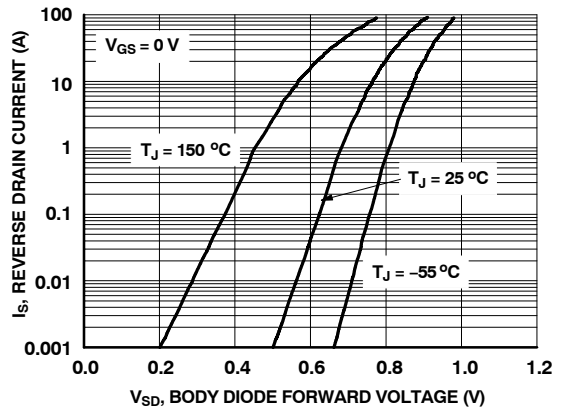


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

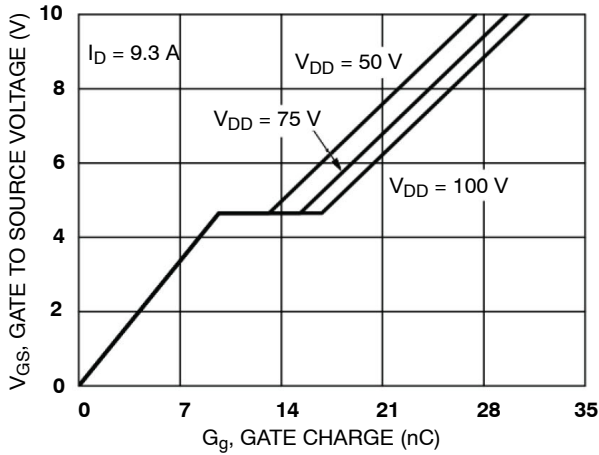


Figure 7. Gate Charge Characteristics

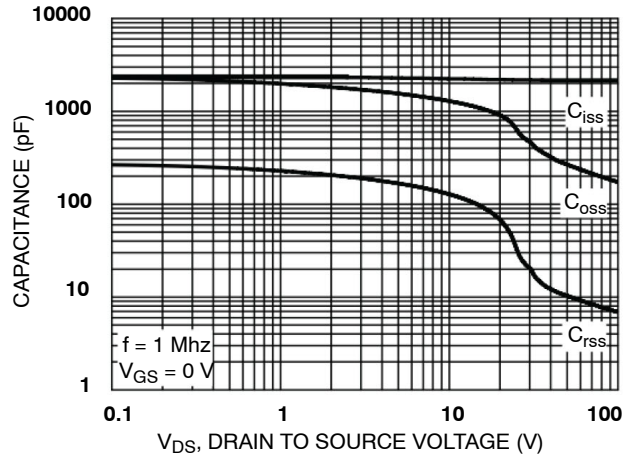


Figure 8. Capacitance vs Drain to Source Voltage

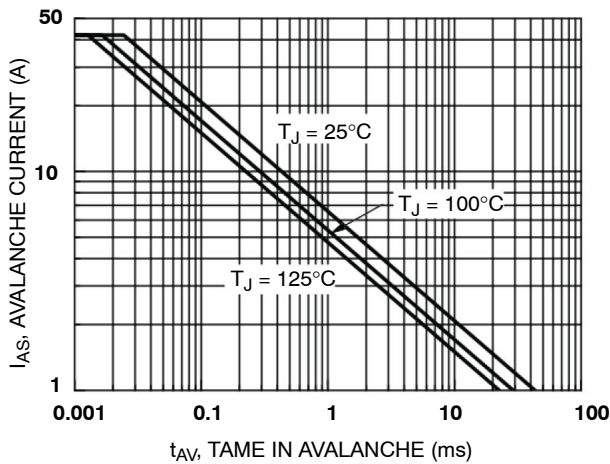


Figure 9. Unclamped Inductive Switching Capability

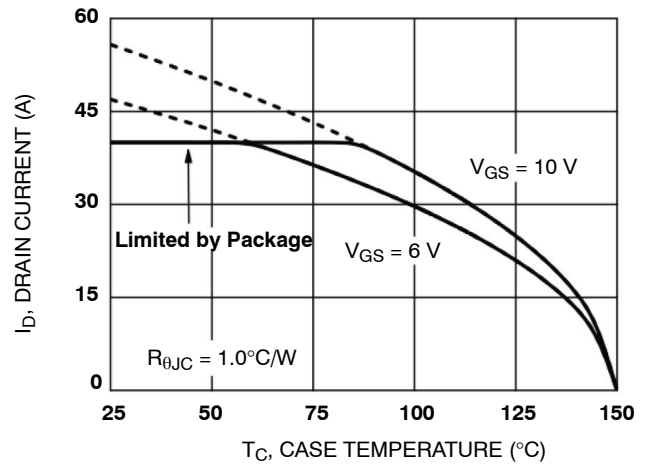


Figure 10. Maximum Continuous Drain Current vs Case Temperature

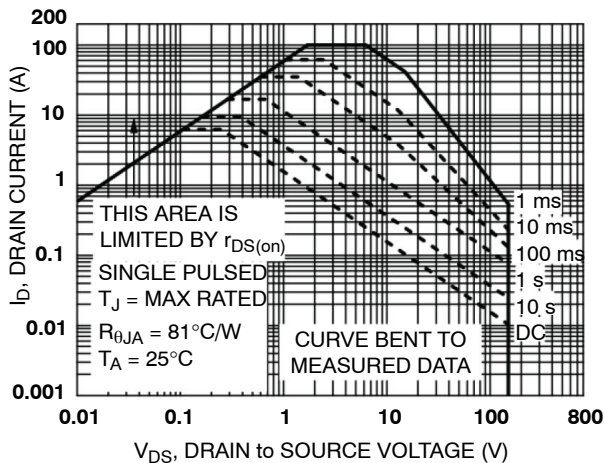


Figure 11. Forward Bias Safe Operating Area

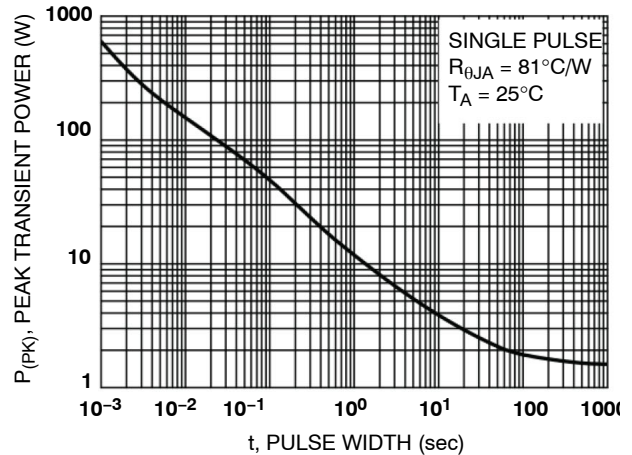


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

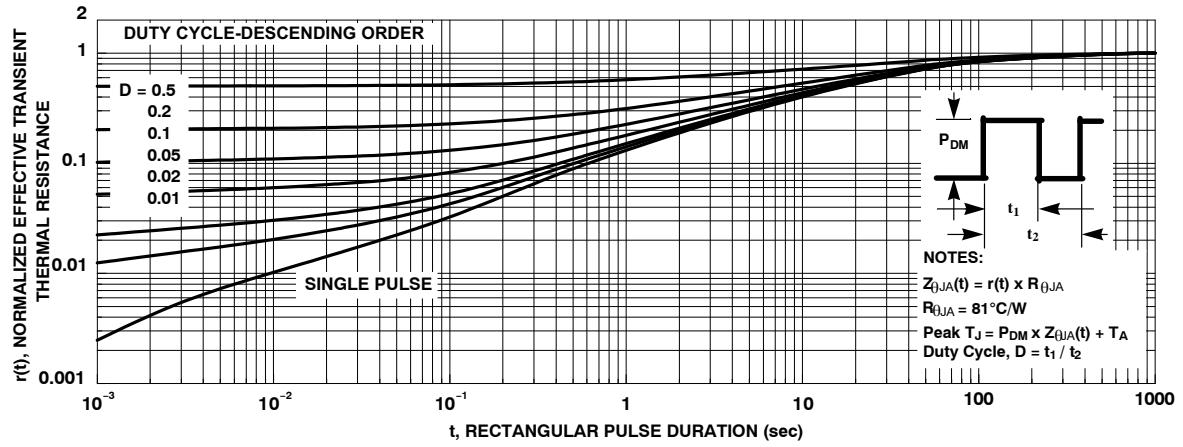


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

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DUAL COOL is a trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries.

MECHANICAL CASE OUTLINE

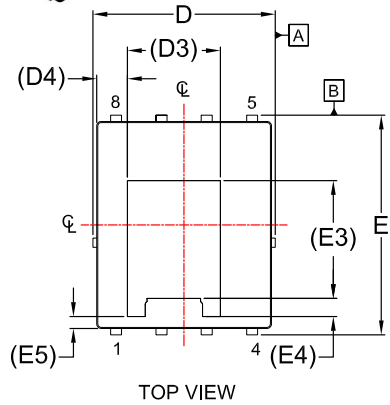
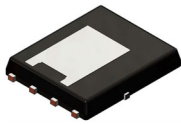
PACKAGE DIMENSIONS

ON Semiconductor®

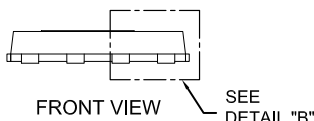


DFN8 5x6.15, 1.27P, DUAL COOL CASE 506EG ISSUE D

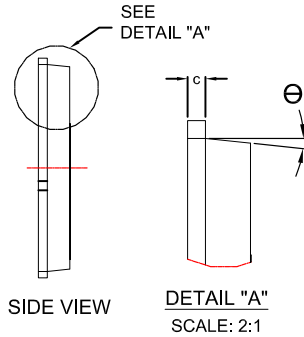
DATE 25 AUG 2020



TOP VIEW



FRONT VIEW

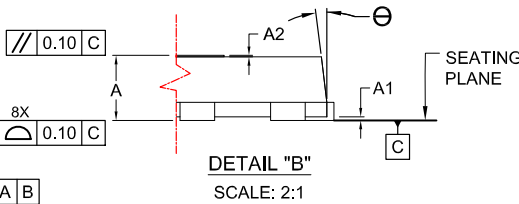


SIDE VIEW

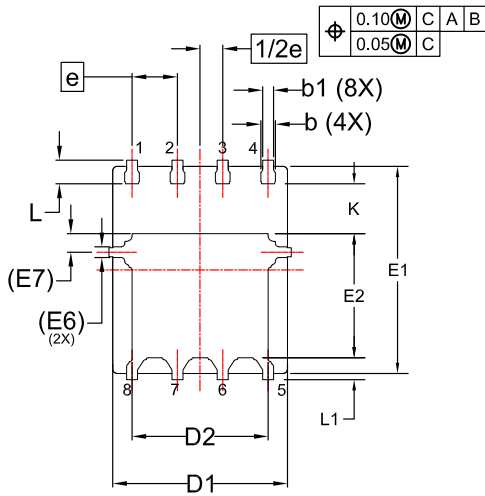
DETAIL "A"
SCALE: 2:1

NOTES:

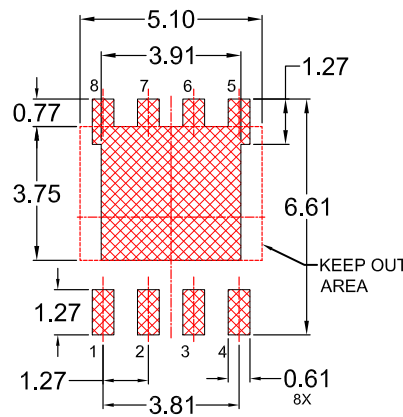
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.



DETAIL "B"
SCALE: 2:1



BOTTOM VIEW

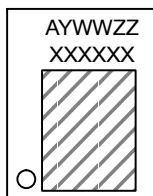


LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.85	0.90	0.95
A1	-	-	0.05
A2	-	-	0.05
b	0.31	0.41	0.51
b1	0.21	0.31	0.41
c	0.20	0.25	0.30
D	4.90	5.00	5.10
D1	4.80	4.90	5.00
D2	3.67	3.82	3.97
D3	2.60 REF		
D4	0.86 REF		
E	6.05	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.58
E3	3.30 REF		
E4	0.50 REF		
E5	0.34 REF		
E6	0.30 REF		
E7	0.52 REF		
e	1.27 BSC		
1/2e	0.635 BSC		
K	1.30	1.40	1.50
L	0.56	0.66	0.76
L1	0.52	0.62	0.72
θ	0°	---	12°

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DFN8 5x6.15, 1.27P, DUAL COOL	PAGE 1 OF 1

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