PD- 95141

International
IOR Rectifier

IRFPS40N50LPbF

SMPS MOSFET

HEXFET® Power MOSFET

V_{DSS}	$R_{DS(on)}$ typ.	Trr typ.	I_D
500V	0.087Ω	170ns	46A

Applications

- Zero Voltage Switching SMPS
- Telecom and Server Power Supplies
- Uninterruptible Power Supplies
- Motor Control applications
- Lead-Free

Features and Benefits

- SuperFast body diode eliminates the need for external diodes in ZVS applications.
- Lower Gate charge results in simpler drive requirements.
- Enhanced dv/dt capabilities offer improved ruggedness.
- Higher Gate voltage threshold offers improved noise immunity.

Super-247™

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	46	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	29	
I_{DM}	Pulsed Drain Current ①	180	
P_D @T_C = 25°C	Power Dissipation	540	W
	Linear Derating Factor	4.3	W/°C
V_{GS}	Gate-to-Source Voltage	±30	V
dv/dt	Peak Diode Recovery dv/dt ②	34	V/ns
T_J	Operating Junction and	-55 to + 150	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	46	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	180		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	T_J = 25°C, I_S = 46A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	170	250	ns	T_J = 25°C, I_F = 46A
		—	220	330		T_J = 125°C, di/dt = 100A/µs ④
Q_{rr}	Reverse Recovery Charge	—	705	1060	nC	T_J = 25°C, I_S = 46A, V_{GS} = 0V ④
		—	1.3	2.0		T_J = 125°C, di/dt = 100A/µs ④
I_{RRM}	Reverse Recovery Current	—	9.0	—	A	T_J = 25°C
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

09/14/04

Static @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.60	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.087	0.100	Ω	V_{GS} = 10V, I_D = 28A ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	µA	V_{DS} = 500V, V_{GS} = 0V
		—	—	2.0	mA	V_{DS} = 400V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -30V
R_G	Internal Gate Resistance	—	0.90	—	Ω	f = 1MHz, open drain

Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
gfs	Forward Transconductance	21	—	—	S	V_{DS} = 50V, I_D = 46A
Q_g	Total Gate Charge	—	—	380	nC	I_D = 46A
Q_{gs}	Gate-to-Source Charge	—	—	80		V_{DS} = 400V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	190		V_{GS} = 10V, See Fig. 7 & 15 ④
$t_{d(on)}$	Turn-On Delay Time	—	27	—	ns	V_{DD} = 250V
t_r	Rise Time	—	170	—		I_D = 46A
$t_{d(off)}$	Turn-Off Delay Time	—	50	—		R_G = 0.85Ω
t_f	Fall Time	—	69	—		V_{GS} = 10V, See Fig. 14a & 14b ④
C_{iss}	Input Capacitance	—	8110	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	960	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	130	—		*f* = 1.0MHz, See Fig. 5
C_{oss}	Output Capacitance	—	11200	—		V_{GS} = 0V, VDS = 1.0V, *f* = 1.0MHz
C_{oss}	Output Capacitance	—	240	—		V_{GS} = 0V, VDS = 400V, *f* = 1.0MHz
C_{oss} eff.	Effective Output Capacitance	—	440	—		V_{GS} = 0V,V_{DS} = 0V to 400V ⑤
C_{oss} eff. (ER)	Effective Output Capacitance (Energy Related)	—	310	—		

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	920	mJ
I_{AR}	Avalanche Current ①	—	46	A
E_{AR}	Repetitive Avalanche Energy ①	—	54	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case⑥	—	0.23	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient⑥	—	40	

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See Fig. 11).

② Starting T_J = 25°C, L = 0.86mH, R_G = 25Ω, I_{AS} = 46A. (See Figure 12).

③ I_{SD} ≤ 46A, di/dt ≤ 550A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 150°C.

④ Pulse width ≤ 400µs; duty cycle ≤ 2%.

⑤ C_{oss} eff. is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
C_{oss} eff.(ER) is a fixed capacitance that stores the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ R_θ is measured at T_J approximately 90°C

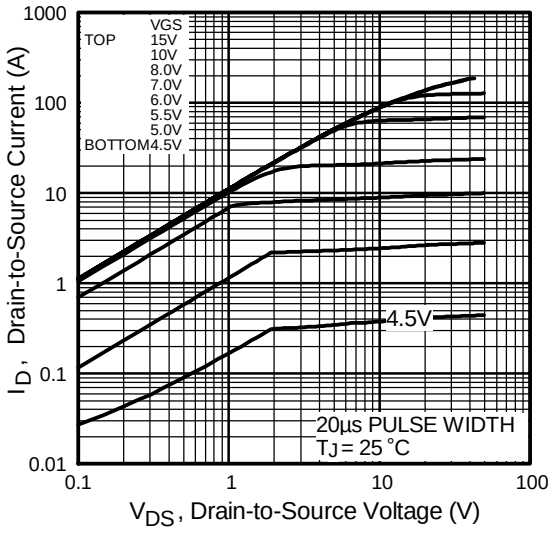


Fig 1. Typical Output Characteristics

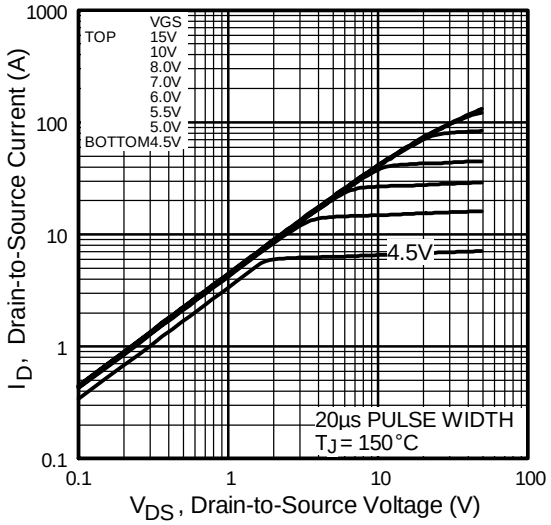


Fig 2. Typical Output Characteristics

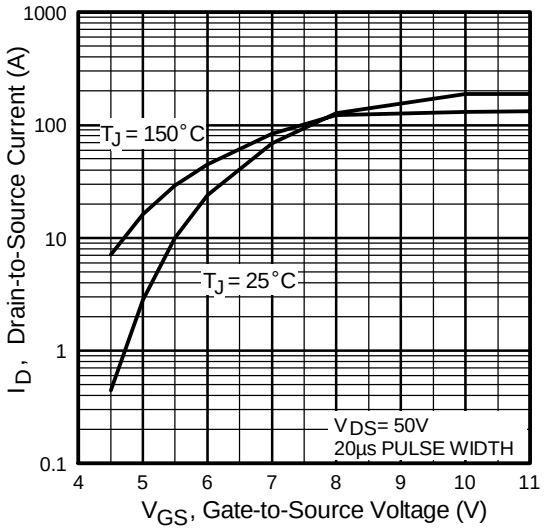


Fig 3. Typical Transfer Characteristics

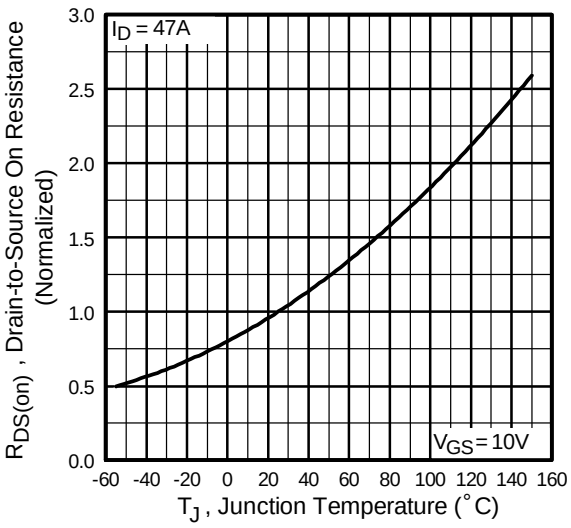


Fig 4. Normalized On-Resistance vs. Temperature

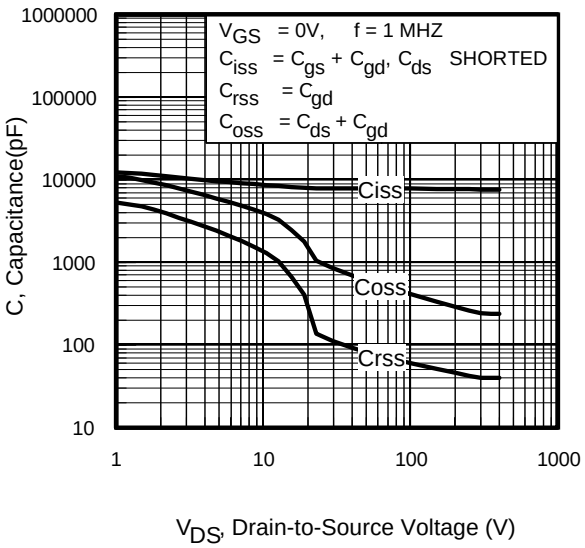


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

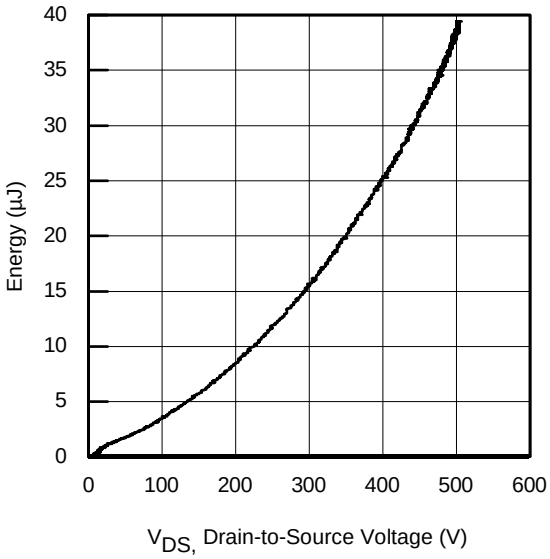


Fig 6. Typ. Output Capacitance Stored Energy vs. V_{DS}

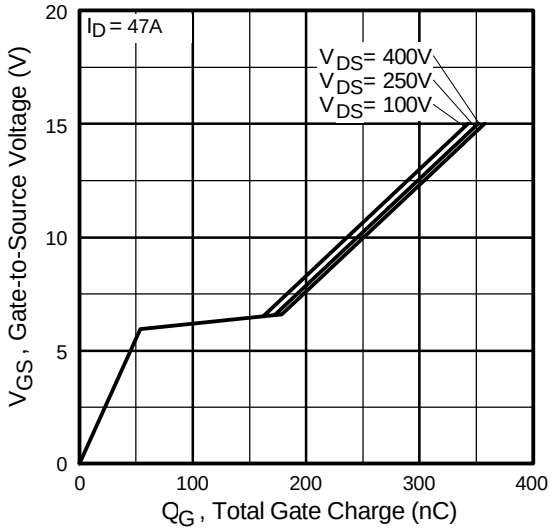


Fig 7. Typical Gate Charge vs. Gate-to-Source Voltage

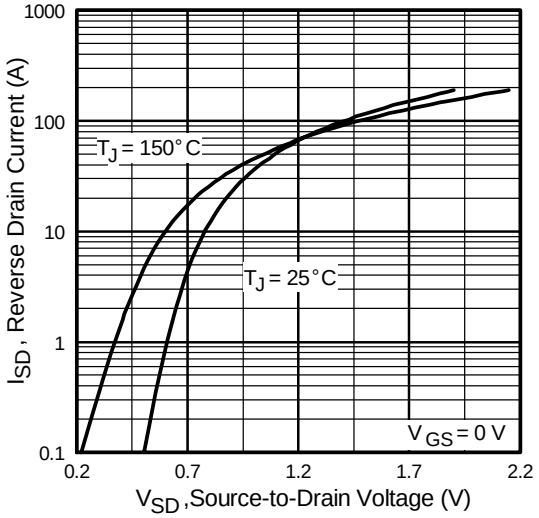


Fig 8. Typical Source-Drain Diode Forward Voltage

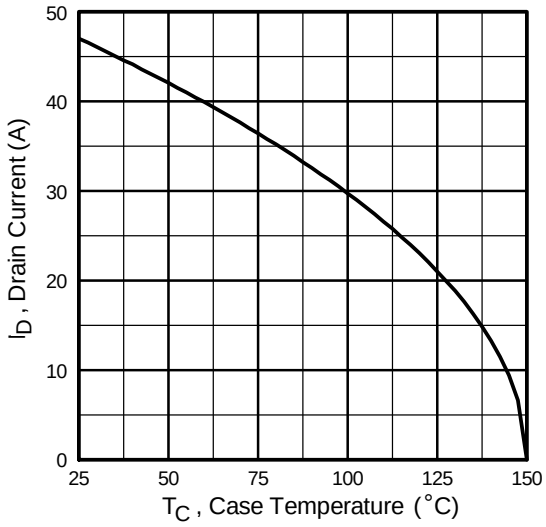


Fig 9. Maximum Drain Current vs. Case Temperature

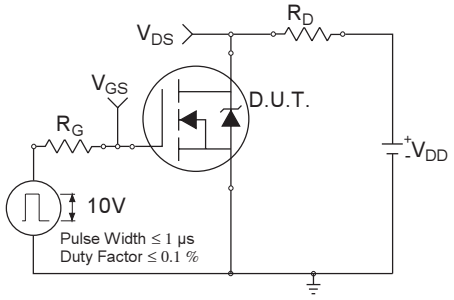


Fig 10a. Switching Time Test Circuit

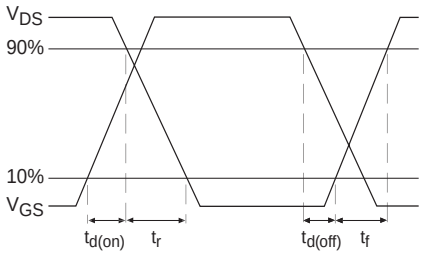


Fig 10b. Switching Time Waveforms

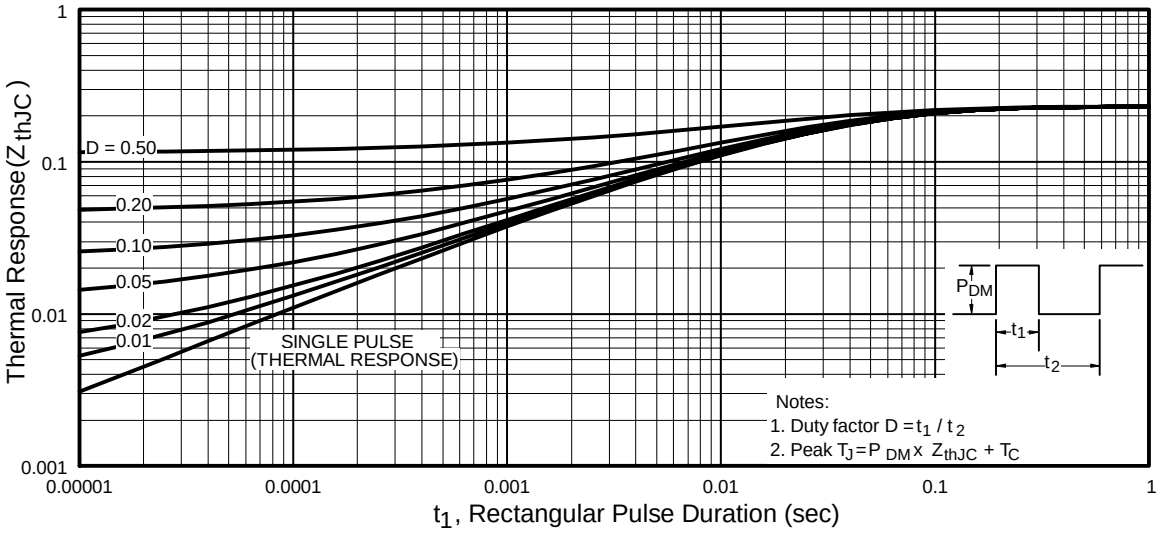


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

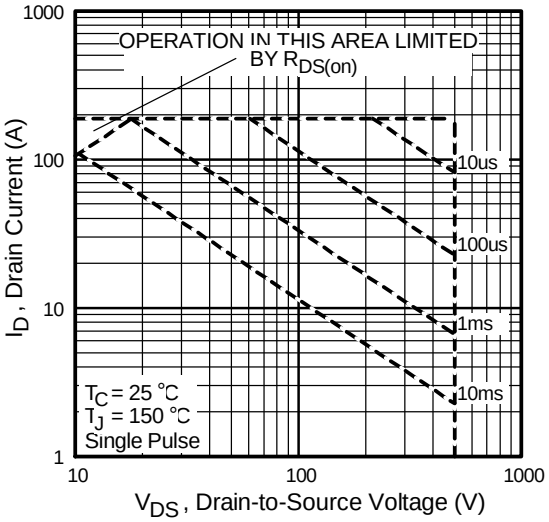


Fig 12. Maximum Safe Operating Area

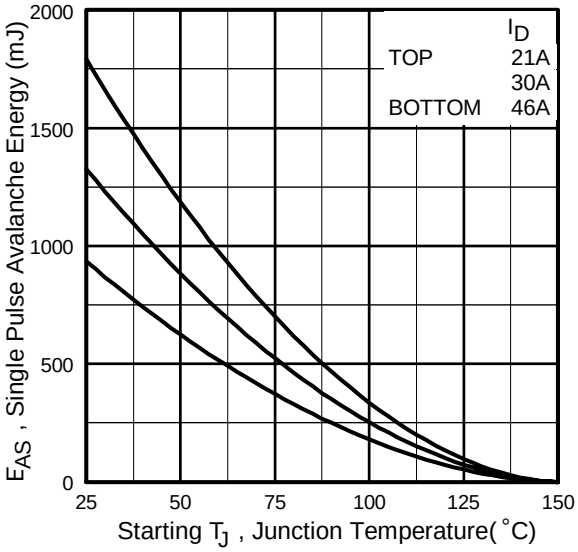


Fig 13. Maximum Avalanche Energy vs. Drain Current

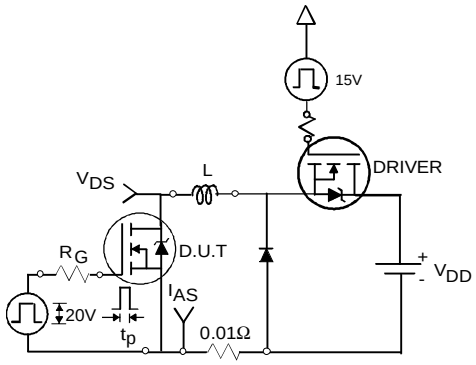


Fig 14a. Unclamped Inductive Test Circuit

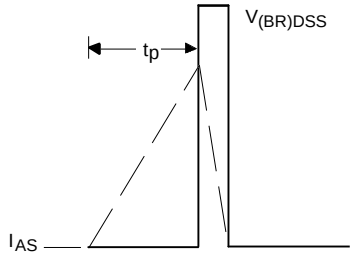


Fig 14b. Unclamped Inductive Waveforms

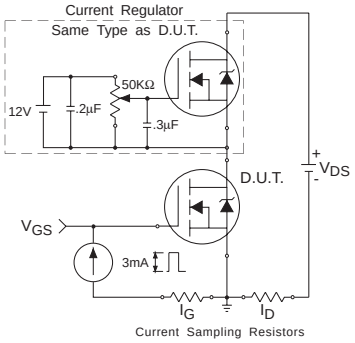


Fig 15a. Gate Charge Test Circuit

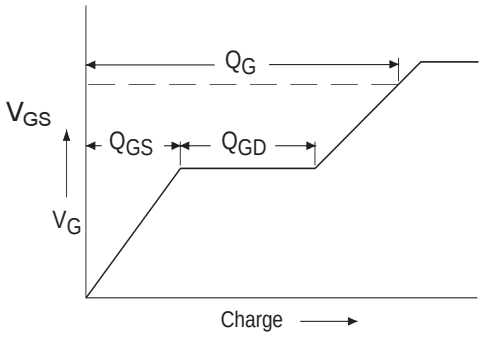


Fig 15b. Basic Gate Charge Waveform

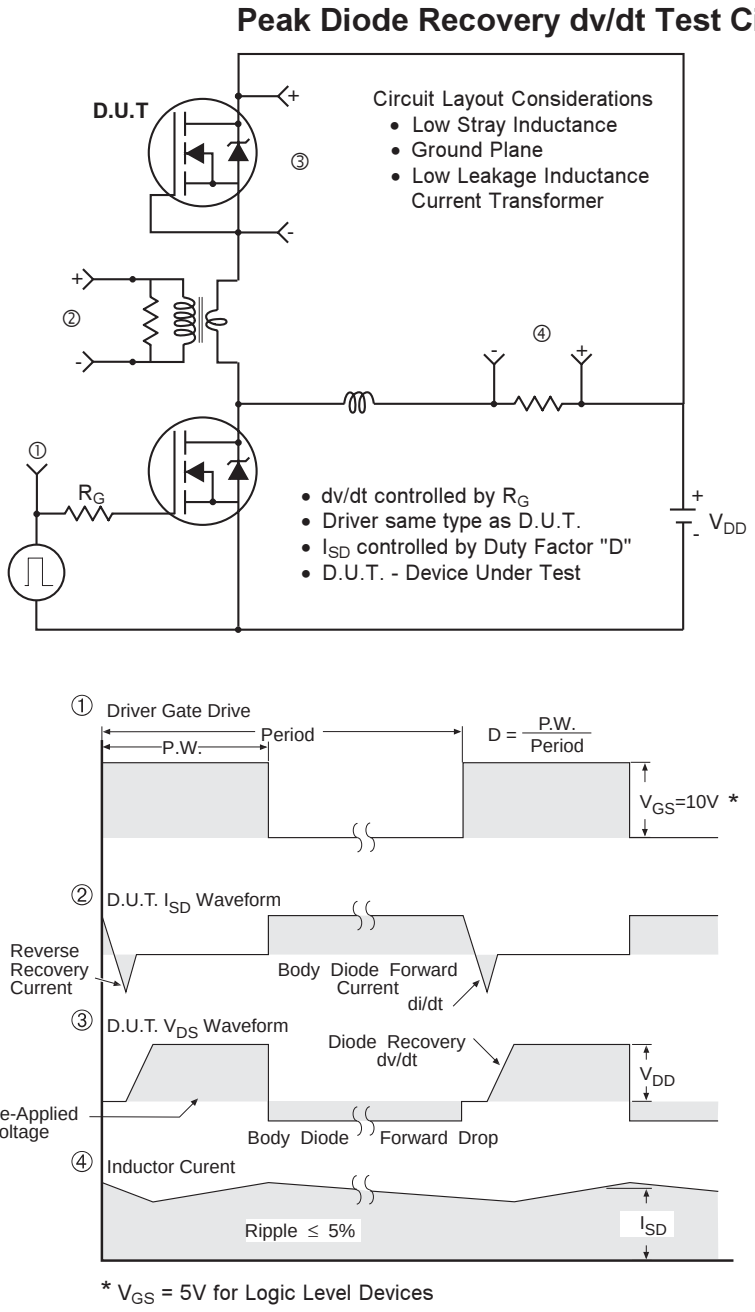
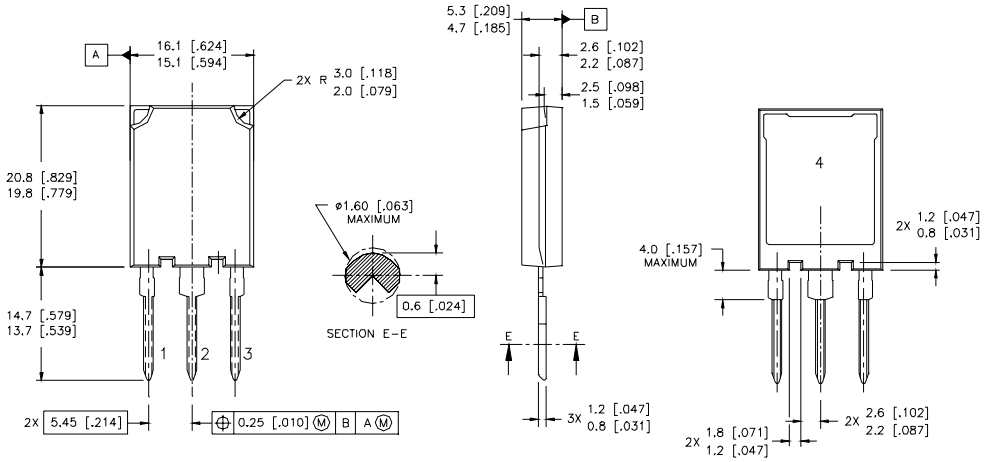


Fig 16. For N-Channel HEXFET® Power MOSFETs

Case Outline and Dimensions — Super-247



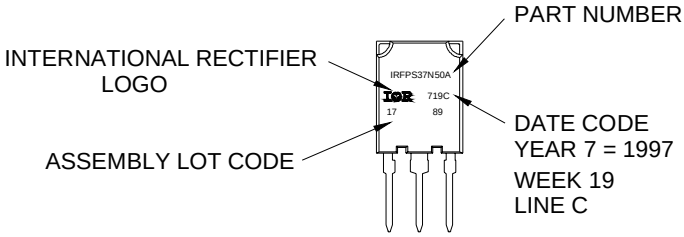
NOTES:
1. DIMENSIONS & TOLERANCING PER ASME Y14.5M-1994
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETRES [INCHES]

LEAD ASSIGNMENTS

MOSFET	IGBT
1 – GATE	1 – GATE
2 – DRAIN	2 – COLLECTOR
3 – SOURCE	3 – EMITTER
4 – DRAIN	4 – COLLECTOR

Super-247 (TO-274AA) Part Marking Information

EXAMPLE: THIS IS AN IRFPS37N50A WITH
ASSEMBLY LOT CODE 1789
ASSEMBLED ON WW 19, 1997
IN THE ASSEMBLY LINE "C"



Note: "P" in assembly line position indicates "Lead-Free"

TOP

Data and specifications subject to change without notice.
This product has been designed and qualified for the industrial market.
Qualification Standards can be found on IR's Web site.

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information.09/04