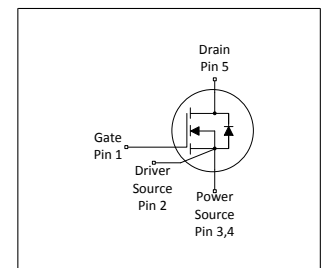
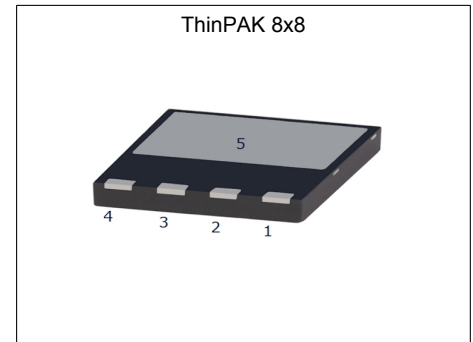


## MOSFET

### 650V CoolMOS™ C7 Power Transistor

CoolMOS™ is a revolutionary technology for high voltage power MOSFETs, designed according to the superjunction (SJ) principle and pioneered by Infineon Technologies.

CoolMOS™ C7 series combines the experience of the leading SJ MOSFET supplier with high class innovation. The product portfolio provides all benefits of fast switching superjunction MOSFETs offering better efficiency, reduced gate charge, easy implementation and outstanding reliability.



### Features

- Increased MOSFET dv/dt ruggedness
- Better efficiency due to best in class FOM  $R_{DS(on)} * E_{oss}$  and  $R_{DS(on)} * Q_g$
- **ThinPAK** SMD Package with very low parasitic inductance to enable fast and reliable switching with minimum of size to increase power-density
- Easy to use/drive due to **driver source pin** for better control of the gate.
- Pb-free plating, halogen free mold compound
- Qualified for industrial grade applications according to JEDEC (J-STD20 and JESD22)

### Benefits

- Enabling higher system efficiency by lower switching losses
- Enabling higher frequency / increased power density solutions
- System cost / size savings due to reduced cooling requirements
- Higher system reliability due to lower operating temperatures



### Potential applications

PFC stages and hard switching PWM stages for e.g. Computing, Server, Telecom, UPS and Solar.

*Please note: For MOSFET paralleling the use of ferrite beads on the gate or separate totem poles is generally recommended.*

**Table 1 Key Performance Parameters**

Parameter	Value	Unit
$V_{DS} @ T_{j,max}$	700	V
$R_{DS(on),max}$	130	mΩ
$Q_{g,typ}$	35	nC
$I_{D,pulse}$	75	A
$E_{oss} @ 400V$	4.2	μJ
Body diode $di_F/dt$	55	A/μs

Type / Ordering Code	Package	Marking	Related Links
IPL65R130C7	PG-VSON-4	65C7130	see Appendix A

## Table of Contents

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## 1 Maximum ratings

at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current <sup>1)</sup>	$I_D$	-	-	15 11	A	$T_C=25^\circ\text{C}$ $T_C=100^\circ\text{C}$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	75	A	$T_C=25^\circ\text{C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	89	mJ	$I_D=7.1\text{A}; V_{DD}=50\text{V}$
Avalanche energy, repetitive	$E_{AR}$	-	-	0.44	mJ	$I_D=7.1\text{A}; V_{DD}=50\text{V}$
Avalanche current, single pulse	$I_{AS}$	-	-	7.1	A	-
MOSFET dv/dt ruggedness	dv/dt	-	-	100	V/ns	$V_{DS}=0\dots400\text{V}$
Gate source voltage (static)	$V_{GS}$	-20	-	20	V	static;
Gate source voltage (dynamic)	$V_{GS}$	-30	-	30	V	AC ( $f>1\text{ Hz}$ )
Power dissipation	$P_{tot}$	-	-	102	W	$T_C=25^\circ\text{C}$
Storage temperature	$T_{stg}$	-40	-	150	$^\circ\text{C}$	-
Operating junction temperature	$T_j$	-40	-	150	$^\circ\text{C}$	-
Mounting torque	-	-	-	n.a.	Ncm	-
Continuous diode forward current	$I_S$	-	-	15	A	$T_C=25^\circ\text{C}$
Diode pulse current <sup>2)</sup>	$I_{S,pulse}$	-	-	75	A	$T_C=25^\circ\text{C}$
Reverse diode dv/dt <sup>3)</sup>	dv/dt	-	-	1.5	V/ns	$V_{DS}=0\dots400\text{V}, I_{SD}\leq I_S, T_j=25^\circ\text{C}$
Maximum diode commutation speed	di <sub>f</sub> /dt	-	-	55	A/ $\mu\text{s}$	$V_{DS}=0\dots400\text{V}, I_{SD}\leq I_S, T_j=25^\circ\text{C}$
Insulation withstand voltage	$V_{ISO}$	-	-	n.a.	V	$V_{rms}, T_C=25^\circ\text{C}, t=1\text{min}$

<sup>1)</sup> Limited by  $T_{j,max}$ .

<sup>2)</sup> Pulse width  $t_p$  limited by  $T_{j,max}$

<sup>3)</sup> Identical low side and high side switch with identical  $R_G$

## 2 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	-	1.22	°C/W	-
Thermal resistance, junction - ambient	$R_{thJA}$	-	-	62	°C/W	device on PCB, minimal footprint
Thermal resistance, junction - ambient for SMD version	$R_{thJA}$	-	35	45	°C/W	Device on 40mm*40mm*1.5mm epoxy PCB FR4 with 6cm <sup>2</sup> (one layer, 70µm thickness) copper area for drain connection and cooling. PCB is vertical without air stream cooling.
Reflow soldering temperature	$T_{sold}$	-	-	260	°C	reflow MSL2a

**3 Electrical characteristics**  
at  $T_j=25^\circ\text{C}$ , unless otherwise specified

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	650	-	-	V	$V_{GS}=0V, I_D=1mA$
Gate threshold voltage	$V_{(GS)th}$	3	3.5	4	V	$V_{DS}=V_{GS}, I_D=0.44mA$
Zero gate voltage drain current	$I_{DSS}$	-	-	1	$\mu\text{A}$	$V_{DS}=650, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=650, V_{GS}=0V, T_j=150^\circ\text{C}$
Gate-source leakage current	$I_{GSS}$	-	-	100	nA	$V_{GS}=20V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	0.115 0.276	0.130 -	$\Omega$	$V_{GS}=10V, I_D=4.4A, T_j=25^\circ\text{C}$ $V_{GS}=10V, I_D=4.4A, T_j=150^\circ\text{C}$
Gate resistance	$R_G$	-	1	-	$\Omega$	$f=1\text{MHz}$ , open drain

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	1670	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Output capacitance	$C_{oss}$	-	26	-	pF	$V_{GS}=0V, V_{DS}=400V, f=250\text{kHz}$
Effective output capacitance, energy related <sup>1)</sup>	$C_{o(er)}$	-	53	-	pF	$V_{GS}=0V, V_{DS}=0...400V$
Effective output capacitance, time related <sup>2)</sup>	$C_{o(tr)}$	-	579	-	pF	$I_D=\text{constant}, V_{GS}=0V, V_{DS}=0...400V$
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.4A, R_G=10\Omega$
Rise time	$t_r$	-	5.3	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.4A, R_G=10\Omega$
Turn-off delay time	$t_{d(off)}$	-	87	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.4A, R_G=10\Omega$
Fall time	$t_f$	-	12	-	ns	$V_{DD}=400V, V_{GS}=13V, I_D=4.4A, R_G=10\Omega$

**Table 6 Gate charge characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{GS}$	-	8	-	nC	$V_{DD}=400V, I_D=4.4A, V_{GS}=0$ to 10V
Gate to drain charge	$Q_{gd}$	-	11	-	nC	$V_{DD}=400V, I_D=4.4A, V_{GS}=0$ to 10V
Gate charge total	$Q_g$	-	35	-	nC	$V_{DD}=400V, I_D=4.4A, V_{GS}=0$ to 10V
Gate plateau voltage	$V_{plateau}$	-	5.0	-	V	$V_{DD}=400V, I_D=4.4A, V_{GS}=0$ to 10V

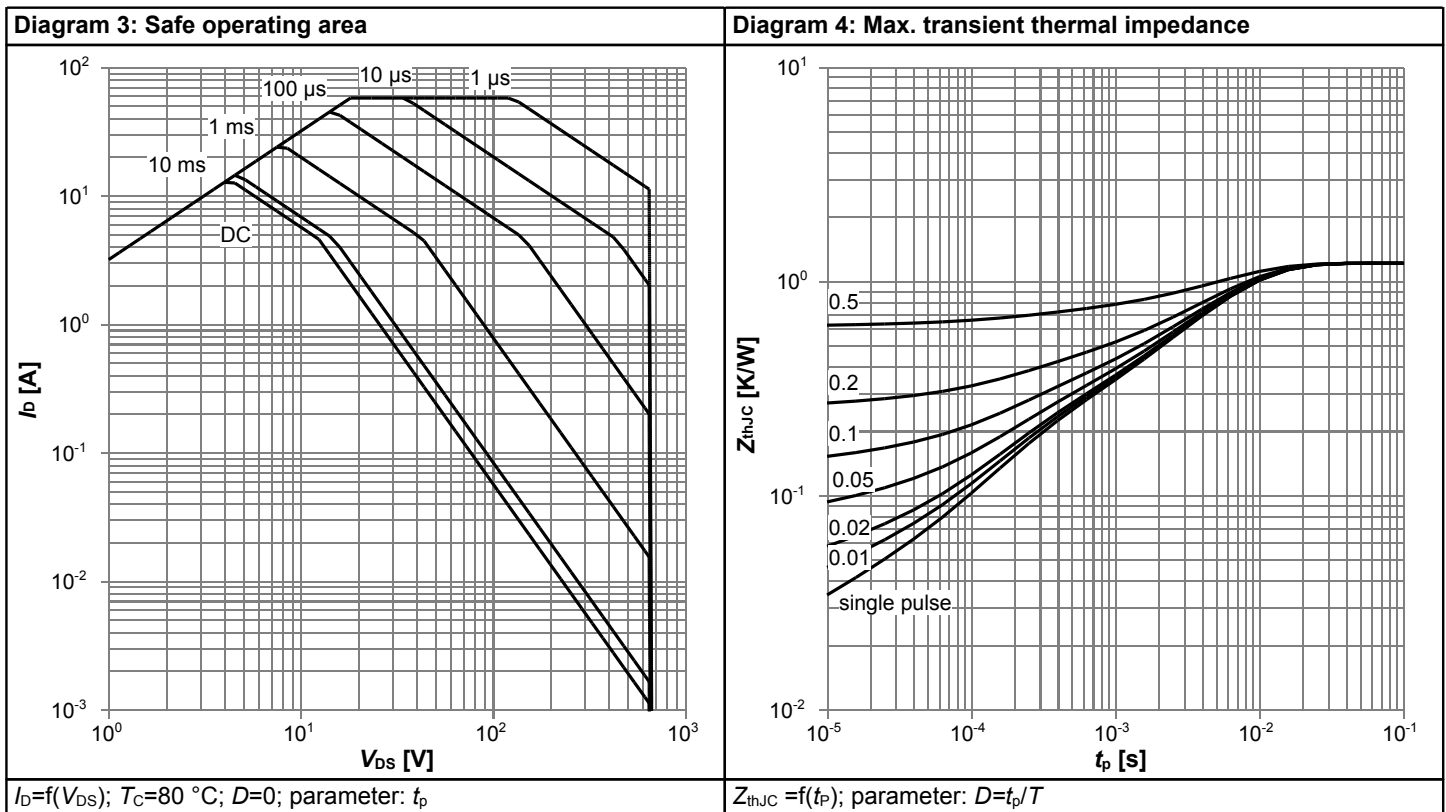
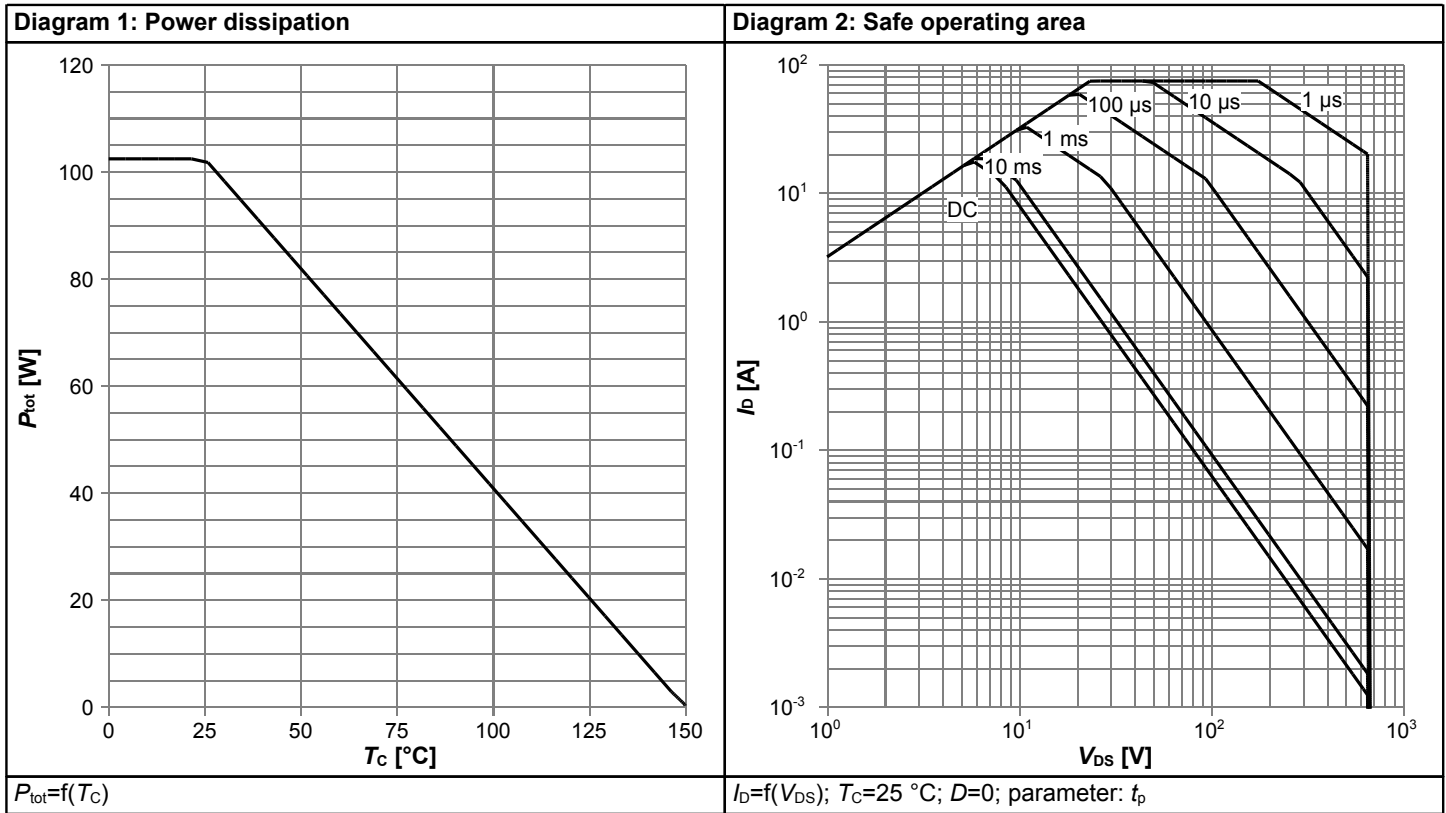
<sup>1)</sup>  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

<sup>2)</sup>  $C_{o(tr)}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 400V

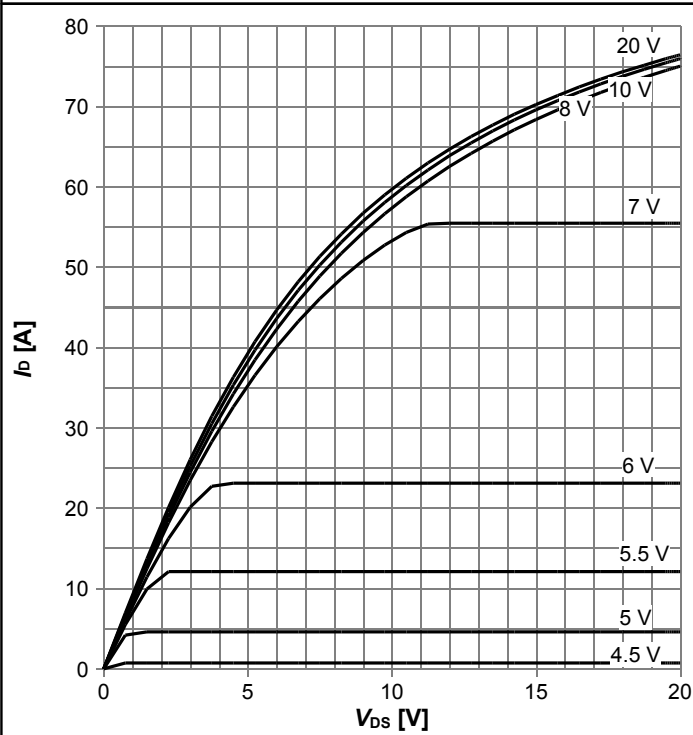
**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode forward voltage	$V_{SD}$	-	0.8	-	V	$V_{GS}=0V, I_F=4.4A, T_j=25^{\circ}C$
Reverse recovery time	$t_{rr}$	-	630	-	ns	$V_R=400V, I_F=15A, di_F/dt=55A/\mu s$
Reverse recovery charge	$Q_{rr}$	-	6.4	-	$\mu C$	$V_R=400V, I_F=15A, di_F/dt=55A/\mu s$
Peak reverse recovery current	$I_{rrm}$	-	20	-	A	$V_R=400V, I_F=15A, di_F/dt=55A/\mu s$

### 4 Electrical characteristics diagrams

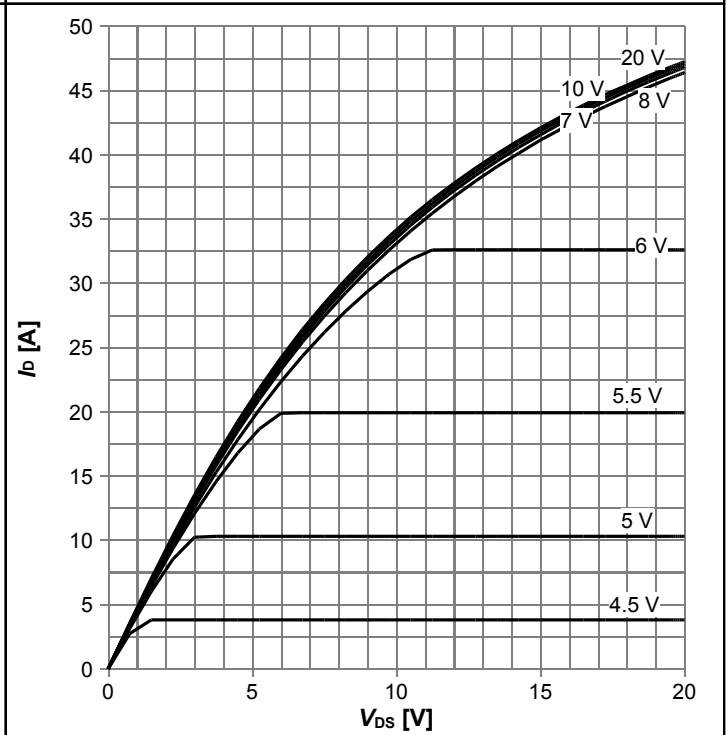


**Diagram 5: Typ. output characteristics**



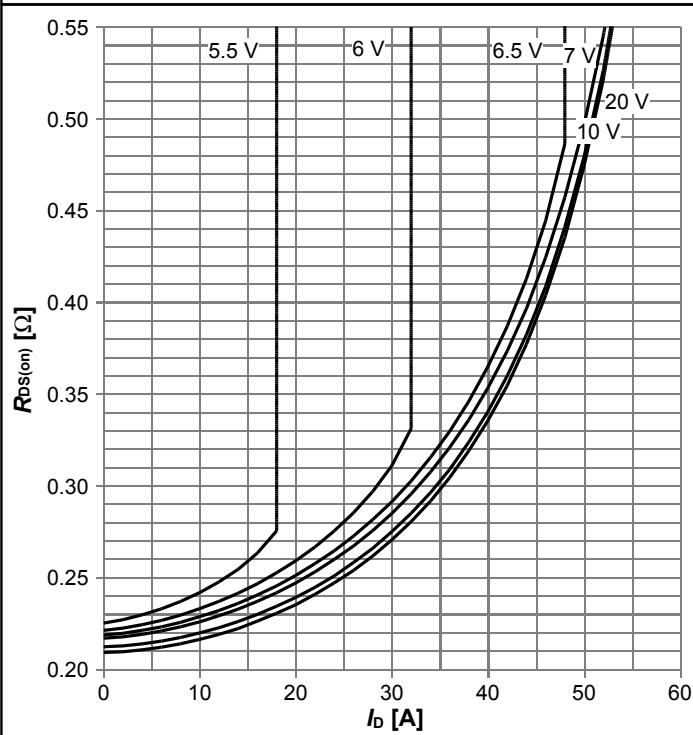
$I_D=f(V_{DS}); T_j=25\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

**Diagram 6: Typ. output characteristics**



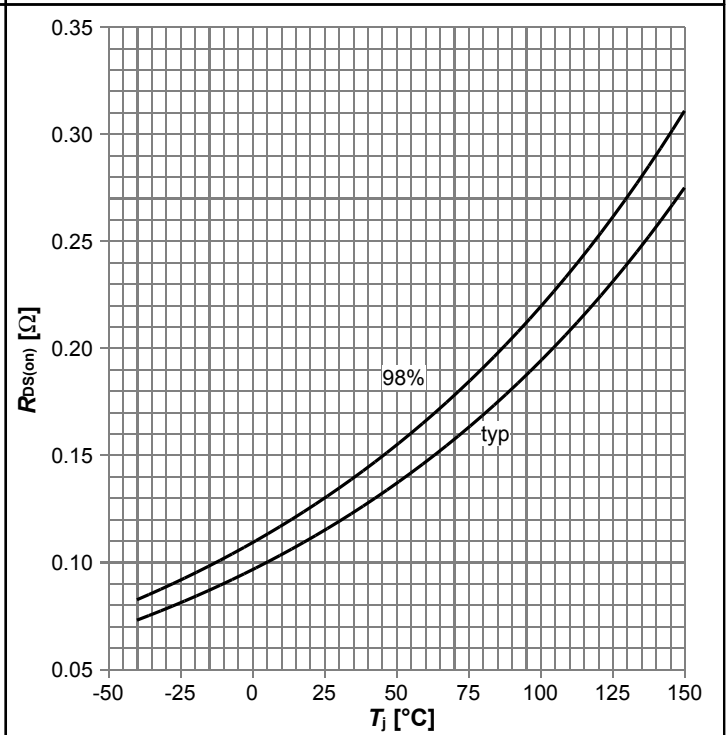
$I_D=f(V_{DS}); T_j=125\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

**Diagram 7: Typ. drain-source on-state resistance**



$R_{DS(on)}=f(I_D); T_j=125\text{ }^\circ\text{C};$  parameter:  $V_{GS}$

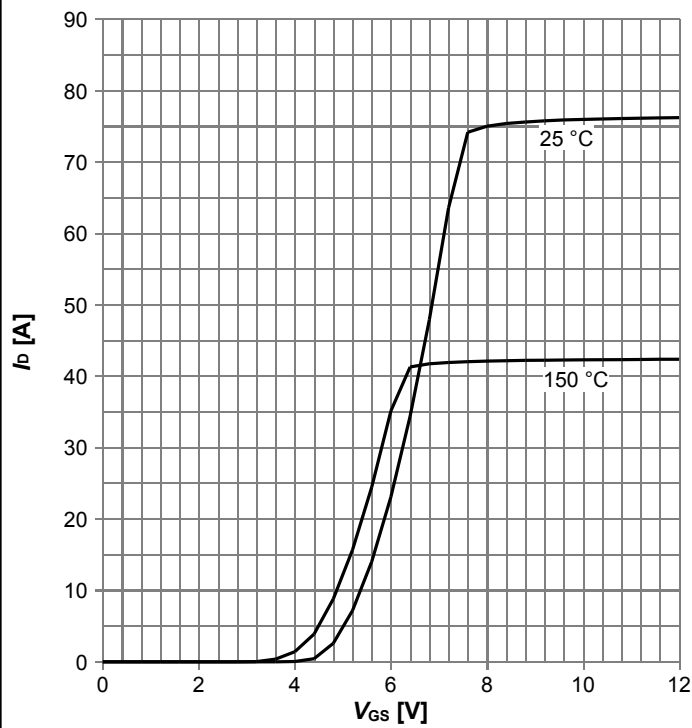
**Diagram 8: Drain-source on-state resistance**



$R_{DS(on)}=f(T_j); I_D=4.4\text{ A}; V_{GS}=10\text{ V}$

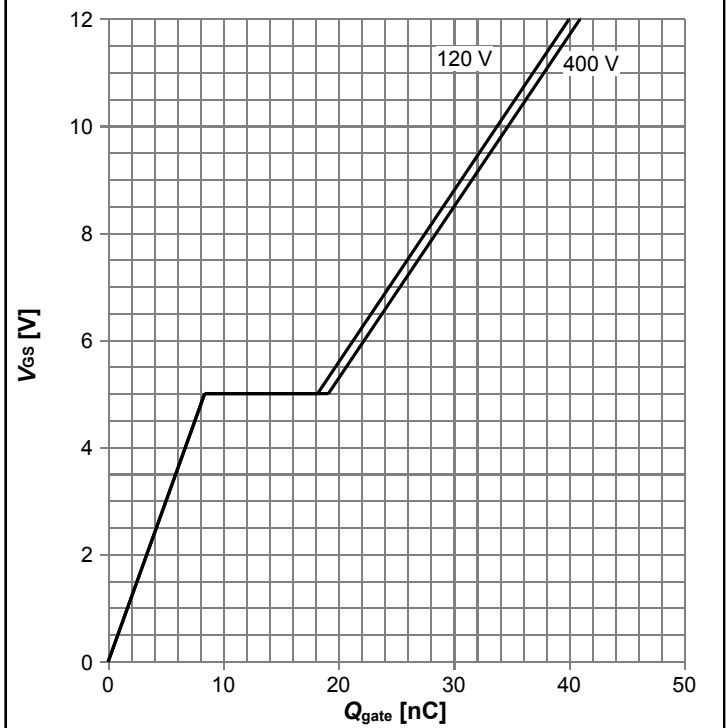


**Diagram 9: Typ. transfer characteristics**



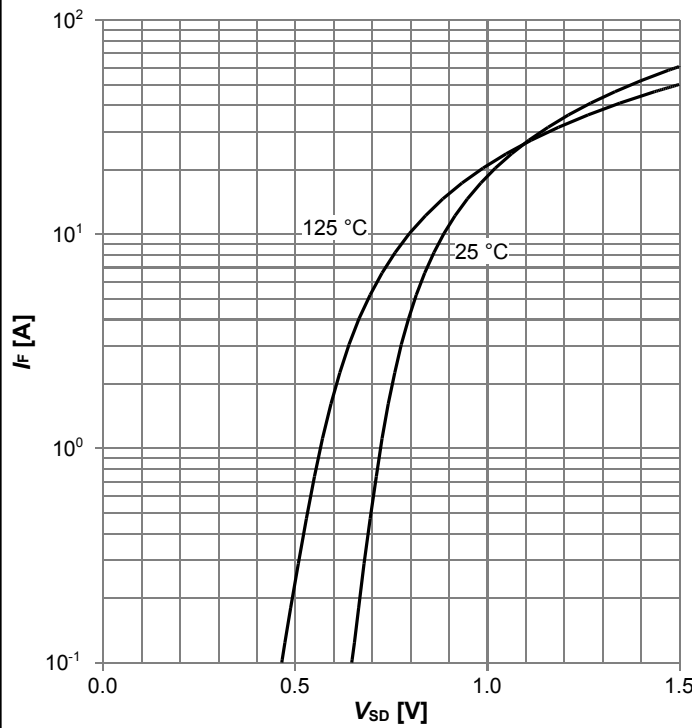
$I_D = f(V_{GS}); V_{DS} = 20V; \text{parameter: } T_j$

**Diagram 10: Typ. gate charge**



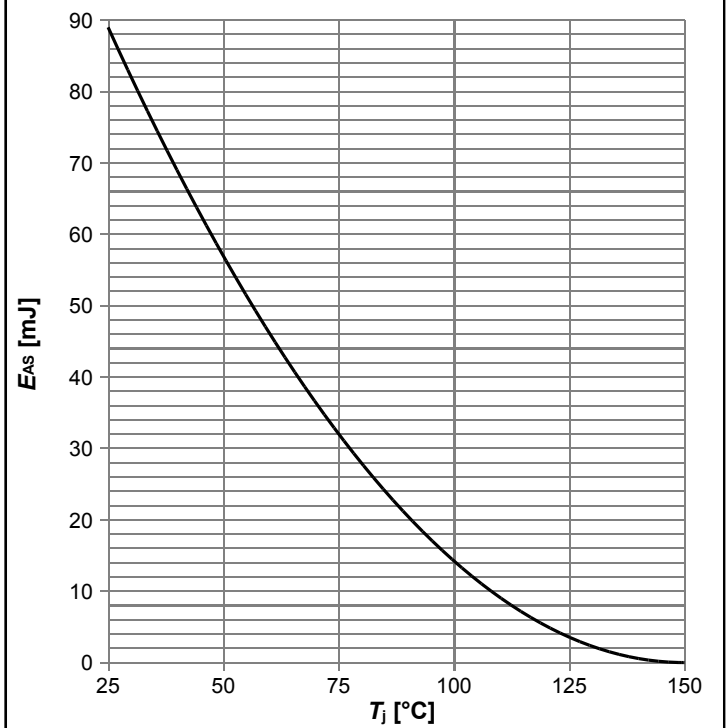
$V_{GS} = f(Q_{gate}); I_D = 4.4 \text{ A pulsed}; \text{parameter: } V_{DD}$

**Diagram 11: Forward characteristics of reverse diode**



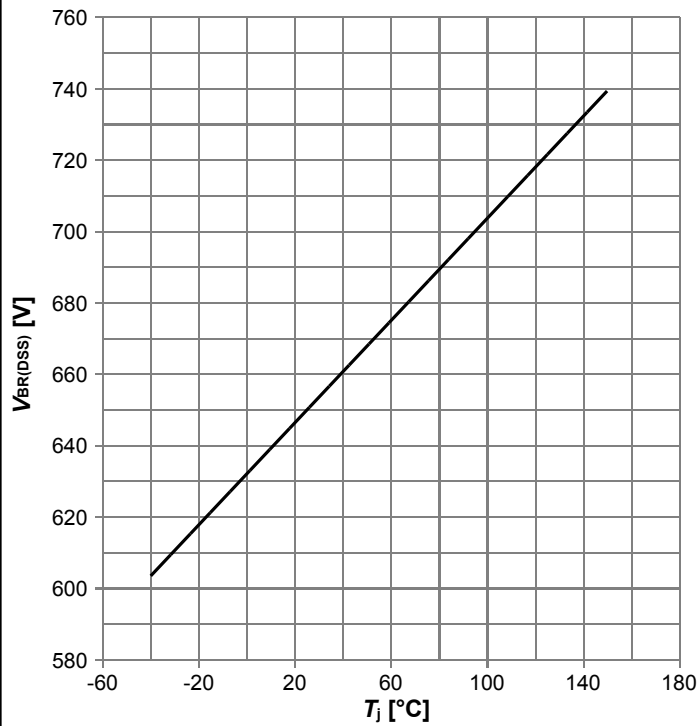
$I_F = f(V_{SD}); \text{parameter: } T_j$

**Diagram 12: Avalanche energy**



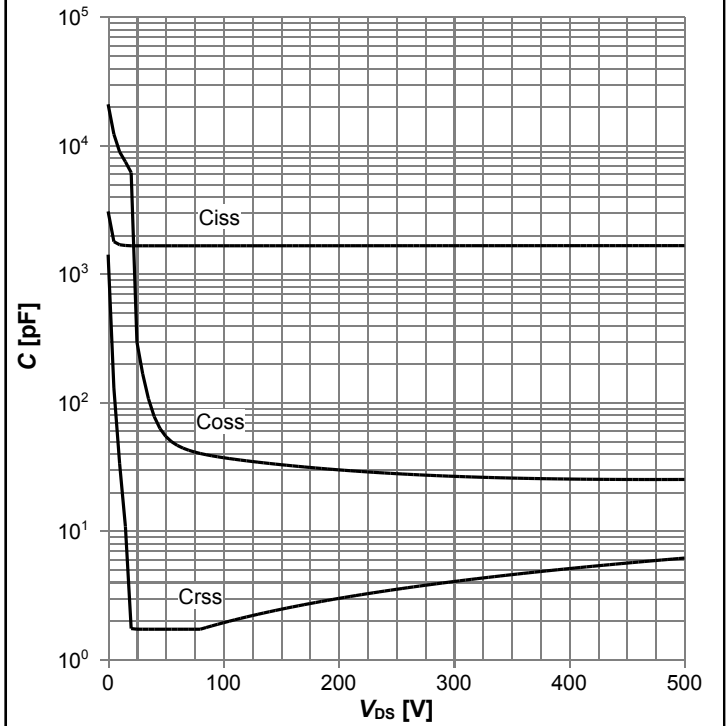
$E_{AS} = f(T_j); I_D = 7.1 \text{ A}; V_{DD} = 50 \text{ V}$

**Diagram 13: Drain-source breakdown voltage**



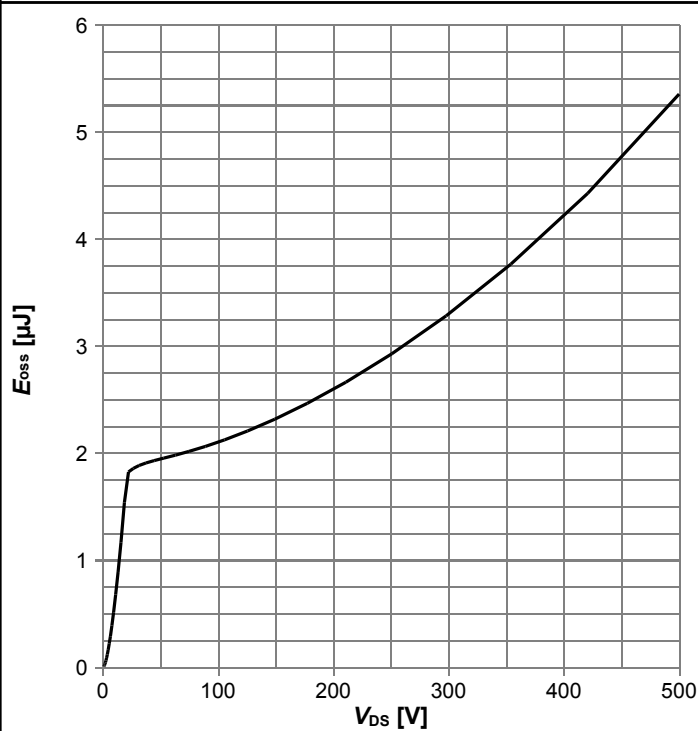
$V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$

**Diagram 14: Typ. capacitances**



$C=f(V_{DS}); V_{GS}=0\text{ V}; f=250\text{ kHz}$

**Diagram 15: Typ. Coss stored energy**



$E_{oss}=f(V_{DS})$

## 5 Test Circuits

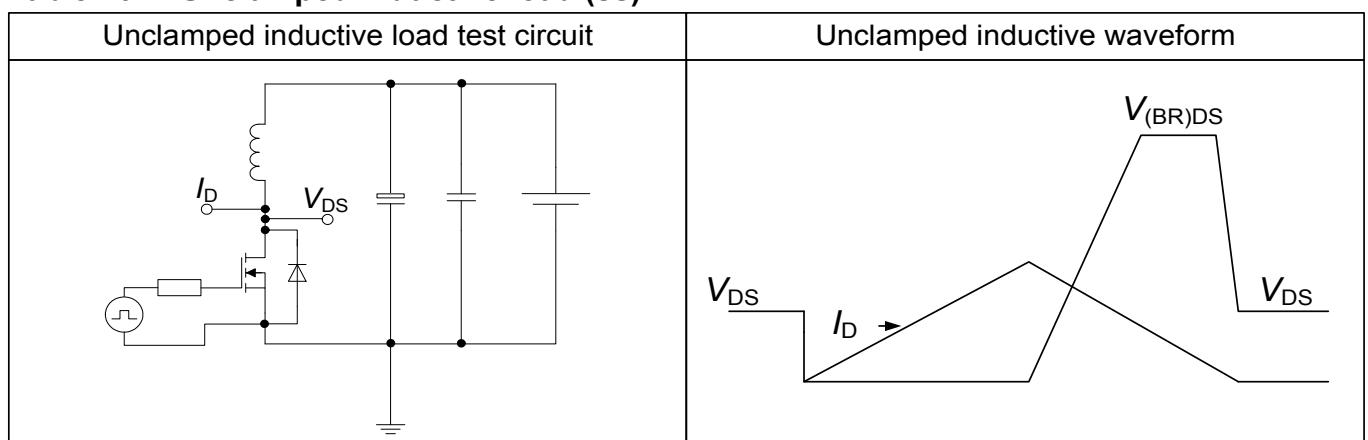
**Table 8 Diode characteristics**



**Table 9 switching times (ss)**



**Table 10 Unclamped inductive load (ss)**



## 6 Package Outlines



**Figure 1 Outline PG-VSON-4, dimensions in mm/inches**

## 7 Appendix A

### Table 11 Related Links

- IFX CoolMOS™ C7 Webpage: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ C7 application note: [www.infineon.com](http://www.infineon.com)
- IFX CoolMOS™ C7 simulation model: [www.infineon.com](http://www.infineon.com)
- IFX Design tools: [www.infineon.com](http://www.infineon.com)

### Revision History

IPL65R130C7

**Revision: 2017-08-29, Rev. 2.1**

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2013-04-29	Release of final version
2.1	2017-08-29	Updated MSL; style updated

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