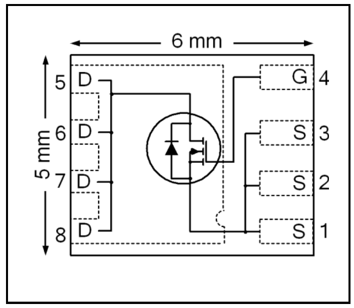
V_{DSS}	**25**	**V**
$R_{DS(on)}$ **max** (@ V_{GS} = 10V)	**0.95**	**mΩ**
(@ V_{GS} = 4.5V)	**1.60**	
Qg (typical)	**56**	**nC**
I_D (@$T_{C\ (Bottom)}$ = 25°C)	**324**	**A**



PQFN 5X6 mm

Applications
- OR-ing MOSFET for 12V (typical) Bus in-Rush Current
- Battery Operated DC Motor Inverters

Features		**Benefits**
Low R_{DSon} (<0.95mΩ)		Lower Conduction Losses
Low Thermal Resistance to PCB (<0.8°C/W)		Enable better thermal dissipation
Low Profile (<0.9 mm)	results in	Increased Power Density
Industry-Standard Pinout	⇒	Multi-Vendor Compatibility
Compatible with Existing Surface Mount Techniques		Easier Manufacturing
RoHS Compliant, Halogen-Free		Environmentally Friendlier
MSL1, Industrial Qualification		Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH8201PbF	PQFN 5mm x 6 mm	Tape and Reel	4000	IRFH8201TRPbF

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D @ T_A = 25°C	Continuous Drain Current, V_{GS} @ 10V	49	A
I_D @ $T_{C\ (Bottom)}$ = 25°C	Continuous Drain Current, V_{GS} @ 10V ⑤	324	
I_D @ $T_{C\ (Bottom)}$ = 100°C	Continuous Drain Current, V_{GS} @ 10V ⑤	205	
I_{DM}	Pulsed Drain Current	1296	
P_D @T_A = 25°C	Power Dissipation ④	3.6	W
P_D @$T_{C\ (Bottom)}$ = 25°C	Power Dissipation ④	156	
	Linear Derating Factor ④	0.029	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑥ are on page 9

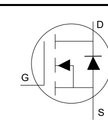
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	25	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	20	——	mV/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	0.80	0.95	mΩ	V_{GS} = 10V, I_D = 50A ②
		——	1.20	1.60		V_{GS} = 4.5V, I_D = 50A ②
$V_{GS(th)}$	Gate Threshold Voltage	1.35	1.80	2.35	V	V_{DS} = V_{GS}, I_D = 150μA
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	——	-6.1	——	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	——	——	1.0	μA	V_{DS} = 20V, V_{GS} = 0V
		——	——	150		V_{DS} = 20V, V_{GS} = 0V, T_J=125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
gfs	Forward Transconductance	181	——	——	S	V_{DS} = 10V, I_D = 50A
Q_g	Total Gate Charge	——	111	——	nC	V_{GS} = 10V, V_{DS} = 13V, I_D = 50A
Q_g	Total Gate Charge	——	56	84	nC	V_{DS} = 13V V_{GS} = 4.5V I_D = 50A
Q_{gs1}	Pre-Vth Gate-to-Source Charge	——	16	——		
Q_{gs2}	Post-Vth Gate-to-Source Charge	——	7.0	——		
Q_{gd}	Gate-to-Drain Charge	——	18	——		
Q_{godr}	Gate Charge Overdrive	——	15	——		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	——	25	——		
Q_{oss}	Output Charge	——	39	——	nC	V_{DS} = 16V, V_{GS} = 0V
R_G	Gate Resistance	——	1.1	——	Ω	
$t_{d(on)}$	Turn-On Delay Time	——	27	——	ns	V_{DD} = 13V, V_{GS} = 4.5V I_D = 50A R_G=4.7Ω
t_r	Rise Time	——	54	——		
$t_{d(off)}$	Turn-Off Delay Time	——	31	——		
t_f	Fall Time	——	22	——		
C_{iss}	Input Capacitance	——	7330	——	pF	V_{GS} = 0V V_{DS} = 13V f = 1.0MHz
C_{oss}	Output Capacitance	——	1730	——		
C_{rss}	Reverse Transfer Capacitance	——	850	——		

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy ①	——	437	mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	156	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	——	——	1296		
V_{SD}	Diode Forward Voltage	——	——	1.0	V	T_J = 25°C, I_S = 50A, V_{GS} = 0V ②
t_{rr}	Reverse Recovery Time	——	25	38	ns	T_J = 25°C, I_F = 50A, V_{DD} = 13V
Q_{rr}	Reverse Recovery Charge	——	57	86	nC	di/dt = 400A/μs ②

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ③	0.5	0.8	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ③	——	21	
$R_{\theta JA}$	Junction-to-Ambient ④	——	35	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ④	——	20	

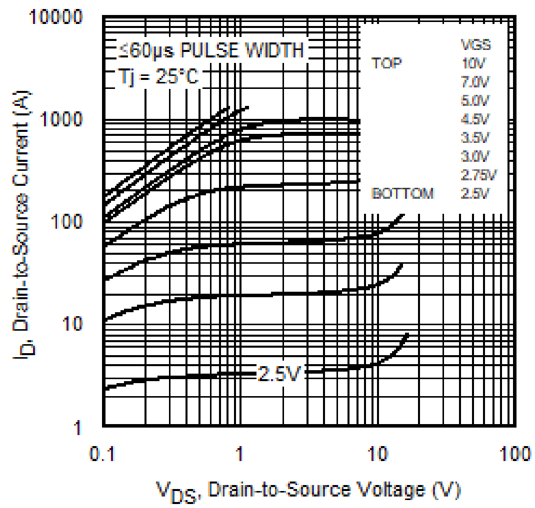


Fig 1. Typical Output Characteristics

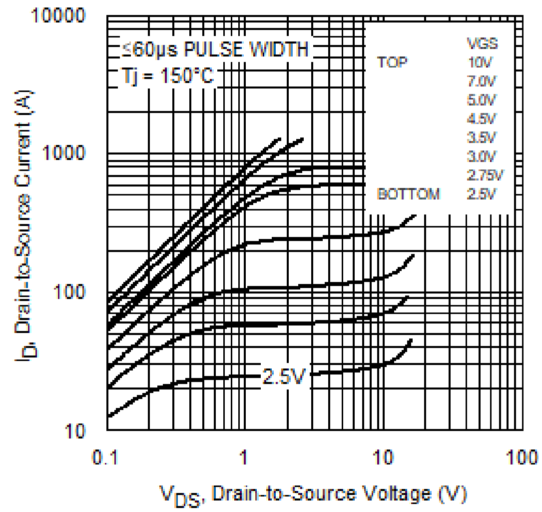


Fig 2. Typical Output Characteristics

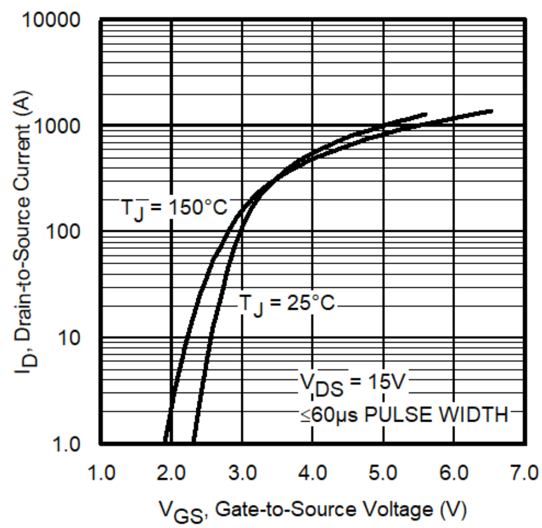


Fig 3. Typical Transfer Characteristics

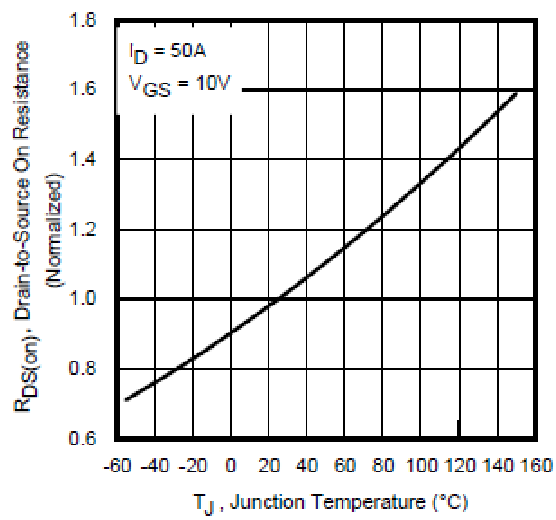


Fig 4. Normalized On-Resistance vs. Temperature

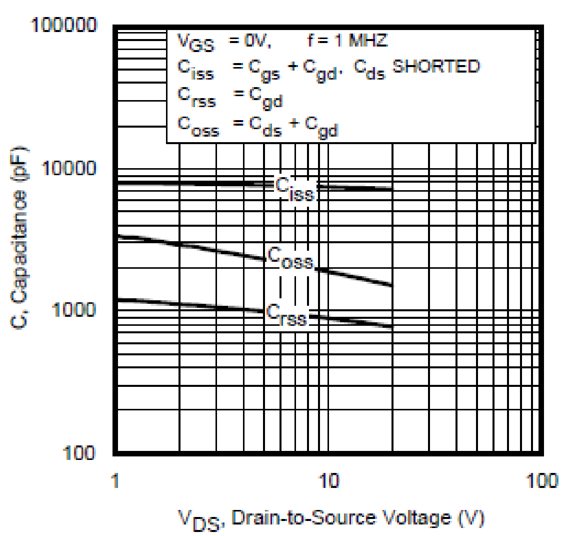


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

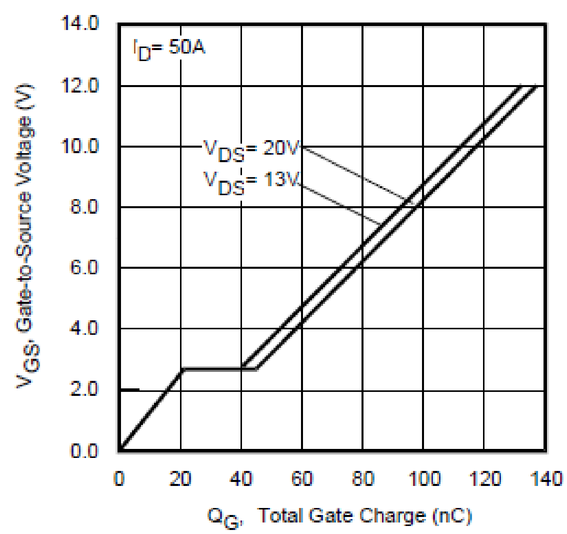


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

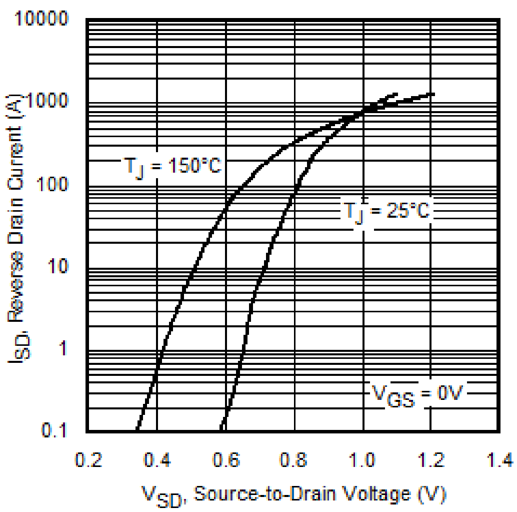


Fig 7. Typical Source-Drain Diode Forward Voltage

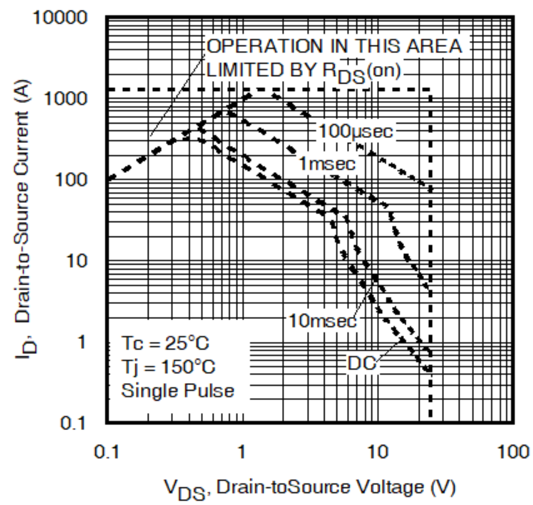


Fig 8. Maximum Safe Operating Area

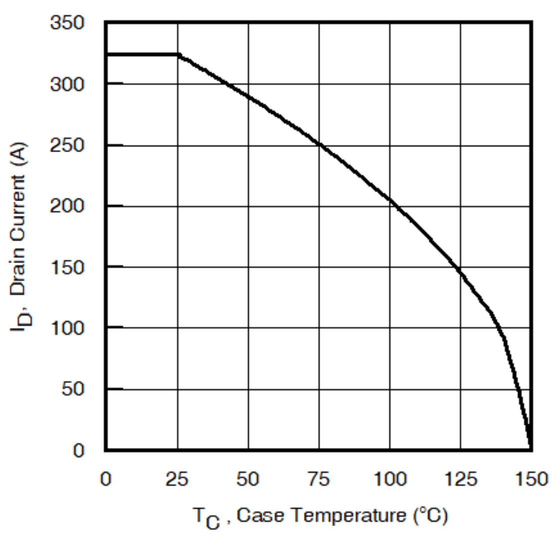


Fig 9. Maximum Drain Current vs. Case Temperature

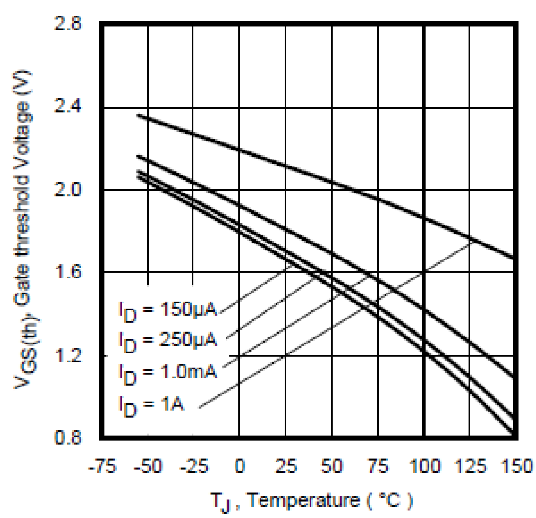


Fig 10. Threshold Voltage Vs. Temperature

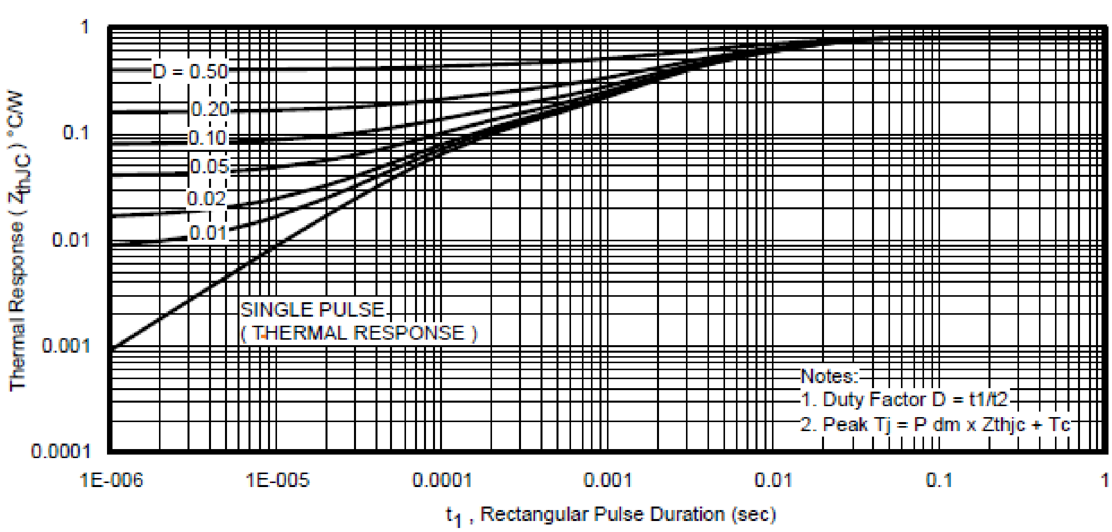


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

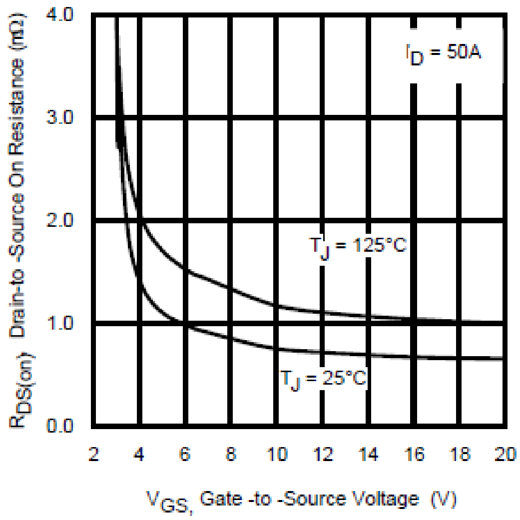


Fig 12. On– Resistance vs. Gate Voltage

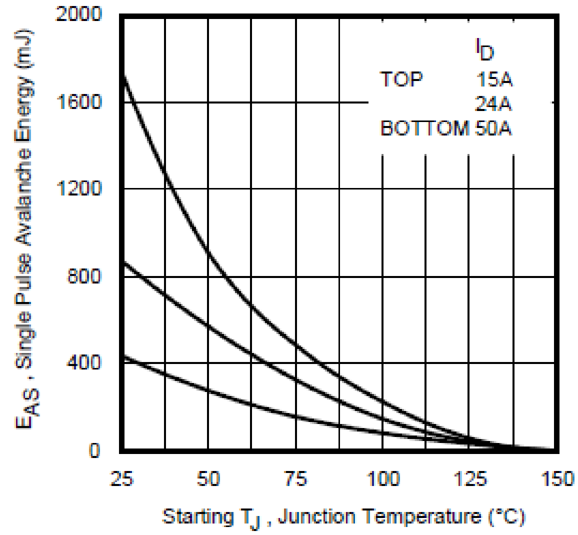


Fig 13. Maximum Avalanche Energy vs. Drain Current

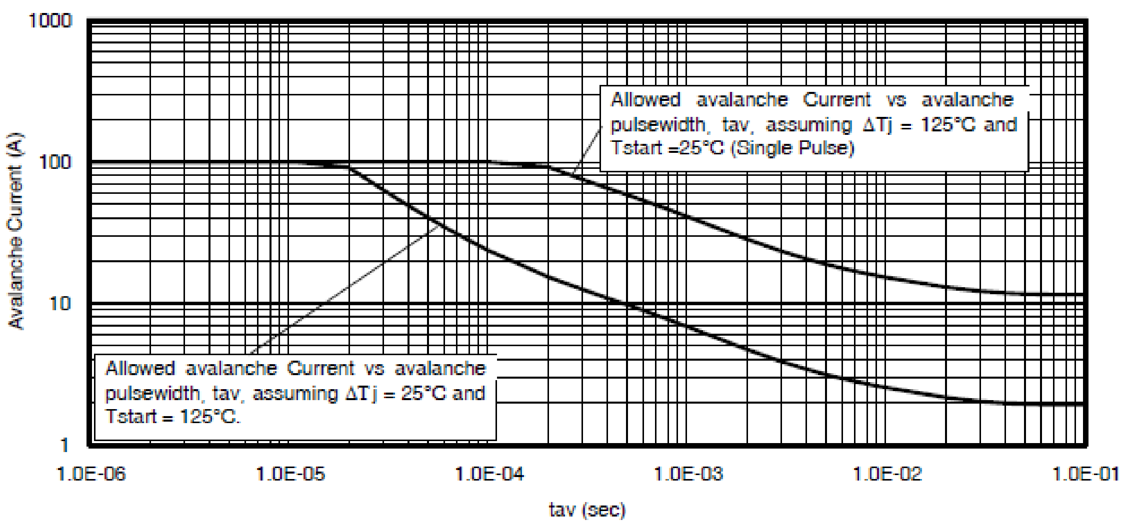


Fig 14. Single Avalanche Event: Pulse Current vs. Pulse Width

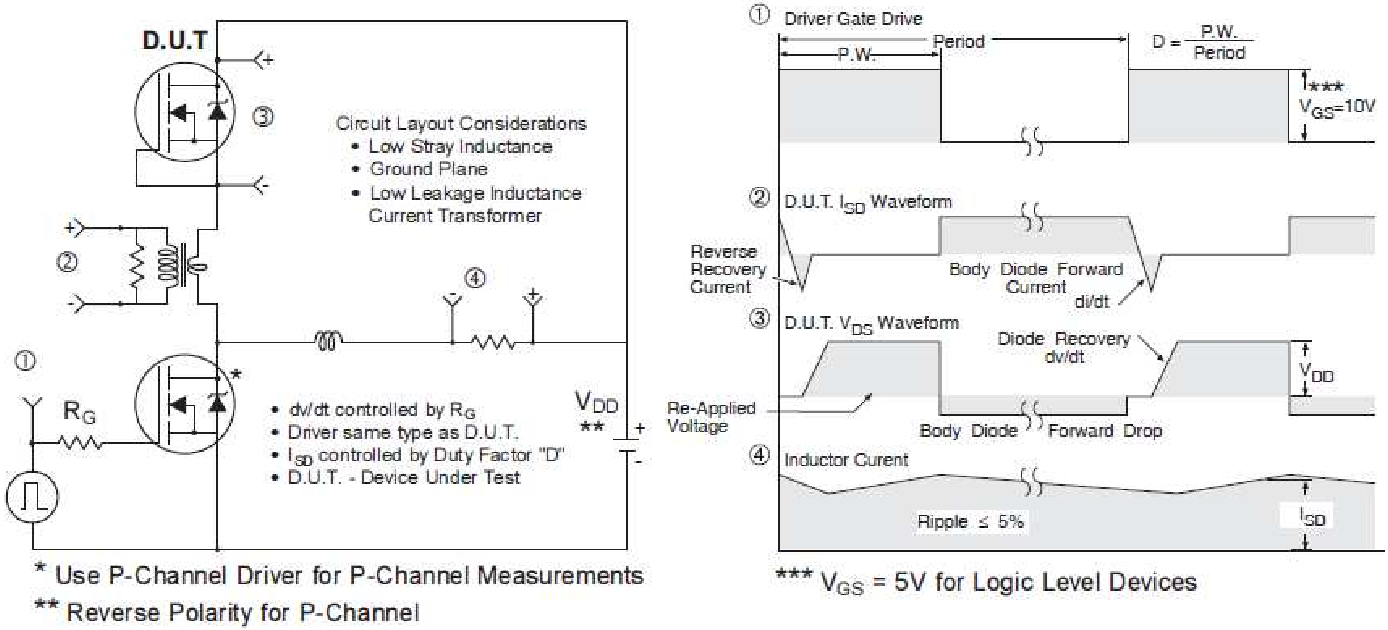


Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

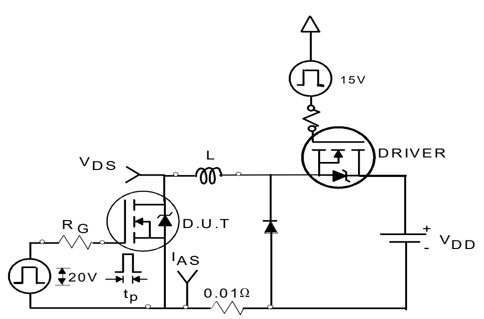


Fig 16a. Unclamped Inductive Test Circuit

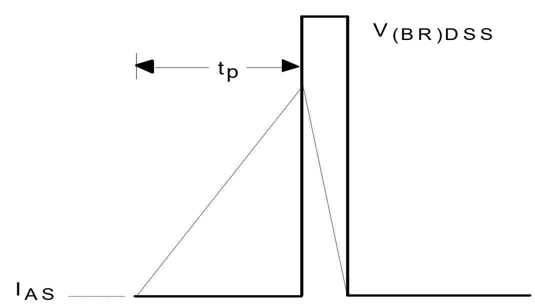


Fig 16b. Unclamped Inductive Waveforms

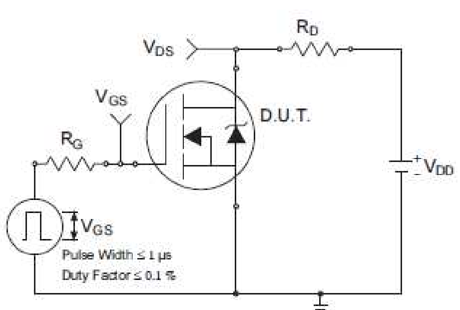


Fig 17a. Switching Time Test Circuit

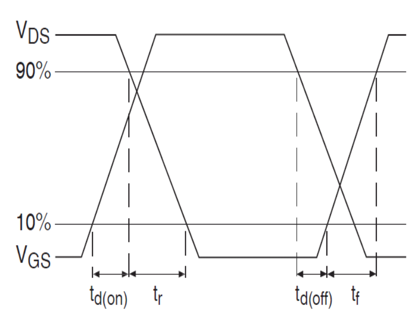


Fig 17b. Switching Time Waveforms

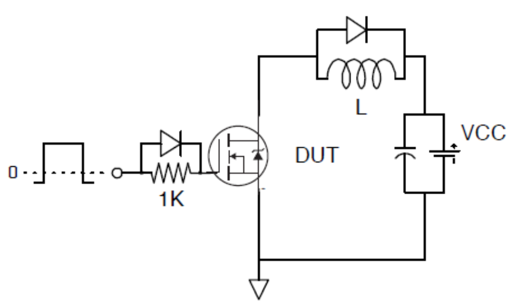


Fig 18a. Gate Charge Test Circuit

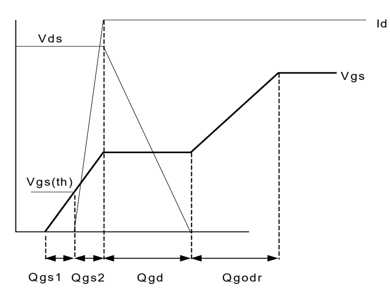
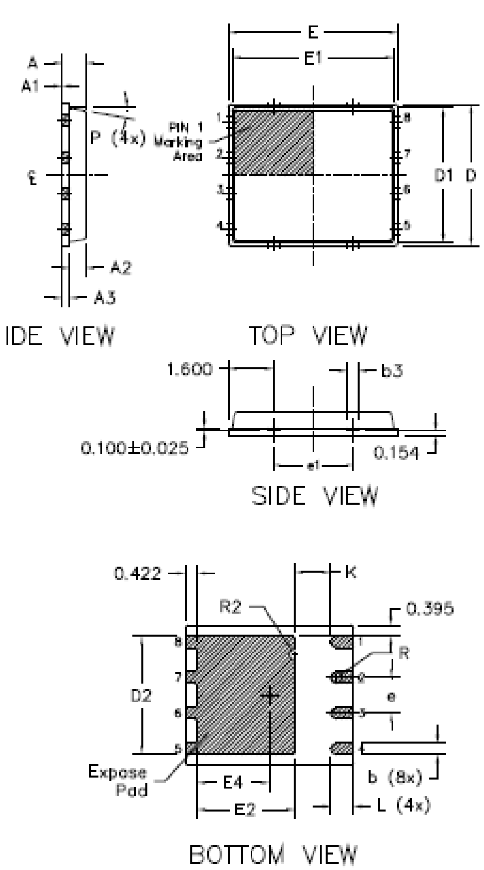


Fig 18b. Gate Charge Waveform

PQFN 5x6 Outline "B" Package Details



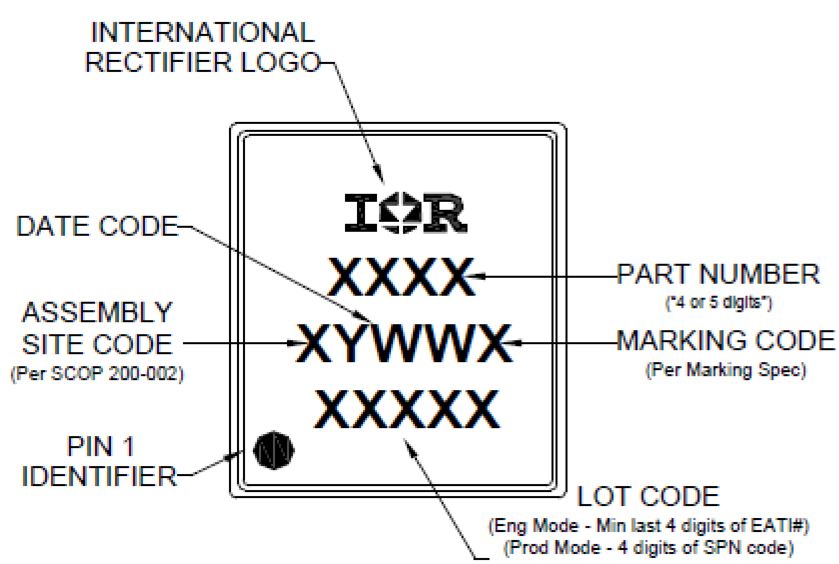
DIM / SYMBOL	MILLIMITERS		INCH	
	MIN	MAX	MIN	MAX
A	0.800	0.900	0.0315	0.0543
A1	0.000	0.050	0.0000	0.0020
A3	0.200 REF		0.0079 REF	
b	0.350	0.470	0.0138	0.0185
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.150	0.450	0.0059	0.0177
D	5.000 BSC		0.1969 BSC	
D1	4.750 BSC		0.1870 BSC	
D2	4.100	4.300	0.1614	0.1693
E	6.000 BSC		0.2362 BSC	
E1	5.750 BSC		0.2264 BSC	
E2	3.380	3.780	0.1331	0.1488
e	1.270 REF		0.0500 REF	
e1	2.800 REF		0.1102 REF	
K	1.200	1.420	0.0472	0.0559
L	0.710	0.900	0.0280	0.0354
P	0°	12°	0°	12°
R	0.200 REF		0.0079 REF	
R2	0.150	0.200	0.0059	0.0079

Note:

1. Dimensions and toleranceing confirm to ASME Y14.5M-1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: http://www.irf.com/technical-info/appnotes/an-1136.pdf
For more information on package inspection techniques, please refer to application note AN-1154: http://www.irf.com/technical-info/appnotes/an-1154.pdf

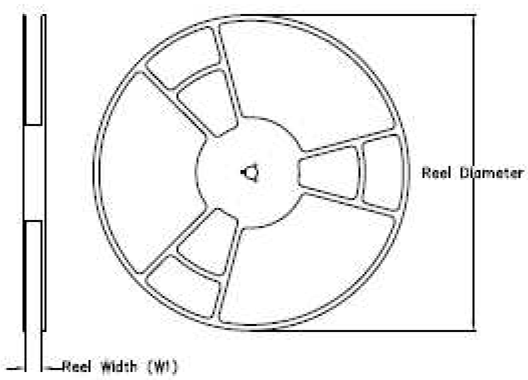
PQFN 5x6 Part Marking



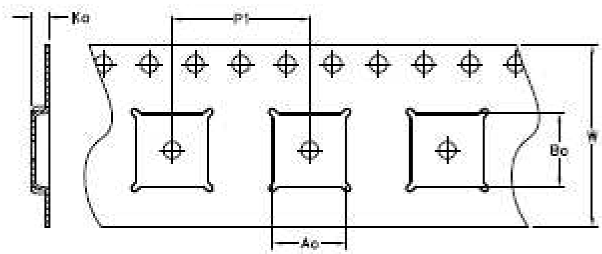
Note: For the most current drawing please refer to IR website at http://www.irf.com/packaging

PQFN 5x6 Tape and Reel

REEL DIMENSIONS

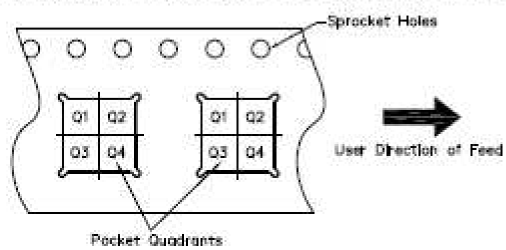


TAPE DIMENSIONS



CODE	DESCRIPTION
Ao	Dimension design to accommodate the component width
Bo	Dimension design to accommodate the component lenght
Ko	Dimension design to accommodate the component thickness
W	Overall width of the carrier tape
P_1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

Note: For the most current drawing please refer to IR website at http://www.irf.com/packaging

Qualifiction Information†

Qualification Level	Industrial (per JEDEC JESD47F† guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D†)
RoHS Compliant	Yes	

† Applicable version of JEDEC standard at the time of product release.

Notes:

① Starting T_J = 25°C, L = 0.35mH, R_G = 50Ω, I_{AS} = 50A.

② Pulse width ≤ 400µs; duty cycle ≤ 2%.

③ R_θ is measured at T_J of approximately 90°C.

④ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details: http://www.irf.com/technical-info/appnotes/an-994.pdf

⑤ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature at 25°C. For higher case temperature please refer to Diagram 9. De-rating will be required based on the actual environmental conditions.

Revision History

Date	Rev.	Comments
10/23/2013	2.1	• Added Rdson @ 4.5V-page1, 2
7/30/2014	2.2	• Updated IDM from "400A" to "700A" on page1, 2. • Updated Fig1, Fig2, Fig3, Fig7 & Fig8 on page 3, 4.
3/11/2015	2.3	• Updated package outline and tape and reel on pages 7 and 8.
12/14/2020	2.4	• Updated datasheet based on IFX template. • Updated Datasheet based on new current rating and application note : App-AN_1912_PL51_2001_180356 • Removed "HEXFET® Power MOSFET" -page1

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