ALPHA & OMEGA SEMICONDUCTOR

AON6450

100V N-Channel MOSFET SDMOS™

General Description

The AON6450 is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge.The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

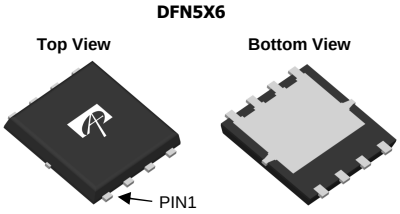
Product Summary

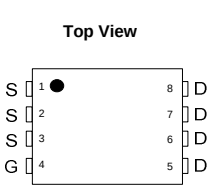
V_{DS}	100V
I_D (at V_{GS}=10V)	52A
$R_{DS(ON)}$ (at V_{GS}=10V)	< 14.5mΩ
$R_{DS(ON)}$ (at V_{GS} = 7V)	< 17.5mΩ

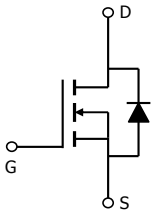
100% UIS Tested
100% R_g Tested

Green Product

DFN5X6







Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	100	V
Gate-Source Voltage		V_{GS}	±25	V
Continuous Drain Current	T_C=25°C	I_D	52	A
	T_C=100°C		33	
Pulsed Drain Current [C]		I_{DM}	110	
Continuous Drain Current	T_A=25°C	I_{DSM}	9	A
	T_A=70°C		7	
Avalanche Current [C]		I_{AR}	41	A
Repetitive avalanche energy L=0.1mH [C]		E_{AR}	84	mJ
Power Dissipation [B]	T_C=25°C	P_D	83	W
	T_C=100°C		33	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.3	W
	T_A=70°C		1.4	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	14	17	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		40	55	°C/W
Maximum Junction-to-Case	Steady-State	$R_{\theta JC}$	1	1.5	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	100			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=100V, V_{GS}=0V			10	µA
		T_J=55°C			50	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±25V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	2.8	3.3	3.8	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	110			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		12.1	14.5	mΩ
		T_J=125°C		22.8	27.5	
		V_{GS}=7V, I_D=20A		14	17.5	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		52		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1	V
I_S	Maximum Body-Diode Continuous Current [G]				85	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=50V, f=1MHz	2000	2570	3100	pF
C_{oss}	Output Capacitance		170	250	330	pF
C_{rss}	Reverse Transfer Capacitance		50	80	120	pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.4	0.8	1.2	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=50V, I_D=20A	34	43	52	nC
Q_{gs}	Gate Source Charge		11	14	17	nC
Q_{gd}	Gate Drain Charge		8	13.5	19	nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=50V, R_L=2.5Ω, R_{GEN}=3Ω		15		ns
t_r	Turn-On Rise Time			5		ns
$t_{D(off)}$	Turn-Off DelayTime			28.5		ns
t_f	Turn-Off Fall Time			5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=500A/µs	17	24	31	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=500A/µs	75	108	140	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The Power dissipation P_{DSM} is based on $R_{\theta JA}$ and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J =25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

G. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

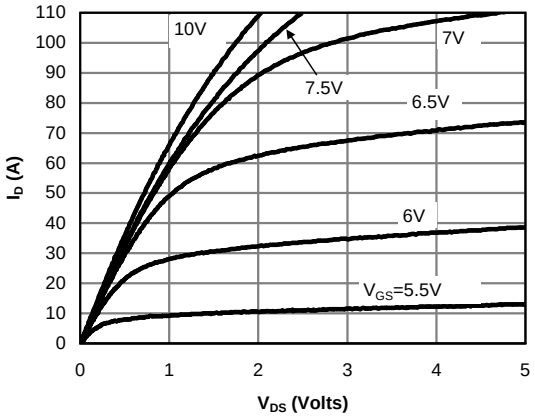


Fig 1: On-Region Characteristics (Note E)

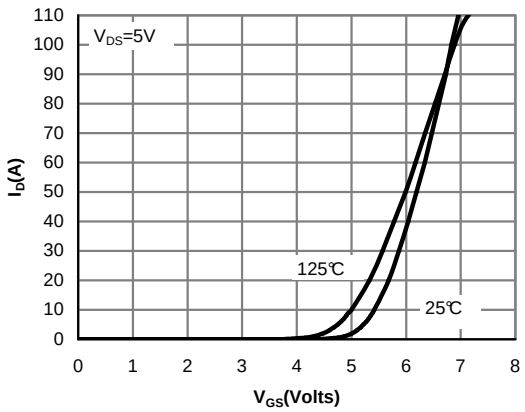


Figure 2: Transfer Characteristics (Note E)

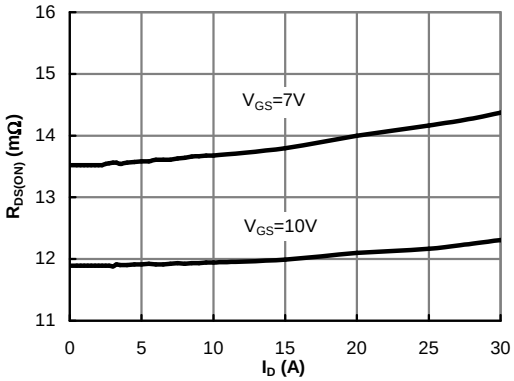


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

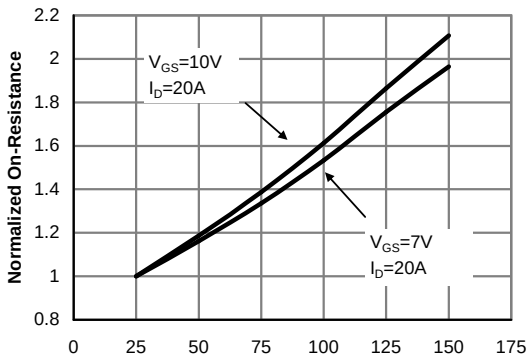


Figure 4: On-Resistance vs. Junction Temperature (Note E)

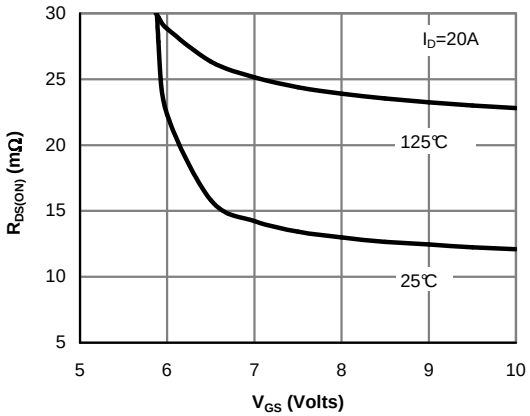


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

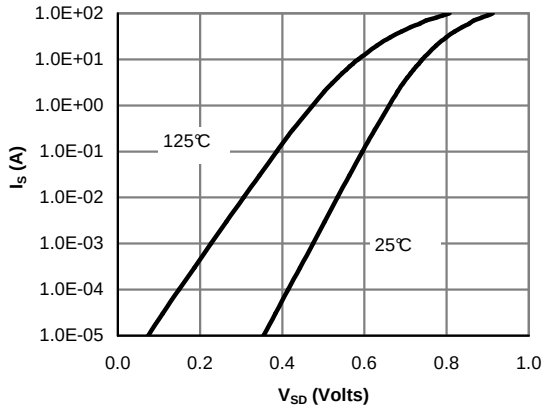


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

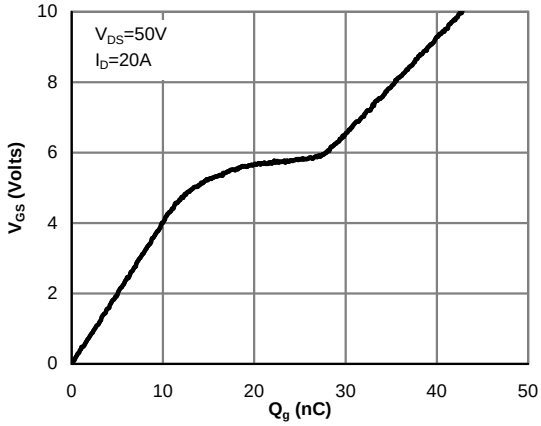


Figure 7: Gate-Charge Characteristics

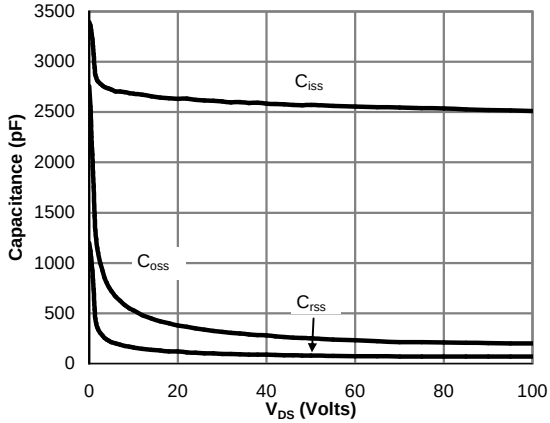


Figure 8: Capacitance Characteristics

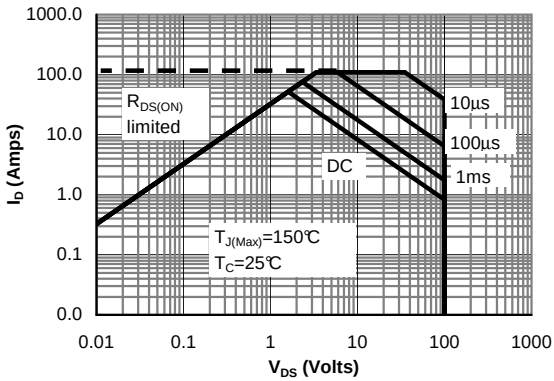


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

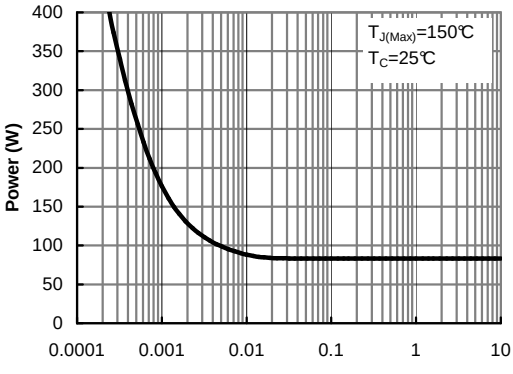


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

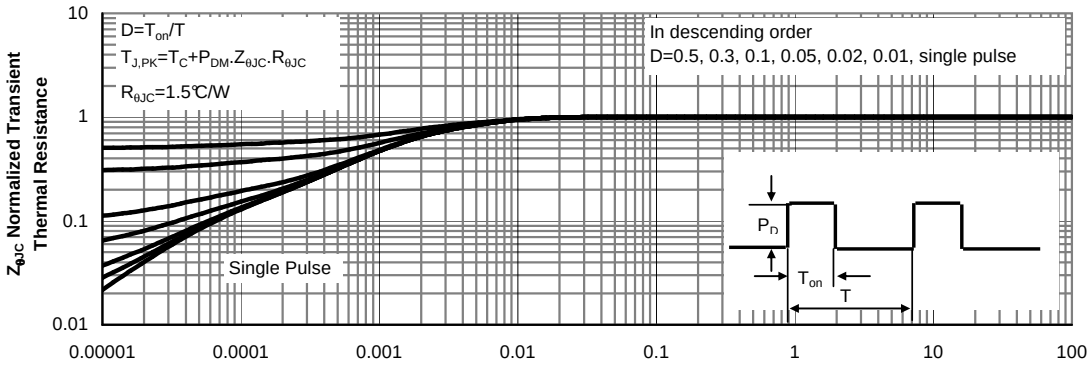


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

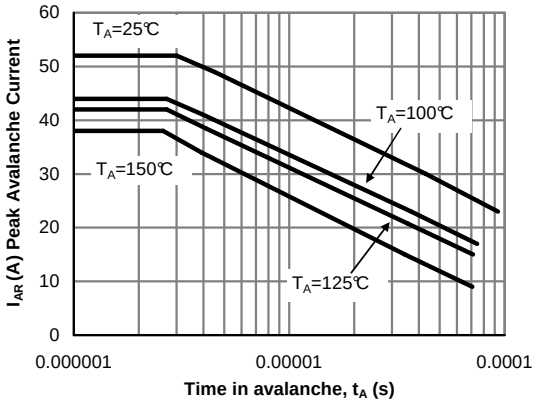


Figure 12: Single Pulse Avalanche capability (Note C)

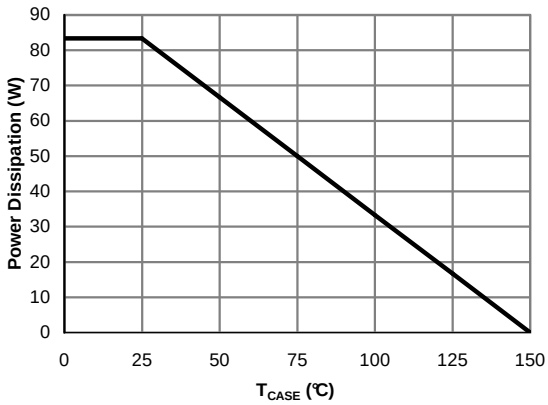


Figure 13: Power De-rating (Note F)

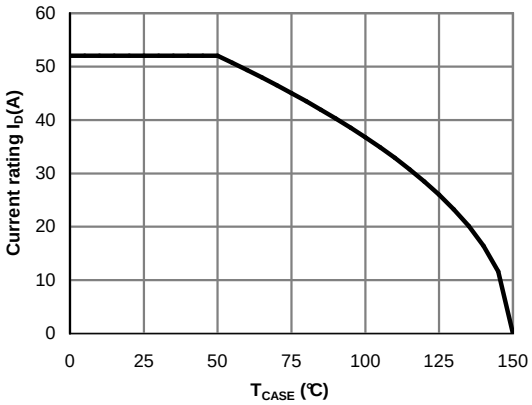


Figure 14: Current De-rating (Note F)

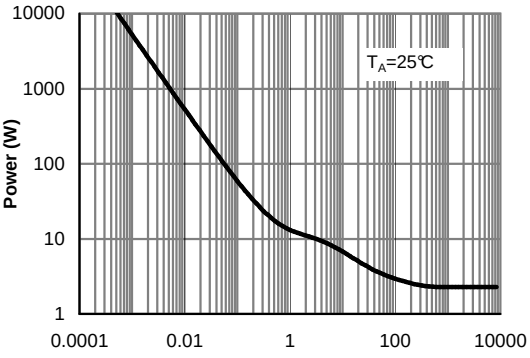


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note G)

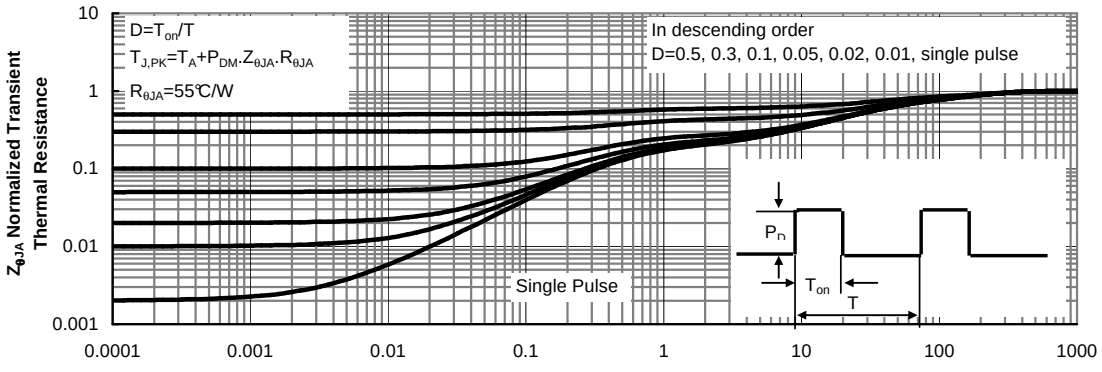


Figure 16: Normalized Maximum Transient Thermal Impedance (Note G)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

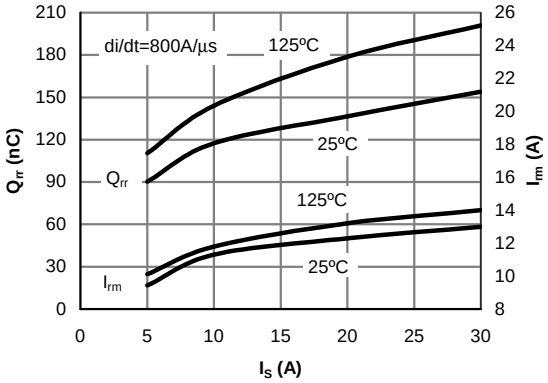


Figure 17: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

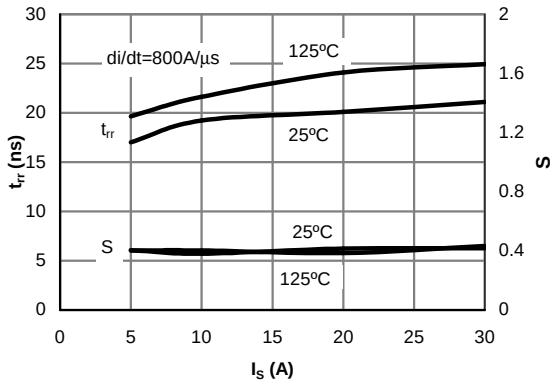


Figure 18: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

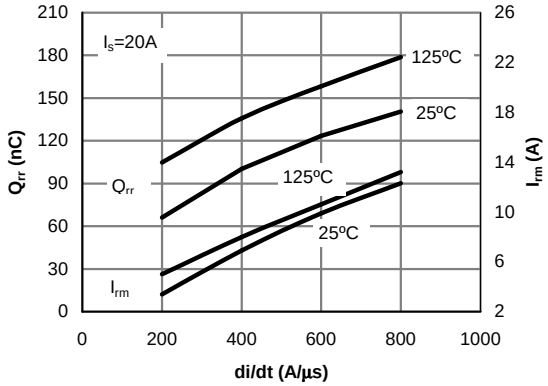


Figure 19: Diode Reverse Recovery Charge and Peak Current vs. di/dt

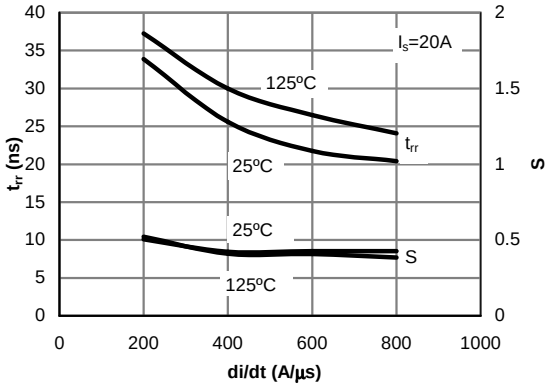
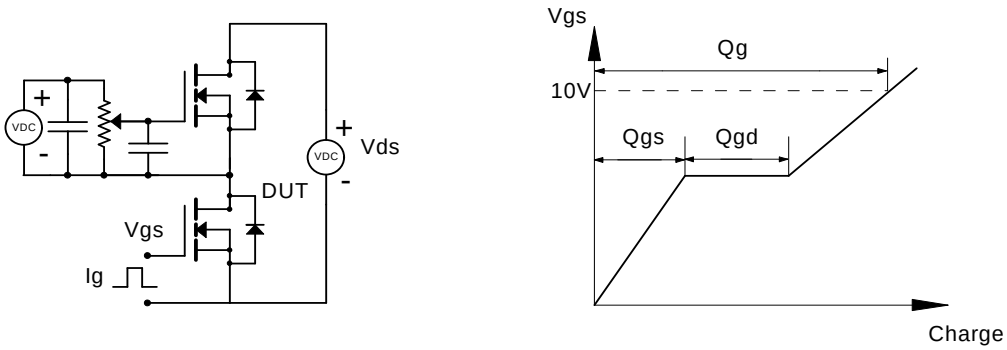
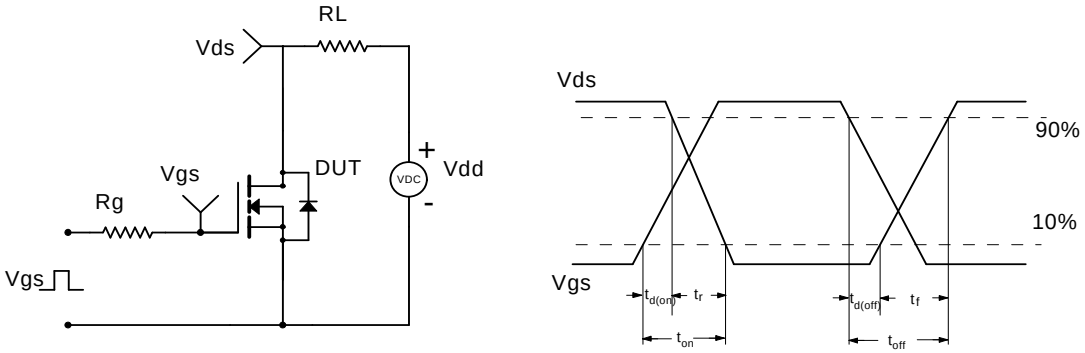


Figure 20: Diode Reverse Recovery Time and Softness Factor vs. di/dt

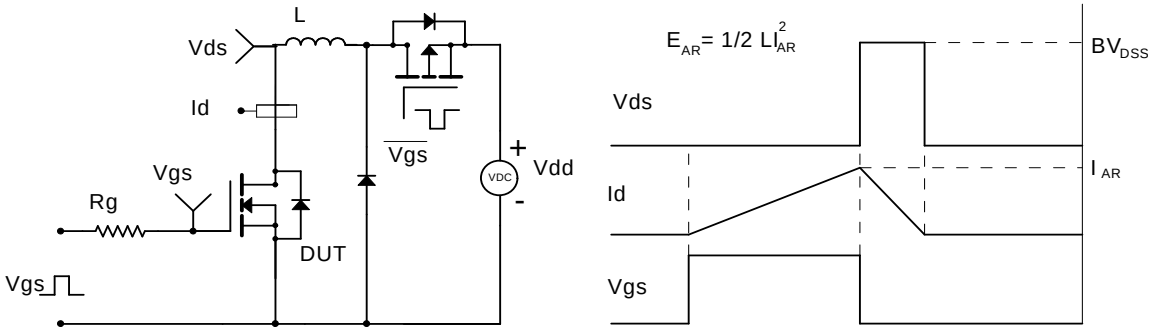
Gate Charge Test Circuit & Waveform



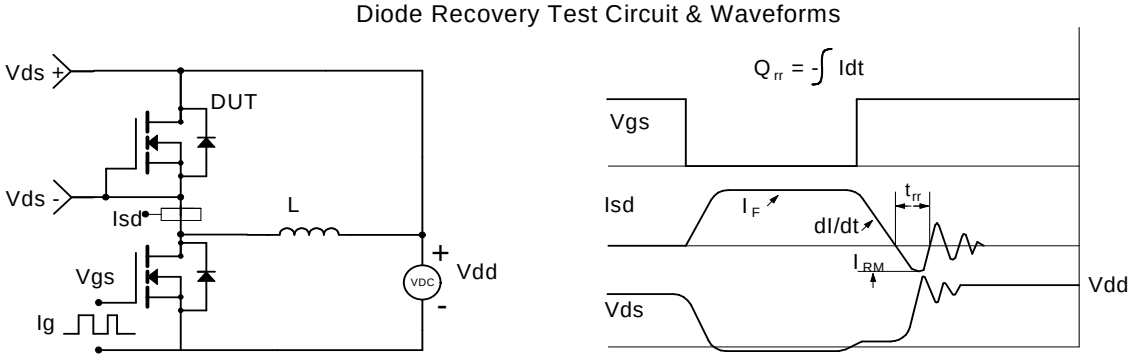
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



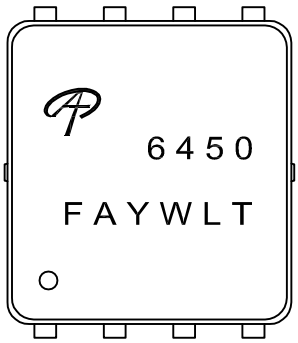
Diode Recovery Test Circuit & Waveforms



ALPHA & OMEGA SEMICONDUCTOR

Document No.	PD-00934
Version	B
Title	AON6450 Marking Description

DFN5X6 PACKAGE MARKING DESCRIPTION



Green product

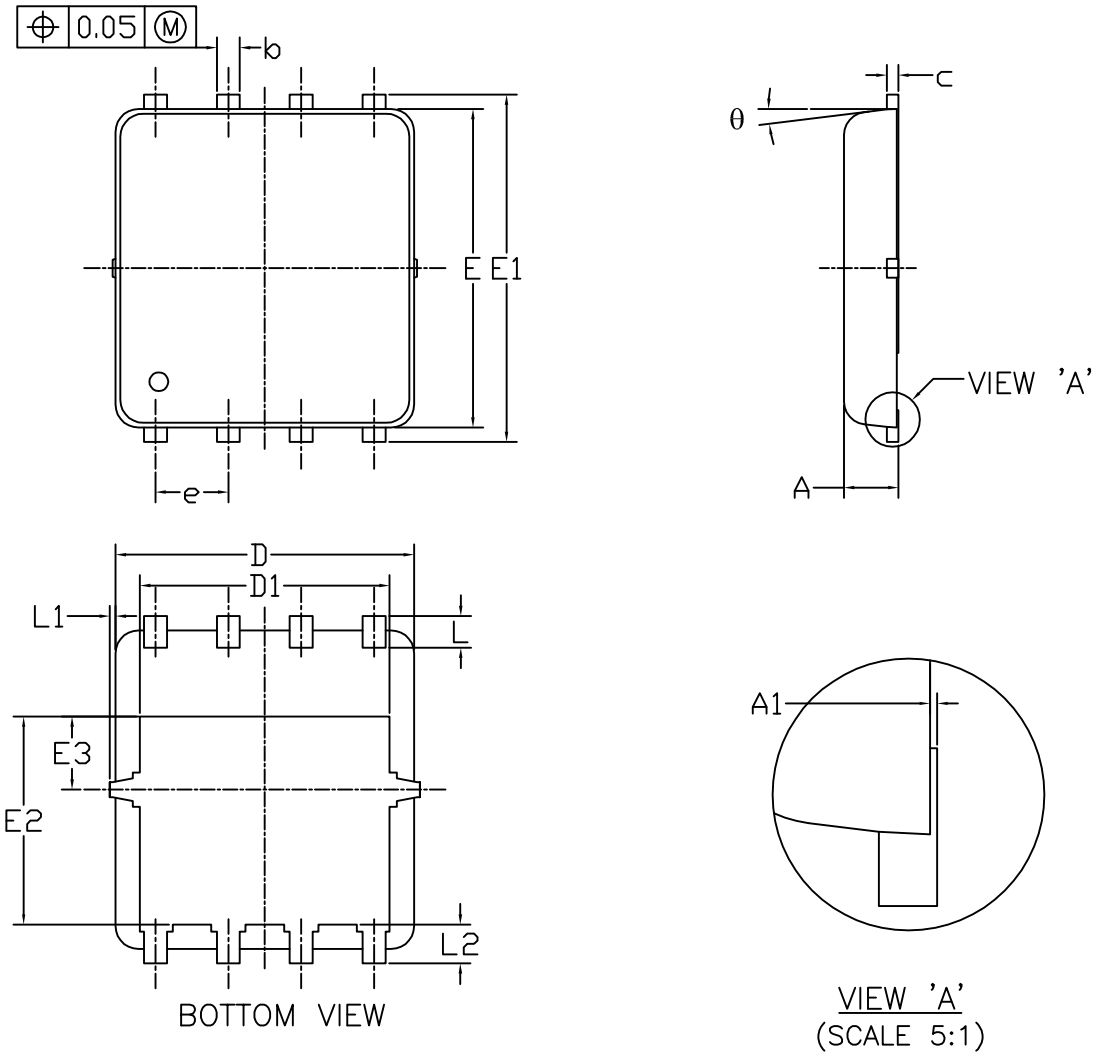
NOTE:
LOGO - AOS Logo
6450 - Part number code
F - Fab code
A - Assembly location code
Y - Year code
W - Week code
L&T - Assembly lot code

PART NO.	DESCRIPTION	CODE
AON6450	Green product	6450
AON6450L	Green product	6450

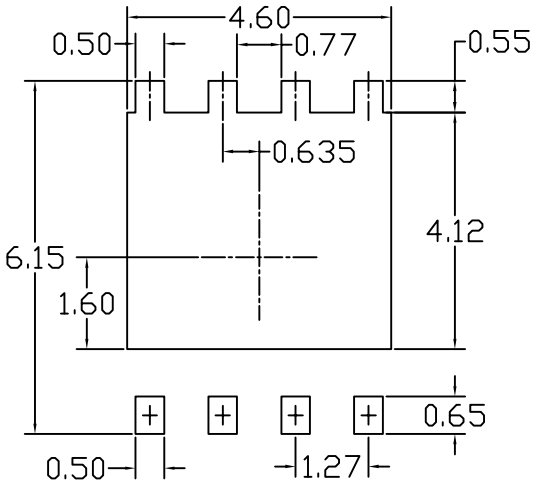
ALPHA & OMEGA SEMICONDUCTOR

Document No.	PO-00044
Version	F

DFN5x6_8L_EP1_P PACKAGE OUTLINE



RECOMMENDED LAND PATTERN



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.85	0.95	1.00	0.033	0.037	0.039
A1	0.00	---	0.05	0.000	---	0.002
b	0.30	0.40	0.50	0.012	0.016	0.020
c	0.15	0.20	0.25	0.006	0.008	0.010
D	5.10	5.20	5.30	0.201	0.205	0.209
D1	4.25	4.35	4.45	0.167	0.171	0.175
E	5.45	5.55	5.65	0.215	0.219	0.222
E1	5.95	6.05	6.15	0.234	0.238	0.242
E2	3.525	3.625	3.725	0.139	0.143	0.147
E3	1.175	1.275	1.375	0.046	0.050	0.054
e	1.27 BSC			0.050 BSC		
L	0.45	0.55	0.65	0.018	0.022	0.026
L1	0	---	0.15	0	---	0.006
L2	0.68 REF			0.027 REF		
θ	0°	---	10°	0°	---	10°

UNIT: mm

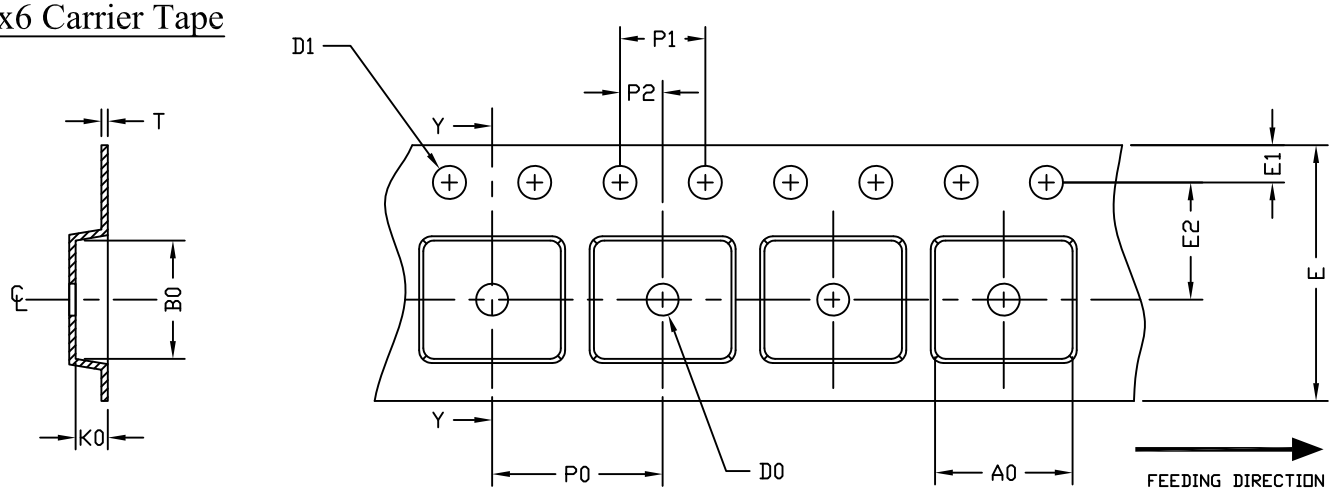
NOTE

1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 6 MILS EACH.
2. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

ALPHA & OMEGA SEMICONDUCTOR

DFN5x6 Tape and Reel Data

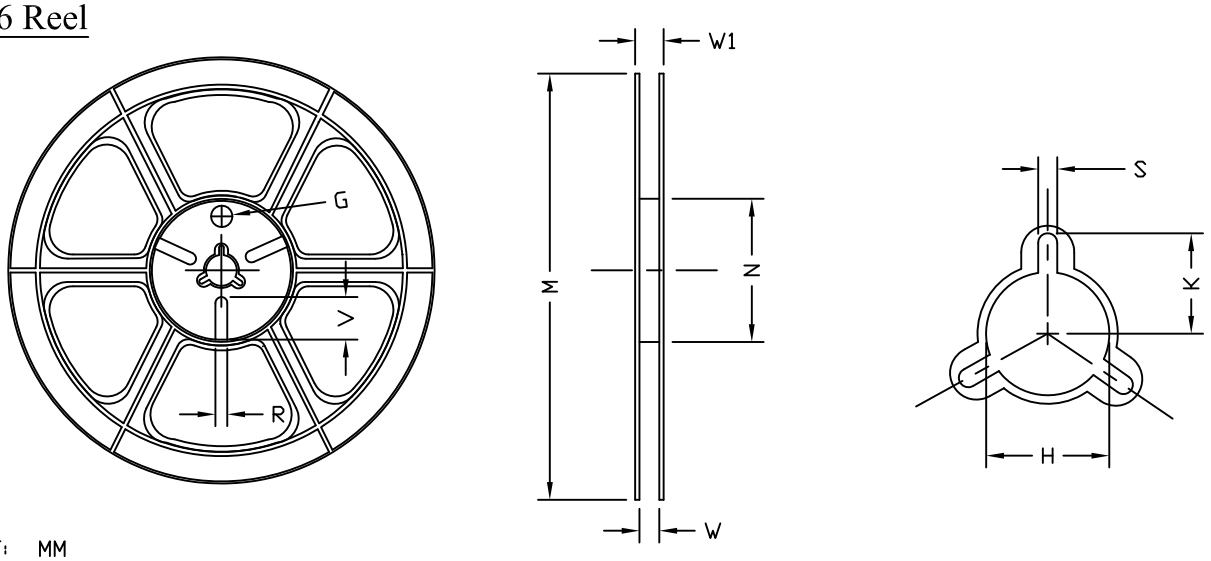
DFN5x6 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN5x6 (12 mm)	6.30 ±0.10	5.45 ±0.10	1.30 ±0.10	1.50 MIN.	1.55 ±0.05	12.00 ±0.30	1.75 ±0.10	5.50 ±0.10	8.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.30 ±0.05

DFN5x6 Reel



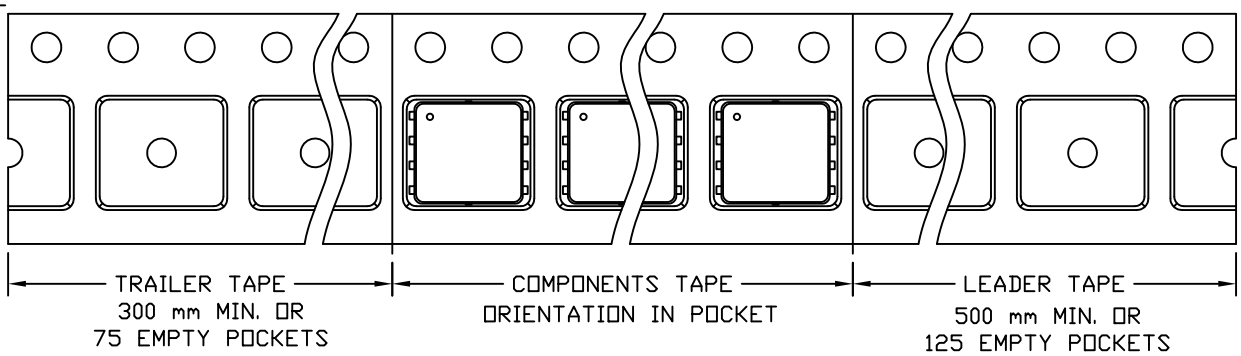
UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
12 mm	ø330	ø330.00 ±0.50	ø97.00 ±0.10	13.00 ±0.30	17.40 ±1.00	ø13.00 +0.50 −0.20	10.60	2.00 ±0.50	---	---	---

DFN5x6 Tape

Leader / Trailer & Orientation

Unit Per Reel: 3000pcs



ALPHA & OMEGA SEMICONDUCTOR

AOS Semiconductor
Product Reliability Report

AON6450L, rev A

Plastic Encapsulated Device

ALPHA & OMEGA Semiconductor, Inc

www.aosmd.com

This AOS product reliability report summarizes the qualification result for AON6450L. Accelerated environmental tests are performed on a specific sample size, and then followed by electrical test at end point. Review of final electrical test result confirms that AON6450L passes AOS quality and reliability requirements. The released product will be categorized by the process family and be monitored on a quarterly basis for continuously improving the product quality.

Table of Contents:

I. Product Description:

The AON6450L is fabricated with SDMOS^{TM} trench technology that combines excellent $R_{DS(ON)}$ with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

-RoHS Compliant
-Halogen Free

Detailed information refers to datasheet.

II. Die / Package Information:

	AON6450L
Process	Standard sub-micron Low voltage N channel
Package Type	DFN 5x6
Lead Frame	Copper
Die Attach	Solder paste
Bonding Wire	Copper clip
Mold Material	Epoxy resin with silica filler
MSL (moisture sensitive level)	Level 1 based on J-STD-020

Note * based on information provided by assembler and mold compound supplier

ALPHA & OMEGA SEMICONDUCTOR

III. Result of Reliability Stress for AON6450L

Test Item	Test Condition	Time Point	Lot Attribution	Total Sample size	Number of Failures	Standard
MSL Precondition	168hr 85℃ /85%RH +3 cycle reflow@260℃	-	11 lots	1815pcs	0	JESD22-A113
HTGB	Temp = 150 °c, Vgs=100% of Vgsmax	168hrs 500 hrs 1000 hrs	1 lot (Note A*)	77pcs 77pcs / lot	0	JESD22-A108
HTRB	Temp = 150 °c, Vds=80% of Vdsmax	168hrs 500 hrs 1000 hrs	1 lot (Note A*)	77pcs 77pcs / lot	0	JESD22-A108
HAST	130 +/- 2°c, 85%RH, 33.3 psi, Vgs = 80% of Vgs max	100 hrs	11 lots (Note A*)	605pcs 55pcs / lot	0	JESD22-A110
Pressure Pot	121°c, 29.7psi, RH=100%	96 hrs	11 lots (Note A*)	605pcs 55pcs / lot	0	JESD22-A102
Temperature Cycle	-65°c to 150°c, air to air	250 / 500 cycles	11 lots (Note A*)	605pcs 55pcs / lot	0	JESD22-A104

Note A: The reliability data presents total of available generic data up to the published date.

IV. Reliability Evaluation

FIT rate (per billion): 23
MTTF = 4957 years

The presentation of FIT rate for the individual product reliability is restricted by the actual burn-in sample size of the selected product (AON6450L). Failure Rate Determination is based on JEDEC Standard JESD 85. FIT means one failure per billion hours.

Failure Rate = $Chi^2 \times 10^9$ **/ [**2 (N) (H) (Af)**] =** 1.83×10^9 **/ [**2x (2x77x1000) x258**] =** 23
MTTF = 10^9 / FIT = 4.34×10^7hrs = 4957 years

Chi² = Chi Squared Distribution, determined by the number of failures and confidence interval
N = Total Number of units from HTRB and HTGB tests
H = Duration of HTRB/HTGB testing
Af = Acceleration Factor from Test to Use Conditions (Ea = 0.7eV and Tuse = 55℃)
Acceleration Factor [Af**]** = **Exp** [Ea / **k** (1/Tj u – 1/Tj s)]
Acceleration Factor ratio list:

	55 deg C	70 deg C	85 deg C	100 deg C	115 deg C	130 deg C	150 deg C
Af	258	87	32	13	5.64	2.59	1

Tj s = Stressed junction temperature in degree (Kelvin), K = C+273.16
Tj u = The use junction temperature in degree (Kelvin), K = C+273.16
K = Boltzmann's constant, 8.617164 X 10-5eV / K