

NTF3055L175

Power MOSFET 2.0 A, 60 V, Logic Level

N-Channel SOT-223

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- This is a Pb-Free Device

Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	60	Vdc
Drain-to-Gate Voltage ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	60	Vdc
Gate-to-Source Voltage Continuous Non-repetitive ($t_p \leq 10 \text{ ms}$)	V_{GS}	± 15 ± 20	Vdc Vpk
Drain Current Continuous @ $T_A = 25^\circ\text{C}$ Continuous @ $T_A = 100^\circ\text{C}$ Single Pulse ($t_p \leq 10 \mu\text{s}$)	I_D I_D I_{DM}	2.0 1.2 6.0	Adc Adc Apk
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 2) Derate above 25°C	P_D	2.1 1.3 0.014	W W W/ $^\circ\text{C}$
Operating and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ($V_{DD} = 25 \text{ Vdc}, V_{GS} = 5.0 \text{ Vdc},$ $I_{L(pk)} = 3.6 \text{ A}, L = 10 \text{ mH}, V_{DS} = 60 \text{ Vdc}$)	E_{AS}	65	mJ
Thermal Resistance Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$R_{\theta JA}$ $R_{\theta JA}$	72.3 114	$^\circ\text{C/W}$
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

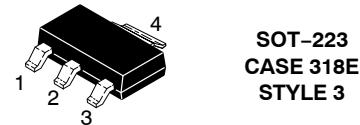
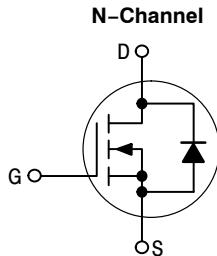
1. When surface mounted to an FR4 board using 1" pad size, 1 oz. (Cu. Area 0.995 in²).
2. When surface mounted to an FR4 board using minimum recommended pad size, 2-2.4 oz. (Cu. Area 0.272 in²).



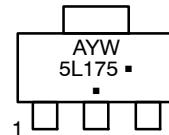
ON Semiconductor®

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2.0 AMPERES, 60 VOLTS
 $R_{DS(on)} = 175 \text{ m}\Omega$



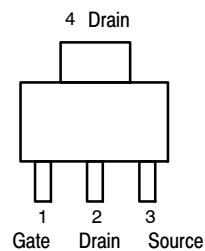
MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
5L175 = Device Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTF3055L175

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 3) (V _{GS} = 0 Vdc, I _D = 250 μ Adc) Temperature Coefficient (Positive)	V _{(BR)DSS}	60 –	72.8 74.4	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc) (V _{DS} = 60 Vdc, V _{GS} = 0 Vdc, T _J = 150°C)	I _{DSS}	– –	– –	1.0 10	μ Adc
Gate-Body Leakage Current (V _{GS} = \pm 15 Vdc, V _{DS} = 0 Vdc)	I _{GS}	–	–	\pm 100	nAdc

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage (Note 3) (V _{DS} = V _{GS} , I _D = 250 μ Adc) Threshold Temperature Coefficient (Negative)	V _{GS(th)}	1.0 –	1.7 4.2	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 5.0 Vdc, I _D = 1.0 Adc)	R _{DS(on)}	–	155	175	m Ω
Static Drain-to-Source On-Resistance (Note 3) (V _{GS} = 5.0 Vdc, I _D = 2.0 Adc) (V _{GS} = 5.0 Vdc, I _D = 1.0 Adc, T _J = 150°C)	V _{DS(on)}	–	0.32 0.57	0.42 –	Vdc
Forward Transconductance (Note 3) (V _{DS} = 8.0 Vdc, I _D = 1.5 Adc)	g _f	–	3.2	–	Mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	(V _{DS} = 25 Vdc, V _{GS} = 0 V, f = 1.0 MHz)	C _{iss}	–	194	270	pF
Output Capacitance		C _{oss}	–	70	100	
Transfer Capacitance		C _{rss}	–	29	40	

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	(V _{DD} = 30 Vdc, I _D = 2.0 Adc, V _{GS} = 5.0 Vdc, R _G = 9.1 Ω) (Note 3)	t _{d(on)}	–	10.2	20	ns
Rise Time		t _r	–	21	40	
Turn-Off Delay Time		t _{d(off)}	–	14.3	30	
Fall Time		t _f	–	15.3	30	
Gate Charge	(V _{DS} = 48 Vdc, I _D = 2.0 Adc, V _{GS} = 5.0 Vdc) (Note 3)	Q _T	–	5.1	10	nC
		Q ₁	–	1.4	–	
		Q ₂	–	2.5	–	

SOURCE-DRAIN DIODE CHARACTERISTICS

Forward On-Voltage	(I _S = 2.0 Adc, V _{GS} = 0 Vdc) (I _S = 2.0 Adc, V _{GS} = 0 Vdc, T _J = 150°C) (Note 3)	V _{SD}	– –	0.84 0.68	1.0 –	Vdc
Reverse Recovery Time	(I _S = 2.0 Adc, V _{GS} = 0 Vdc, dI _S /dt = 100 A/ μ s) (Note 3)	t _{rr}	–	28.3	–	ns
		t _a	–	15.6	–	
		t _b	–	12.7	–	
Reverse Recovery Stored Charge		Q _{RR}	–	0.027	–	μ C

3. Pulse Test: Pulse Width \leq 300 μ s, Duty Cycle \leq 2.0%.

4. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

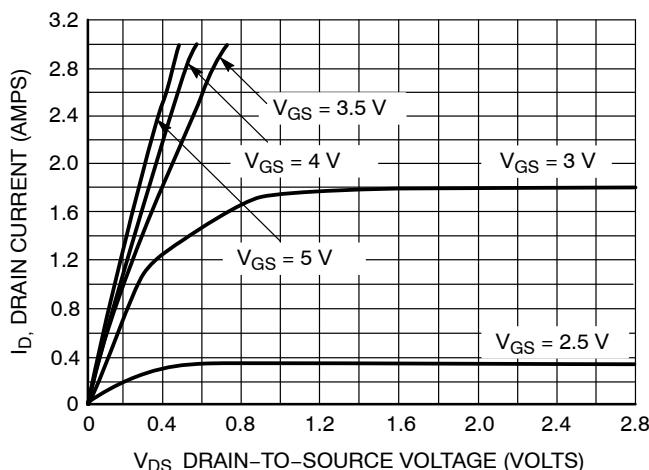


Figure 1. On-Region Characteristics

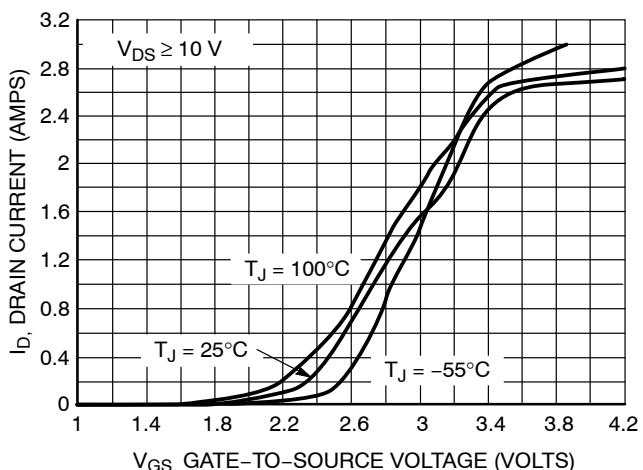


Figure 2. Transfer Characteristics

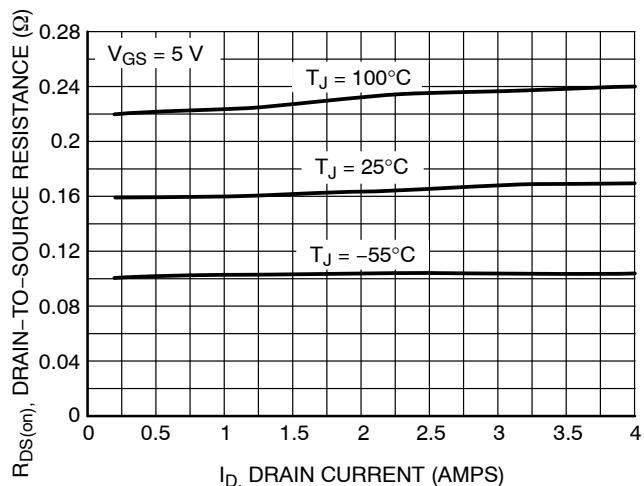


Figure 3. On-Resistance versus Gate-to-Source Voltage

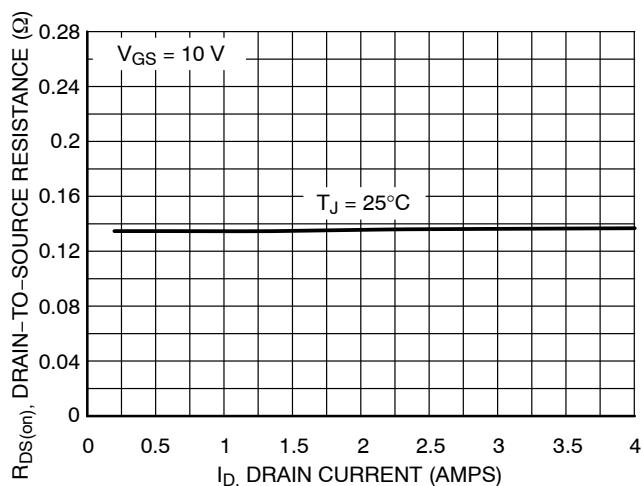


Figure 4. On-Resistance versus Drain Current and Gate Voltage

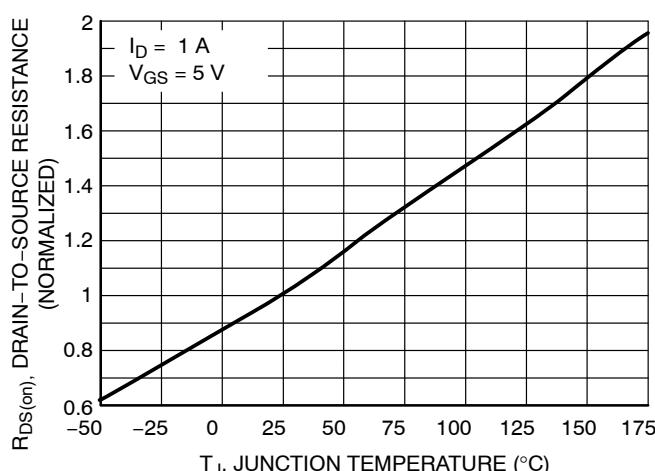


Figure 5. On-Resistance Variation with Temperature

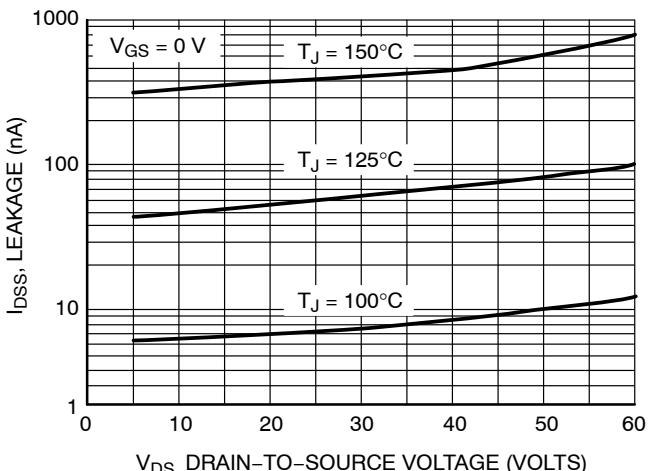


Figure 6. Drain-to-Source Leakage Current versus Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

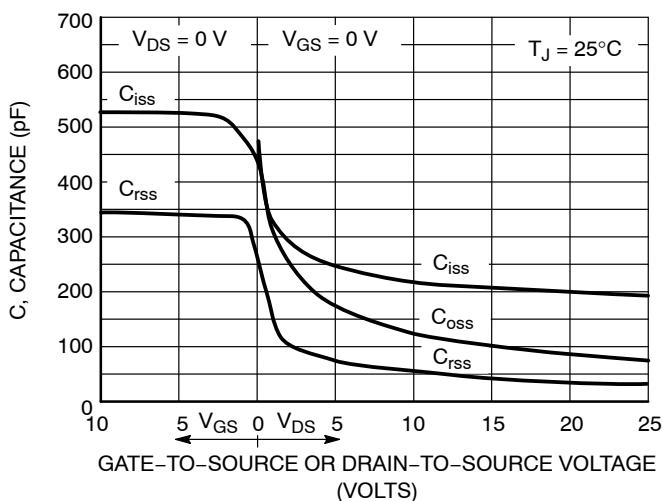


Figure 7. Capacitance Variation

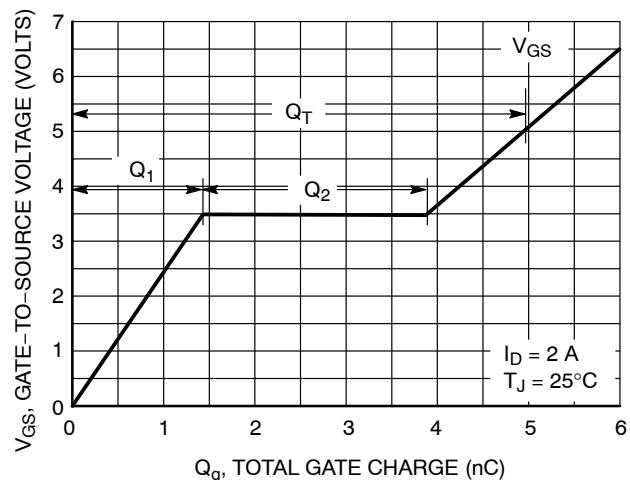


Figure 8. Gate-to-Source and Drain-to-Source Voltage versus Total Charge

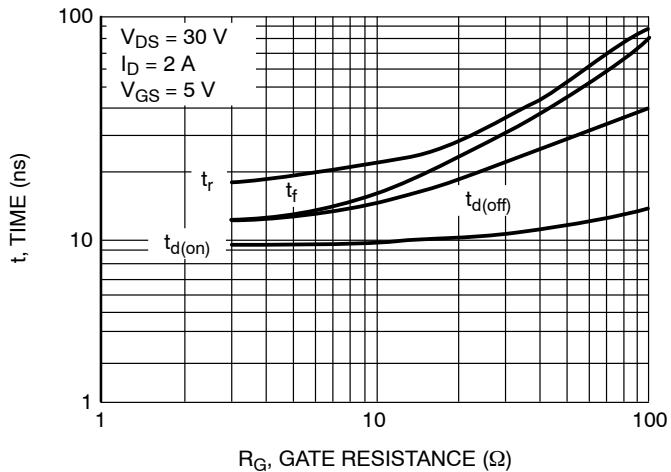


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

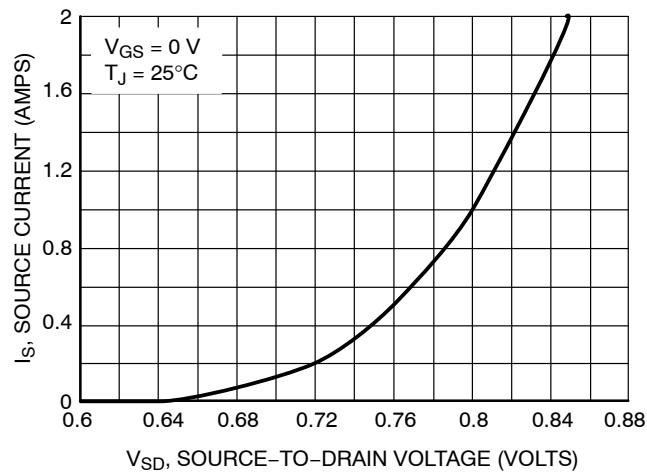


Figure 10. Diode Forward Voltage versus Current

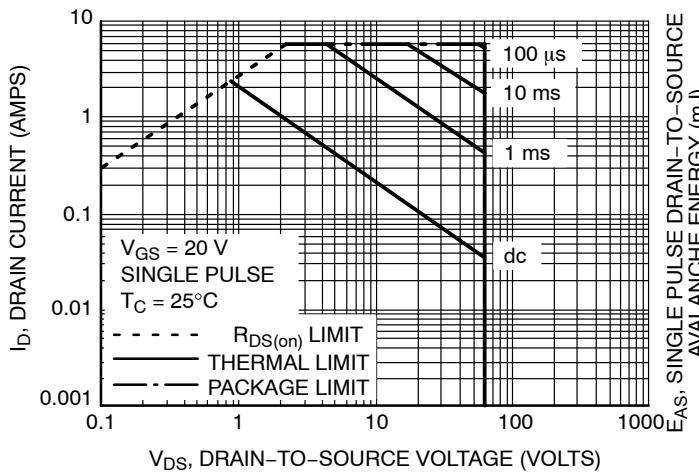


Figure 11. Maximum Rated Forward Biased Safe Operating Area

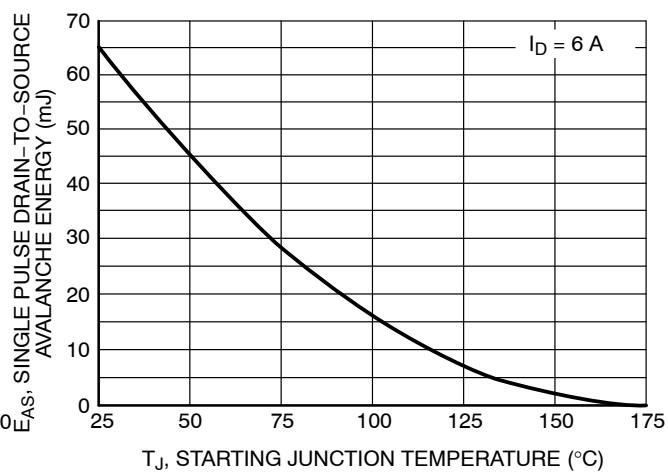


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

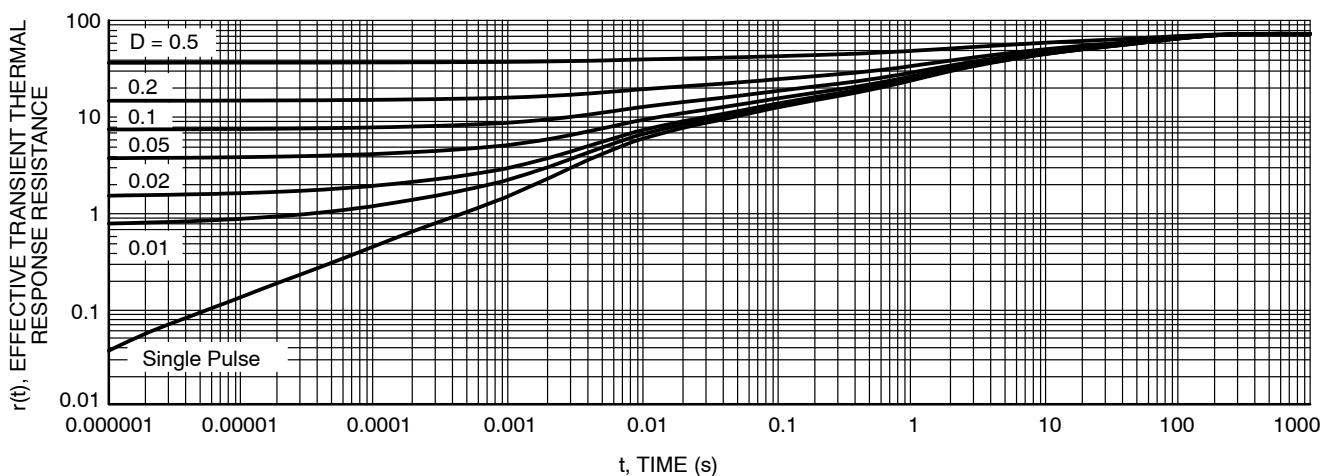


Figure 13. Thermal Response

ORDERING INFORMATION

Device	Package	Shipping [†]
NTF3055L175T1G	SOT-223 (TO-261) (Pb-Free)	1000 / Tape & Reel

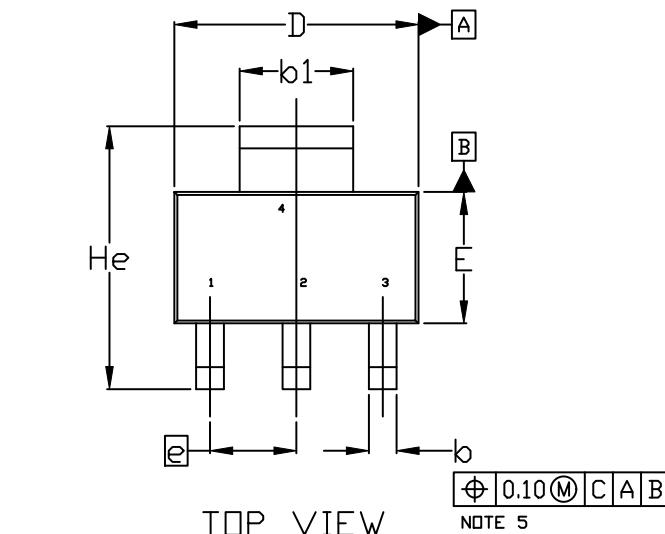
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



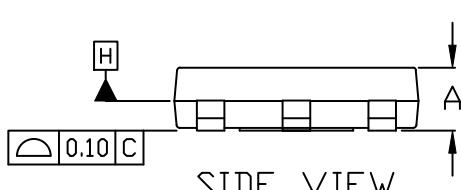
SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

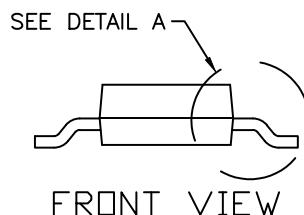
DATE 02 OCT 2018



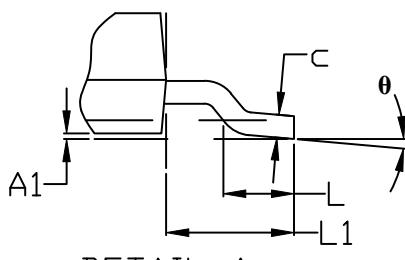
TOP VIEW



SIDE VIEW



FRONT VIEW

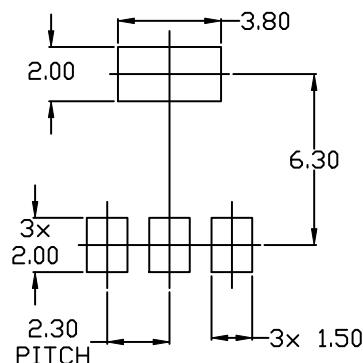


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



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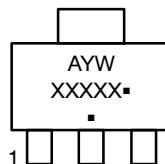
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SOT-223 (TO-261)
CASE 318E-04
ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. Emitter 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. Emitter 4. COLLECTOR		

**GENERIC
MARKING DIAGRAM***



A = Assembly Location

Y = Year

W = Work Week

XXXXX = Specific Device Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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