

# NTB5411N, NTP5411N

## Power MOSFET 80 Amps, 60 Volts N-Channel D<sup>2</sup>PAK, TO-220

### Features

- Low  $R_{DS(on)}$
- High Current Capability
- Avalanche Energy Specified
- These are Pb-Free Devices

### Applications

- LED Lighting and LED Backlight Drivers
- DC-DC Converters
- DC Motor Drivers
- Power Supplies Secondary Side Synchronous Rectification

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  Unless otherwise specified)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		$V_{DSS}$	60	V
Gate-to-Source Voltage – Continuous		$V_{GS}$	$\pm 20$	V
Gate-to-Source Voltage – Nonrepetitive ( $T_P < 10 \mu\text{s}$ )		$V_{GS}$	$\pm 30$	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$I_D$	80
				61
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	$P_D$	166
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	$I_{DM}$	185	A
Operating and Storage Temperature Range		$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$
Source Current (Body Diode)		$I_S$	75	A
Single Pulse Drain-to-Source Avalanche Energy – Starting $T_J = 25^\circ\text{C}$ ( $V_{DD} = 50 \text{ V}_{\text{dc}}, V_{GS} = 10 \text{ V}_{\text{dc}}, I_{L(pk)} = 75 \text{ A}, L = 0.1 \text{ mH}, R_G = 25 \Omega$ )		$E_{AS}$	280	mJ
Lead Temperature for Soldering Purposes, 1/8" from Case for 10 Seconds		$T_L$	260	$^\circ\text{C}$

### THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Case (Drain) Steady State (Note 1)	$R_{\theta JC}$	0.9	$^\circ\text{C/W}$
	$R_{\theta JA}$	43	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface mounted on FR4 board using 1 sq in pad size, (Cu Area 1.127 sq in [1 oz] including traces).

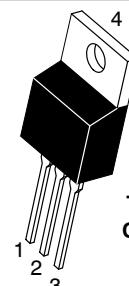
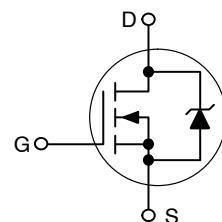


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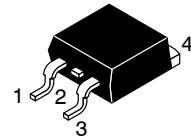
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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$ (Note 1)
60 V	10 m $\Omega$ @ 10 V	80 A

N-Channel

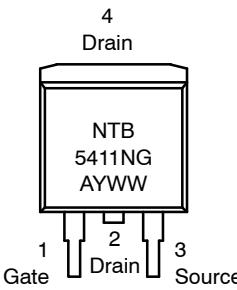
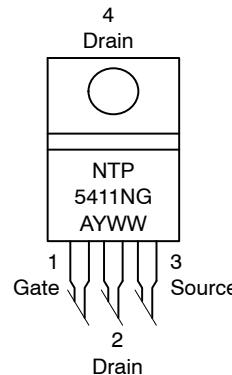


TO-220AB  
CASE 221A  
STYLE 5



D<sup>2</sup>PAK  
CASE 418B  
STYLE 2

### MARKING DIAGRAM & PIN ASSIGNMENT



G = Pb-Free Device  
 A = Assembly Location  
 Y = Year  
 WW = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTB5411N, NTP5411N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ Unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{DS}} = 0 \text{ V}, I_{\text{D}} = 250 \mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(\text{BR})\text{DSS}/T_J}$			54.2		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	$I_{\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}$ $V_{\text{DS}} = 60 \text{ V}$	$T_J = 25^\circ\text{C}$		10	$\mu\text{A}$
			$T_J = 150^\circ\text{C}$		100	
Gate-Body Leakage Current	$I_{\text{GSS}}$	$V_{\text{DS}} = 0 \text{ V}, V_{\text{GS}} = \pm 20 \text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{\text{GS}(\text{th})}$	$V_{\text{GS}} = V_{\text{DS}}, I_{\text{D}} = 250 \mu\text{A}$	2.0	3.2	4.0	V
Negative Threshold Temperature Coefficient	$V_{\text{GS}(\text{th})/T_J}$			6.6		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Voltage	$V_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}, I_{\text{D}} = 80 \text{ A}$		0.71	0.92	V
		$V_{\text{GS}} = 10 \text{ V}, I_{\text{D}} = 40 \text{ A}, 150^\circ\text{C}$		0.65		
Static Drain-to-Source On-Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}, I_{\text{D}} = 40 \text{ A}$		8.4	10	$\text{m}\Omega$
Forward Transconductance	$g_{\text{FS}}$	$V_{\text{GS}} = 15 \text{ V}, I_{\text{D}} = 40 \text{ A}$		70		S

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{\text{iss}}$	$V_{\text{DS}} = 25 \text{ V}, V_{\text{GS}} = 0 \text{ V}, f = 1 \text{ MHz}$		3365	4500	pF
Output Capacitance	$C_{\text{oss}}$			615		
Transfer Capacitance	$C_{\text{rss}}$			230		
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$	$V_{\text{GS}} = 10 \text{ V}, V_{\text{DS}} = 48 \text{ V}, I_{\text{D}} = 80 \text{ A}$		92	130	nC
Threshold Gate Charge	$Q_{\text{G}(\text{TH})}$			4.1		
Gate-to-Source Charge	$Q_{\text{GS}}$			19		
Gate-to-Drain Charge	$Q_{\text{GD}}$			43		

### SWITCHING CHARACTERISTICS, $V_{\text{GS}} = 10 \text{ V}$ (Note 3)

Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}, V_{\text{DD}} = 48 \text{ V}, I_{\text{D}} = 80 \text{ A}, R_{\text{G}} = 9.1 \Omega$		22		ns
Rise Time	$t_{\text{r}}$			122		
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			116		
Fall Time	$t_{\text{f}}$			113		

### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{\text{SD}}$	$V_{\text{GS}} = 0 \text{ V}$ $I_{\text{S}} = 37.5 \text{ A}$	$T_J = 25^\circ\text{C}$		0.91	1.1	$V_{\text{dc}}$
			$T_J = 150^\circ\text{C}$		0.8		
Reverse Recovery Time	$t_{\text{rr}}$	$I_{\text{S}} = 37.5 \text{ A}_{\text{dc}}, V_{\text{GS}} = 0 \text{ V}_{\text{dc}}, \frac{dI_{\text{S}}}{dt} = 100 \text{ A}/\mu\text{s}$			62		ns
Charge Time	$t_{\text{a}}$				43		
Discharge Time	$t_{\text{b}}$				19		
Reverse Recovery Stored Charge	$Q_{\text{RR}}$				0.15		

2. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle = 2%.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

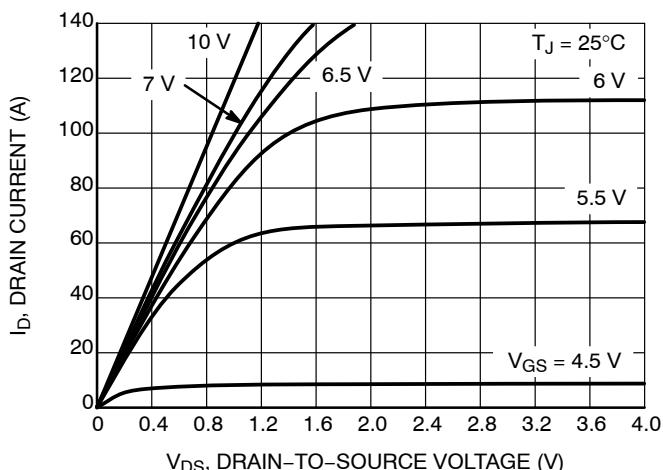


Figure 1. On-Region Characteristics

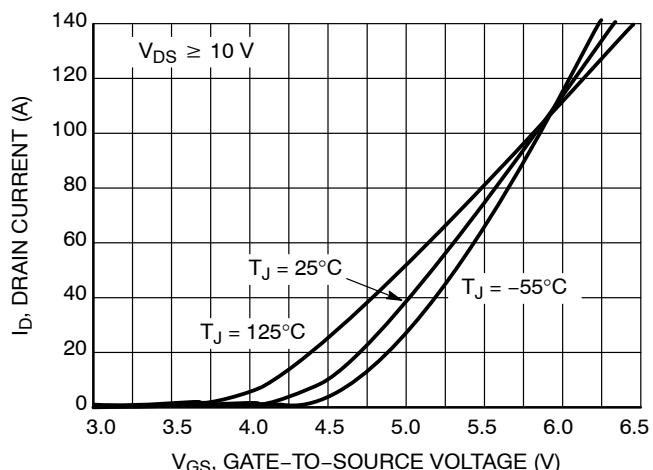


Figure 2. Transfer Characteristics

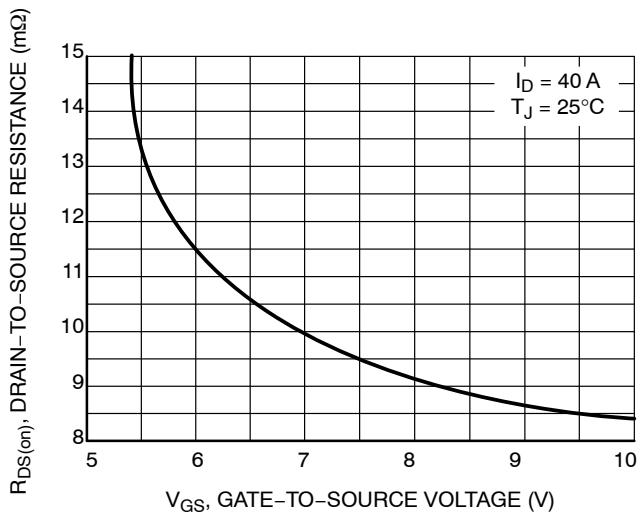


Figure 3. On-Resistance vs. Gate-to-Source Voltage

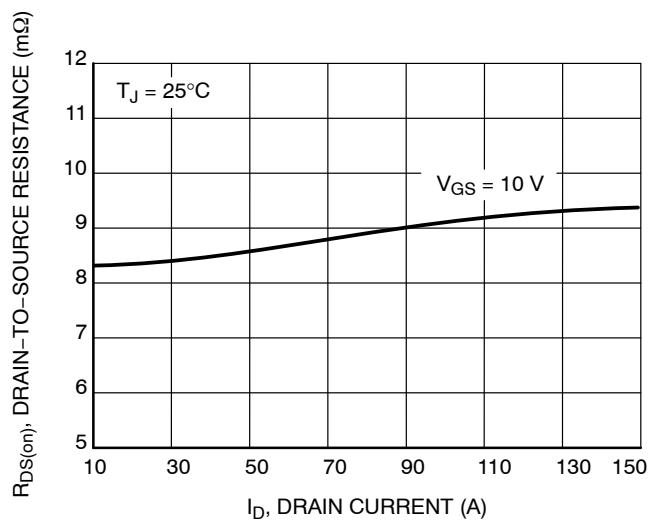


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

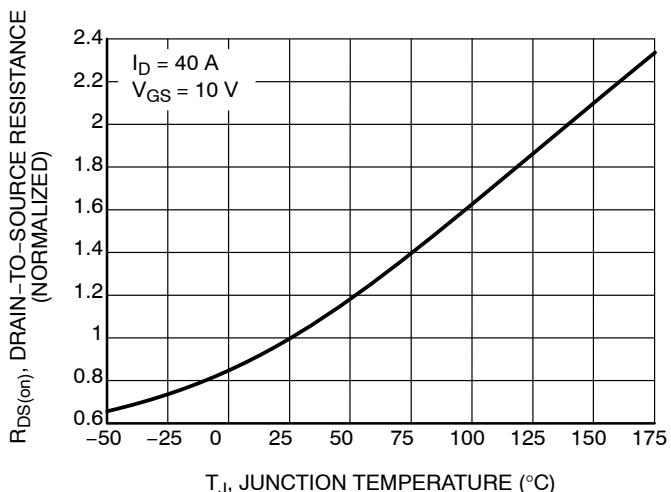


Figure 5. On-Resistance Variation with Temperature

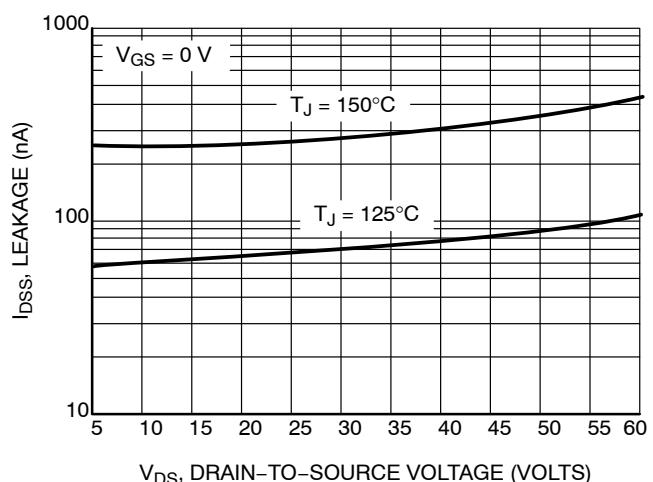
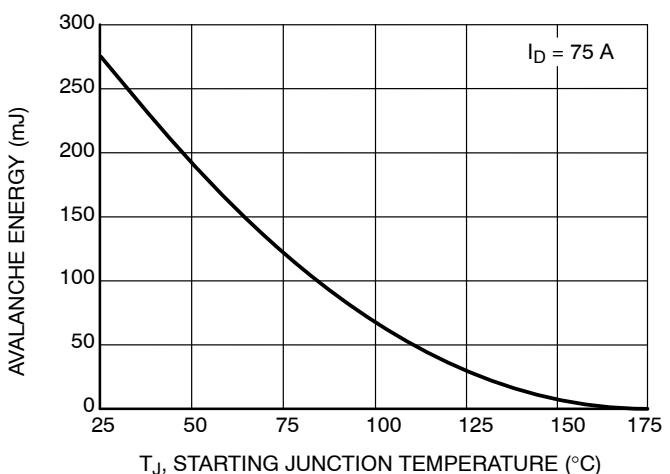
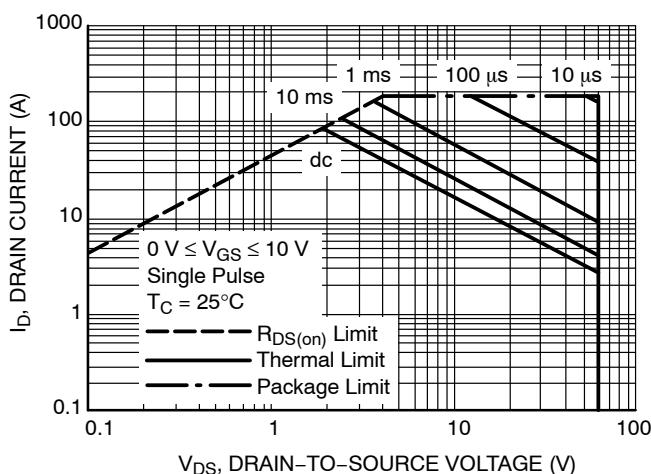
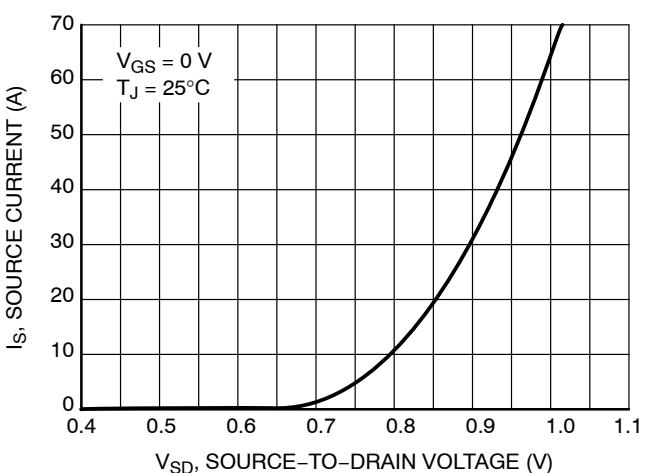
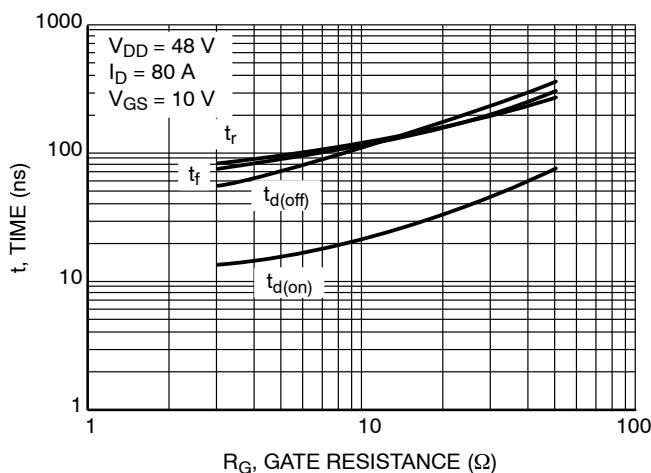
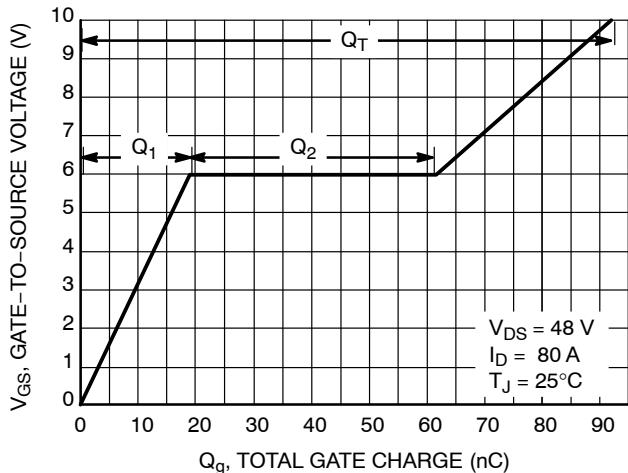
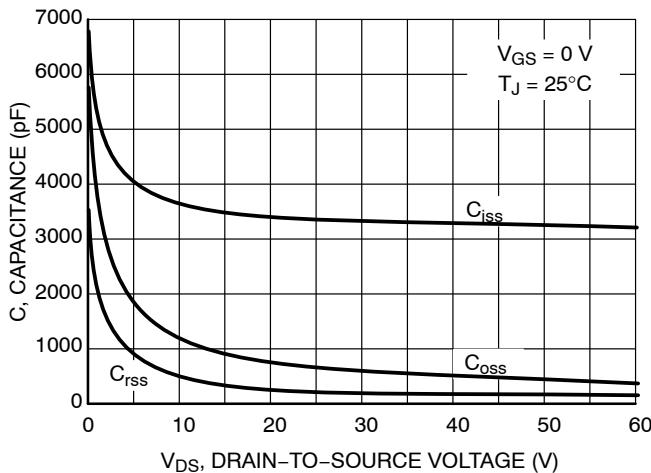


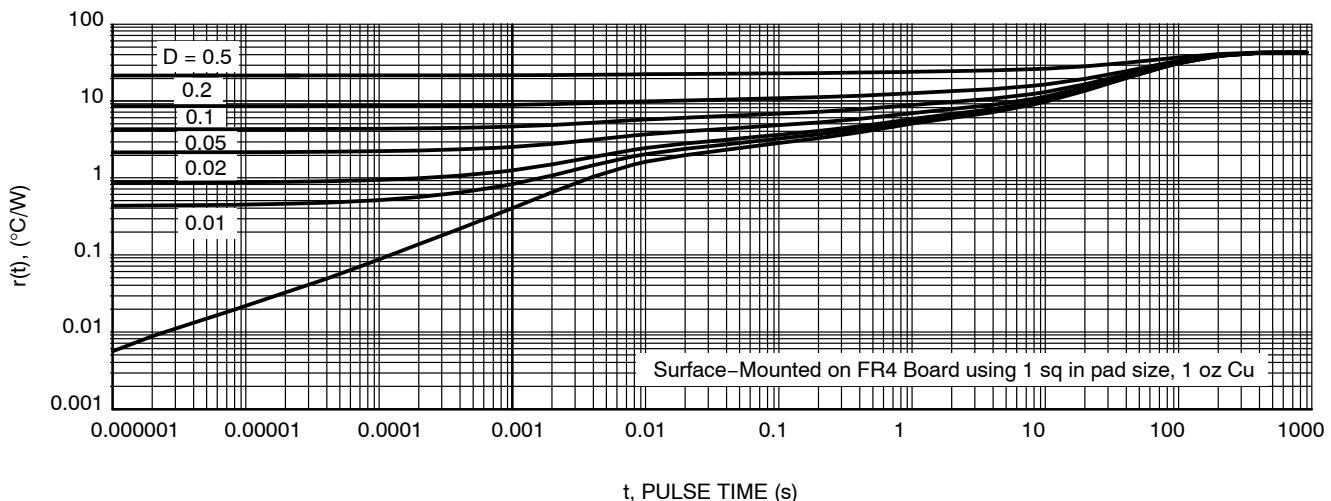
Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES



# NTB5411N, NTP5411N

## TYPICAL PERFORMANCE CURVES



**Figure 13. Thermal Response**

### ORDERING INFORMATION

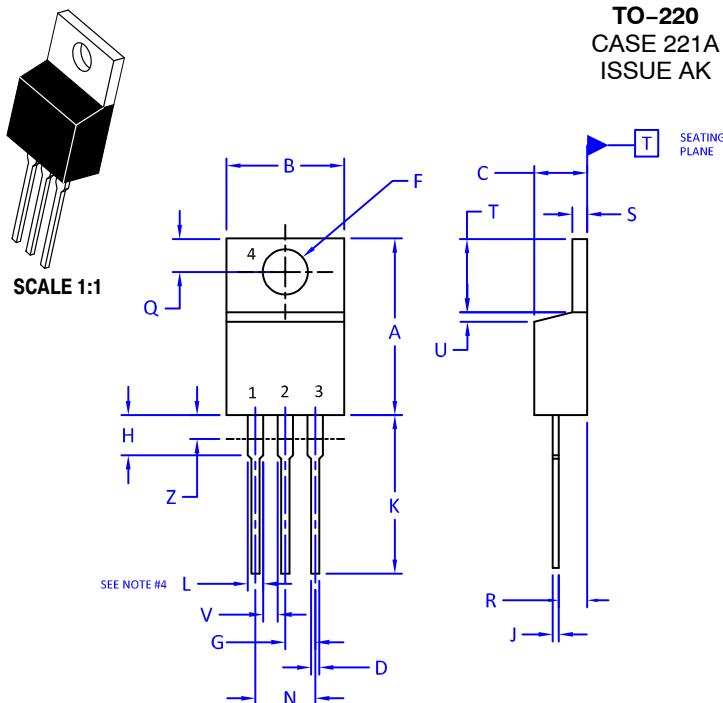
Device	Package	Shipping <sup>†</sup>
NTP5411NG	TO-220AB (Pb-Free)	50 Units / Rail
NTB5411NT4G	D <sup>2</sup> PAK (Pb-Free)	800 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

onsemi™



DATE 13 JAN 2022

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. Emitter  
4. COLLECTOR

STYLE 5:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

STYLE 9:  
PIN 1. GATE  
2. COLLECTOR  
3. Emitter  
4. COLLECTOR

STYLE 2:  
PIN 1. BASE  
2. Emitter  
3. COLLECTOR  
4. Emitter

STYLE 6:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE

STYLE 10:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN  
4. SOURCE

STYLE 3:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE

STYLE 7:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. ANODE

STYLE 11:  
PIN 1. DRAIN  
2. SOURCE  
3. GATE  
4. SOURCE

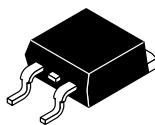
STYLE 4:  
PIN 1. MAIN TERMINAL 1  
2. MAIN TERMINAL 2  
3. GATE  
4. MAIN TERMINAL 2

STYLE 8:  
PIN 1. CATHODE  
2. ANODE  
3. EXTERNAL TRIP/DELAY  
4. ANODE

STYLE 12:  
PIN 1. MAIN TERMINAL 1  
2. MAIN TERMINAL 2  
3. GATE  
4. NOT CONNECTED

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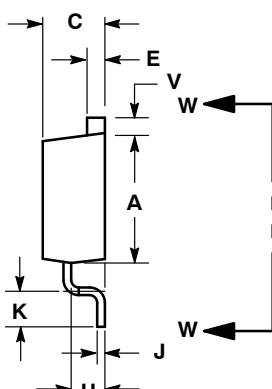
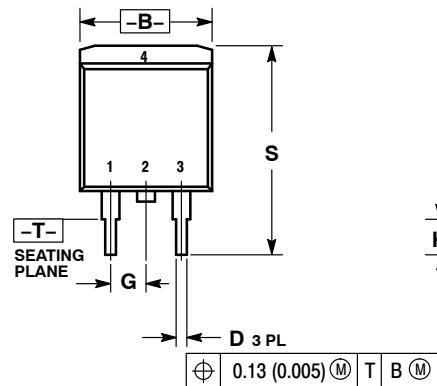
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**D<sup>2</sup>PAK 3**  
CASE 418B-04  
ISSUE L

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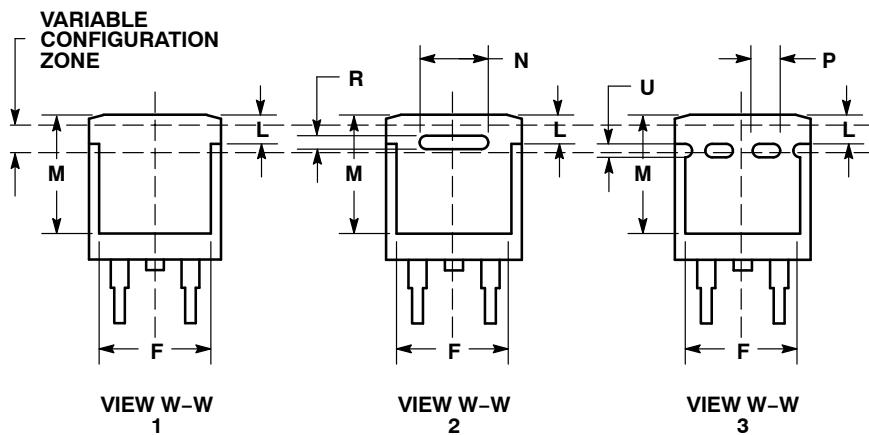
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NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. Emitter  
4. COLLECTOR

STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE

STYLE 4:  
PIN 1. GATE  
2. COLLECTOR  
3. Emitter  
4. COLLECTOR

STYLE 5:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. ANODE

STYLE 6:  
PIN 1. NO CONNECT  
2. CATHODE  
3. ANODE  
4. CATHODE

**MARKING INFORMATION AND FOOTPRINT ON PAGE 2**

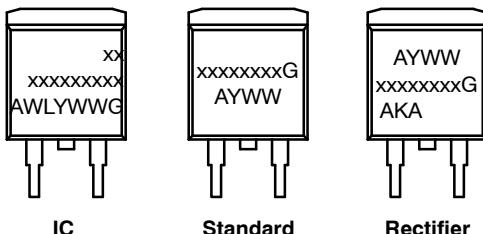
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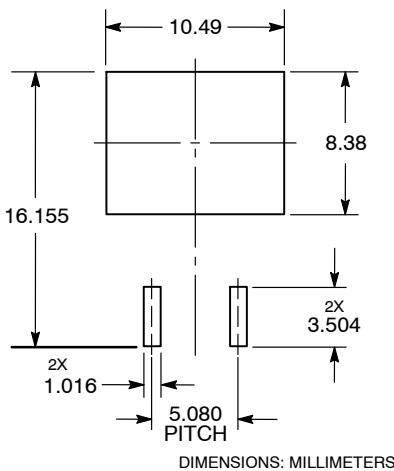
## GENERIC MARKING DIAGRAM\*



xx	= Specific Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb-Free Package
AKA	= Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

## SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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