DUAL N-CHANNEL ENHANCEMENT MODE FIELD EFFECT TRANSISTOR

Features

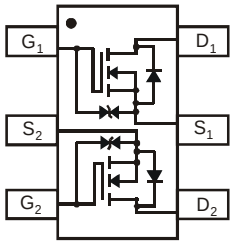
- Dual N-Channel MOSFET
- Low On-Resistance
  - 100mΩ @V_{GS} = 4.5V, I_D = 2.5A
  - 140mΩ @V_{GS} = 2.5V, I_D = 1.5A
  - 215mΩ @V_{GS} = 1.8V, I_D = 0.1A
- Very Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate to 2kV HBM
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

Mechanical Data

- Case: SOT26
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections: See Diagram
- Terminals: Finish — Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.015 grams (Approximate)

SOT26

Top View



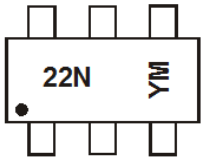
Top View
Schematic and Pin Configuration

Ordering Information (Note 4)

Part Number	Case	Packaging
DMN2215UDM-7	SOT26	3000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



22N = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: G = 2019)
M = Month (ex: 9 = September)

Date Code Key

Year	2007	~	2019	2020	2021	2022	2023	2024	2025
Code	U	~	G	H	I	J	K	L	M

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	20	V
Gate-Source Voltage		V_{GSS}	±12	V
Drain Current (Note 5)	T_A = +25°C T_A = +85°C	I_D	2.0 1.4	A
Pulsed Drain Current (Note 6)		I_{DM}	7.0	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	650	mW
Thermal Resistance, Junction to Ambient	$R_{\theta JA}$	192	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	20	—	—	V	V_{GS} = 0V, I_D = 10μA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	V_{DS} = 20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±10	μA	V_{GS} = ±12V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	0.6	—	1.0	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	80 105 165	100 140 215	mΩ	V_{GS} = 4.5V, I_D = 2.5A V_{GS} = 2.5V, I_D = 1.5A V_{GS} = 1.8V, I_D = 0.1A
Forward Transfer Admittance	$\|Y_{fs}\|$	—	5	—	S	V_{DS} =5V, I_D = 2.4A
Diode Forward Voltage (Note 7)	V_{SD}	—	0.73	1.1	V	V_{GS} = 0V, I_S = 1.05A
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	—	188	—	pF	V_{DS} = 10V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	44	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	30	—	pF	
Turn-On Delay Time	$t_{D(ON)}$	—	8	—	ns	V_{DD} = 10V, R_L = 10Ω I_D = 1A, V_{GEN} = 4.5V, R_G = 6Ω
Rise Time	t_R	—	3.8	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	19.6	—		
Fall Time	t_F	—	8.3	—		

Notes: 5. Device mounted on FR-4 PCB, or minimum recommended pad layout.
6. Pulse width ≤ 10μs, duty cycle ≤ 1%.
7. Short duration pulse test used to minimize self-heating effect.

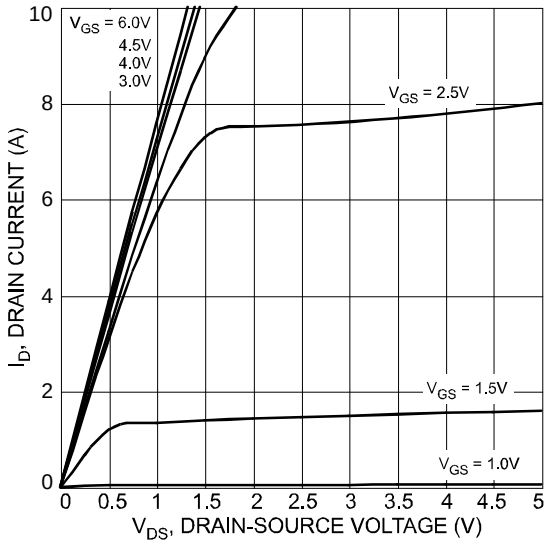


Fig. 1 Typical Output Characteristic

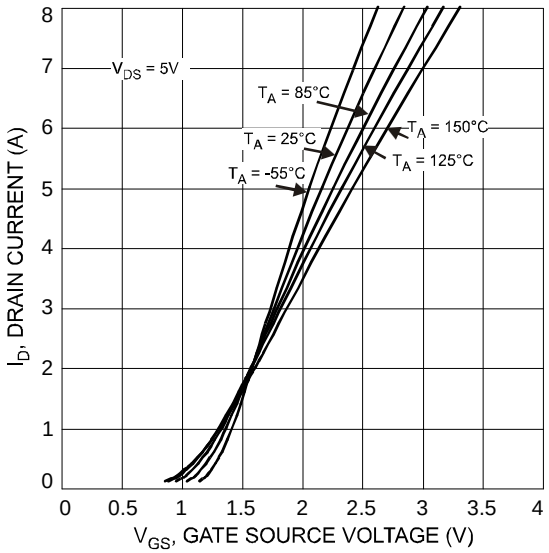


Fig. 2 Typical Transfer Characteristics

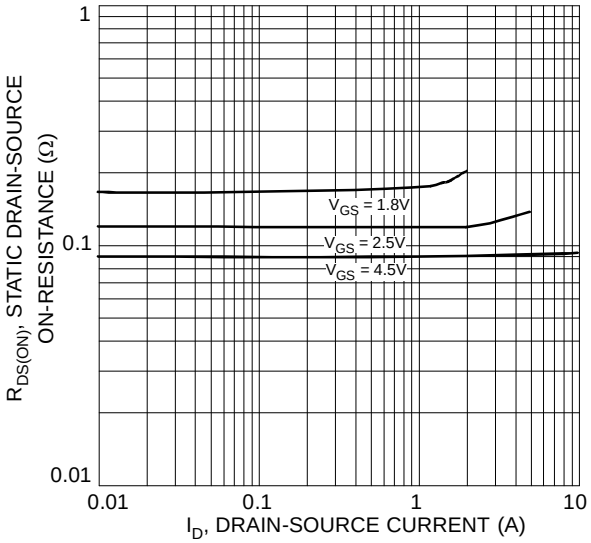


Fig. 3 On-Resistance vs. Drain-Source Current & Gate Voltage

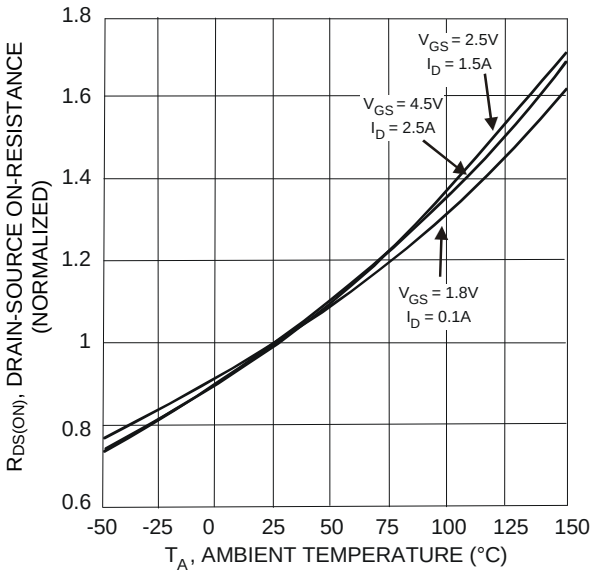


Fig. 4 Normalized Static Drain-Source On-Resistance vs. Ambient Temperature

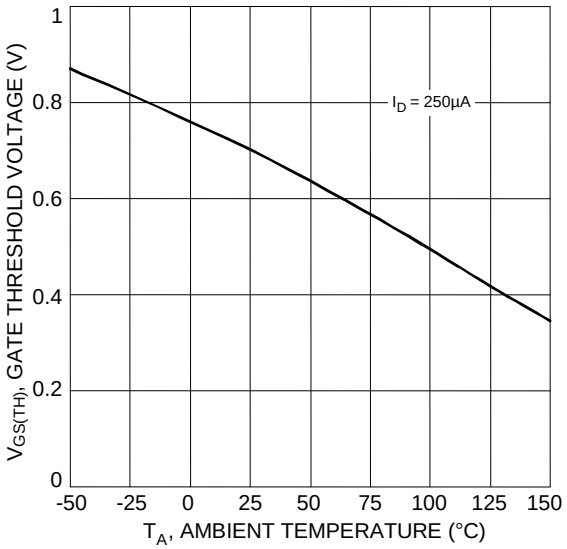


Fig. 5 Gate Threshold Variation with Temperature

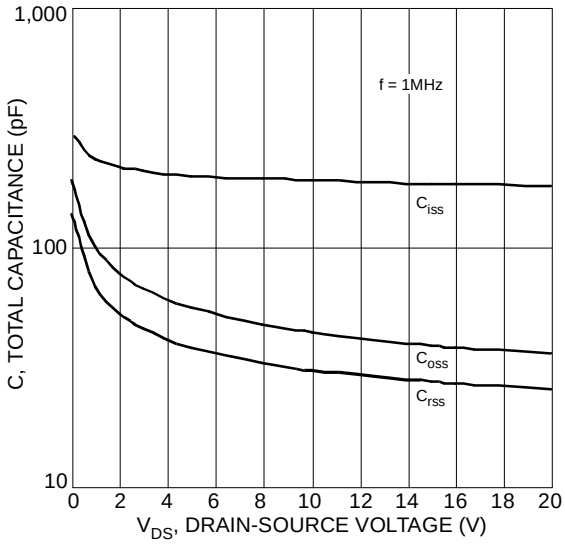


Fig. 6 Typical Total Capacitance

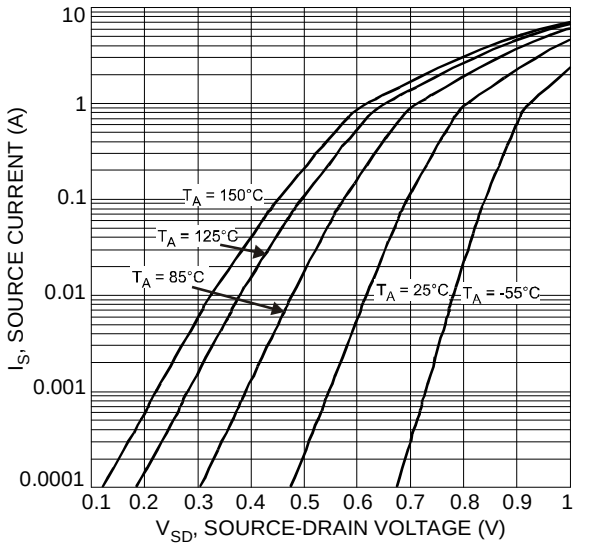
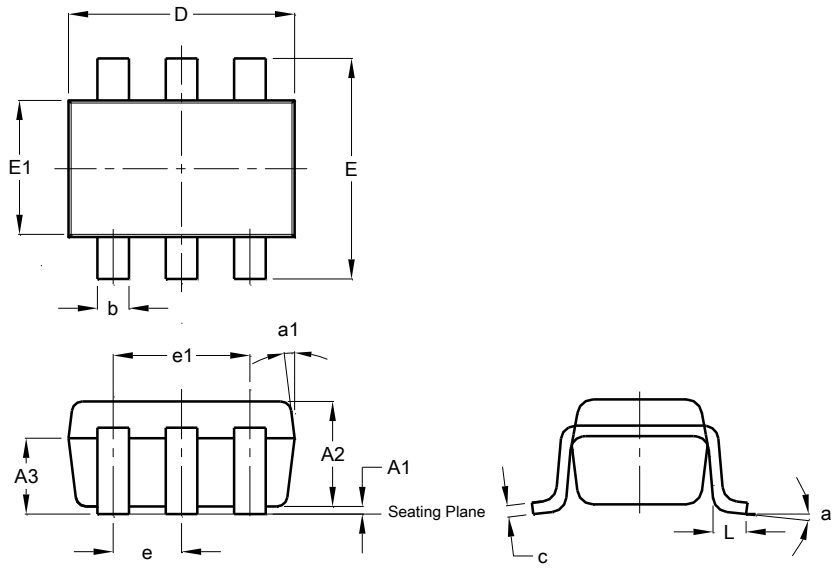


Fig. 7 Reverse Drain Current vs. Source-Drain Voltage

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26

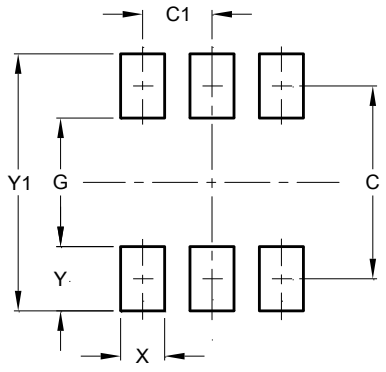


SOT26			
Dim	**Min**	**Max**	**Typ**
A1	0.013	0.10	0.05
A2	1.00	1.30	1.10
A3	0.70	0.80	0.75
b	0.35	0.50	0.38
c	0.10	0.20	0.15
D	2.90	3.10	3.00
e	-	-	0.95
e1	-	-	1.90
E	2.70	3.00	2.80
E1	1.50	1.70	1.60
L	0.35	0.55	0.40
a	-	-	8°
a1	-	-	7°
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT26



Dimensions	Value (in mm)
C	2.40
C1	0.95
G	1.60
X	0.55
Y	0.80
Y1	3.20

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