

NVDD5894NL

Power MOSFET

40 V, 10 mΩ, 64 A, Dual N-Channel
DPAK-5L

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- High Current Capability
- Avalanche Energy Specified
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	40	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	<small>Steady State</small>	$T_C = 25^\circ\text{C}$	I_D	64
		$T_C = 100^\circ\text{C}$		45
	<small>Steady State</small>	$T_C = 25^\circ\text{C}$	P_D	75
		$T_C = 100^\circ\text{C}$		38
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	<small>Steady State</small>	$T_A = 25^\circ\text{C}$	I_D	14
		$T_A = 100^\circ\text{C}$		10
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	<small>Steady State</small>	$T_A = 25^\circ\text{C}$	P_D	3.8
		$T_A = 100^\circ\text{C}$		1.9
Pulsed Drain Current	$T_A = 25^\circ\text{C}$, $t_p = 10\ \mu\text{s}$	I_{DM}	324	A
Operating Junction and Storage Temperature		T_J , T_{stg}	-55 to +175	°C
Source Current (Body Diode)		I_S	75	A
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}$, $I_{L(pk)} = 25\text{ A}$, $L = 0.3\text{ mH}$)		E_{AS}	94	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Drain)	$R_{\theta JC}$	2.0	°C/W
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	40	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

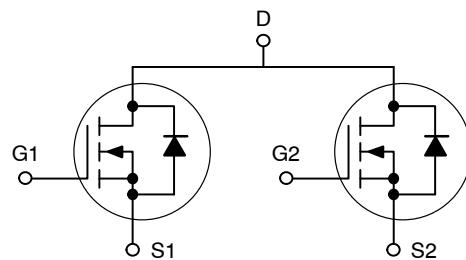


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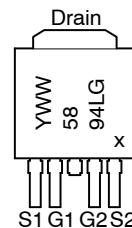
$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
40 V	10 mΩ @ 10 V	64 A
	14.5 mΩ @ 4.5 V	

Dual N-Channel



**DPAK 5-LEAD
CASE 175AA**

MARKING DIAGRAM & PIN ASSIGNMENT



Y = Year
WW = Work Week
5894L = Specific Device Code
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping [†]
NVDD5894NLT4G	DPAK-5 (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NVDD5894NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{\text{GS}} = 0 \text{ V}$, $I_D = 250 \mu\text{A}$	40			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{\text{GS}} = 0 \text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
		$V_{\text{DS}} = 40 \text{ V}$	$T_J = 125^\circ\text{C}$		100	
Gate-to-Source Leakage Current	I_{GSS}	$V_{\text{DS}} = 0 \text{ V}$, $V_{\text{GS}} = \pm 20 \text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{\text{GS}(\text{TH})}$	$V_{\text{GS}} = V_{\text{DS}}$, $I_D = 250 \mu\text{A}$	1.5		2.5	V
Drain-to-Source On Resistance	$R_{\text{DS}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}$, $I_D = 50 \text{ A}$		8.3	10	$\text{m}\Omega$
		$V_{\text{GS}} = 4.5 \text{ V}$, $I_D = 20 \text{ A}$		11.2	14.5	
Forward Transconductance	g_{FS}	$V_{\text{DS}} = 15 \text{ V}$, $I_D = 10 \text{ A}$		8.8		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{iss}	$V_{\text{GS}} = 0 \text{ V}$, $f = 1 \text{ MHz}$ $V_{\text{DS}} = 25 \text{ V}$		2103		pF
Output Capacitance	C_{oss}			259		
Reverse Transfer Capacitance	C_{rss}			183		
Total Gate Charge	$Q_{\text{G}(\text{TOT})}$	$V_{\text{GS}} = 4.5 \text{ V}$, $V_{\text{DS}} = 32 \text{ V}$, $I_D = 20 \text{ A}$		21		nC
	$Q_{\text{G}(\text{TOT})}$	$V_{\text{GS}} = 10 \text{ V}$, $V_{\text{DS}} = 32 \text{ V}$, $I_D = 20 \text{ A}$		41		
Threshold Gate Charge	$Q_{\text{G}(\text{TH})}$	$V_{\text{GS}} = 10 \text{ V}$, $V_{\text{DS}} = 32 \text{ V}$, $I_D = 20 \text{ A}$		1.7		nC
Gate-to-Source Charge	Q_{GS}			6.9		
Gate-to-Drain Charge	Q_{GD}			11.3		
Plateau Voltage	V_{GP}			3.5		V

SWITCHING CHARACTERISTICS

Turn-On Delay Time	$t_{\text{d}(\text{on})}$	$V_{\text{GS}} = 10 \text{ V}$, $V_{\text{DS}} = 32 \text{ V}$ $I_D = 20 \text{ A}$, $R_G = 2.5 \Omega$		12.4		ns
Rise Time	t_r			30.2		
Turn-Off Delay Time	$t_{\text{d}(\text{off})}$			36		
Fall Time	t_f			54		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{\text{GS}} = 0 \text{ V}$ $I_S = 20 \text{ A}$	$T_J = 25^\circ\text{C}$		0.88	1.0	V
			$T_J = 125^\circ\text{C}$		0.76		
Reverse Recovery Time	t_{RR}	$V_{\text{GS}} = 0 \text{ V}$, $dI_S/dt = 100 \text{ A}/\mu\text{s}$ $I_S = 20 \text{ A}$			22.8		ns
Charge Time	t_a				11.2		
Discharge Time	t_b				11.6		
Reverse Recovery Charge	Q_{RR}				13.7		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

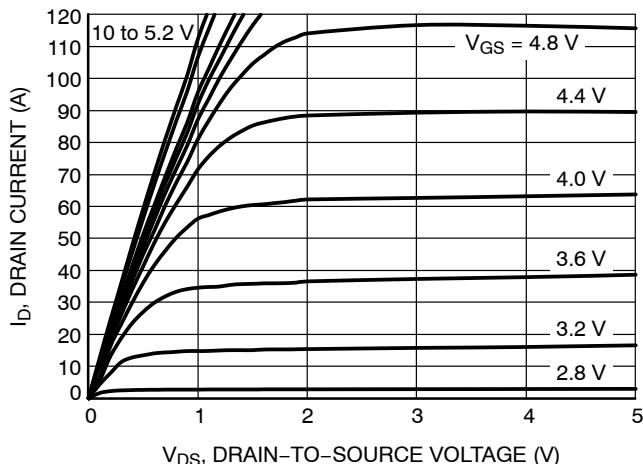


Figure 1. On-Region Characteristics

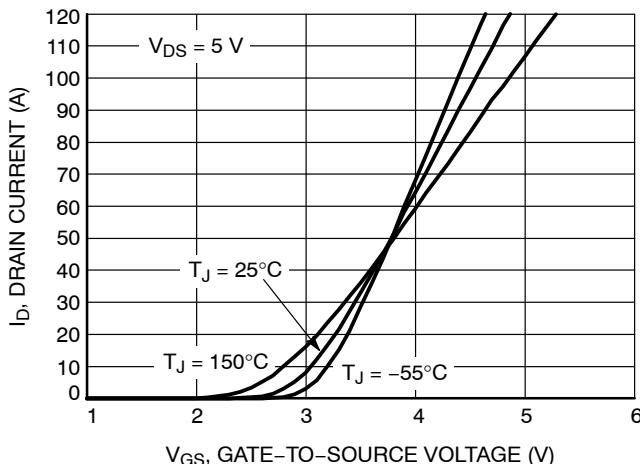


Figure 2. Transfer Characteristics

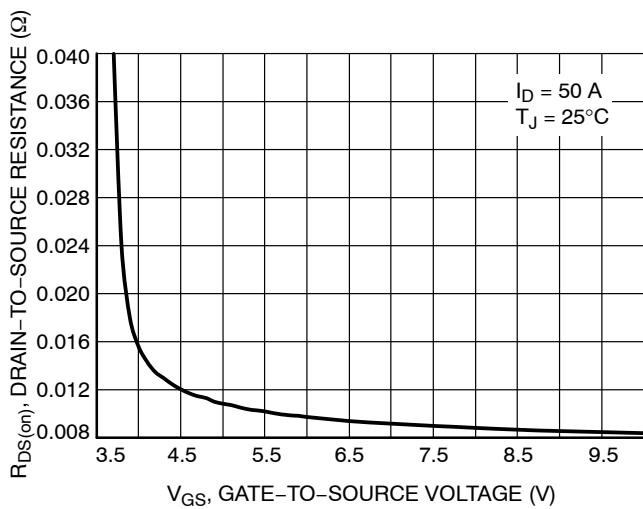


Figure 3. On-Resistance vs. Gate-to-Source Voltage

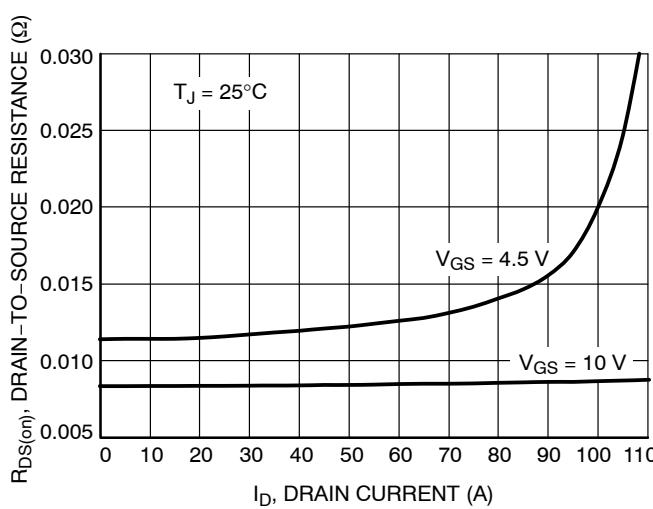


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

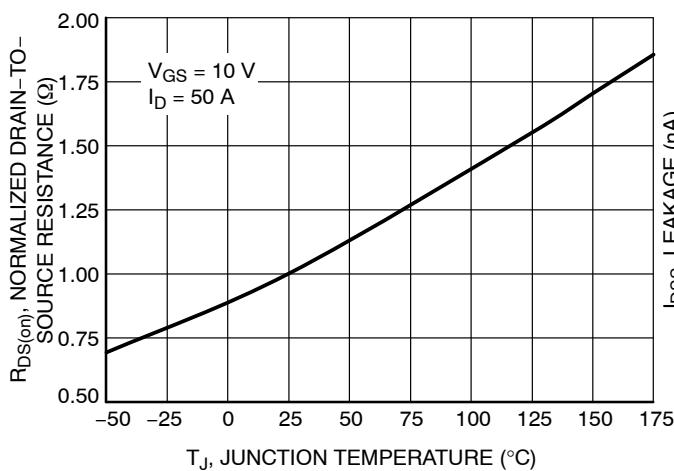


Figure 5. On-Resistance Variation with Temperature

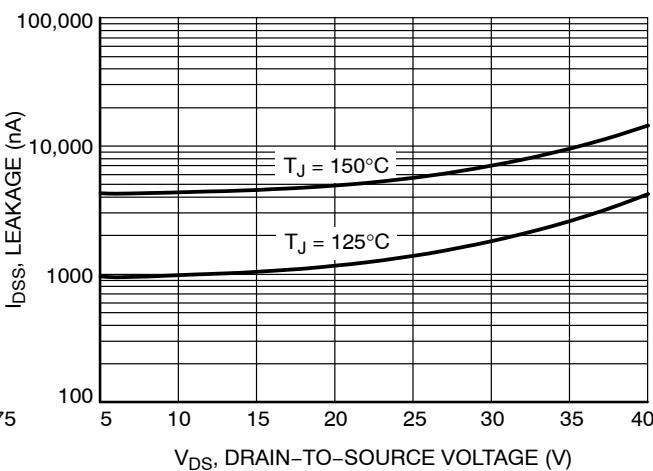
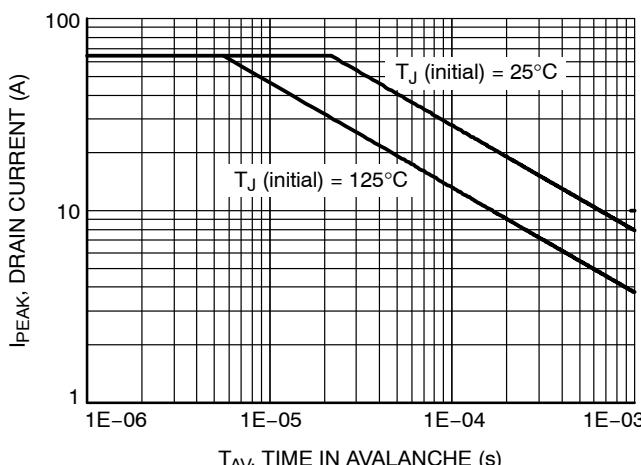
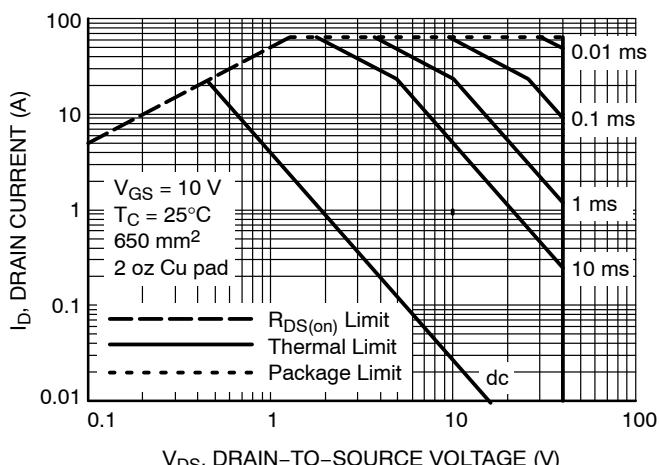
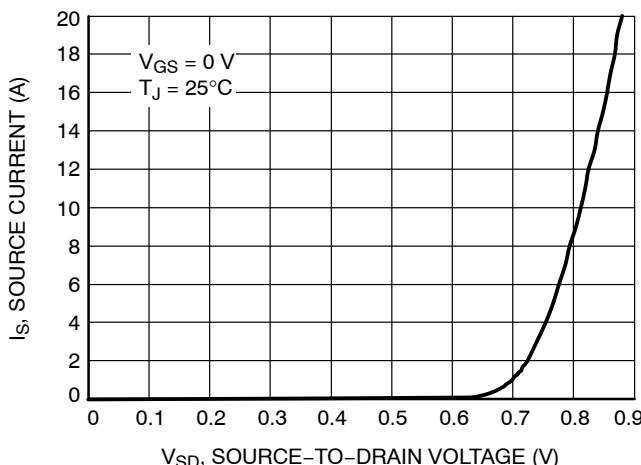
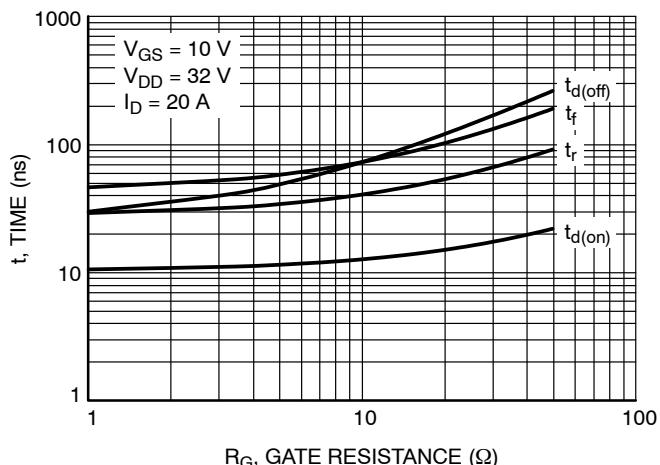
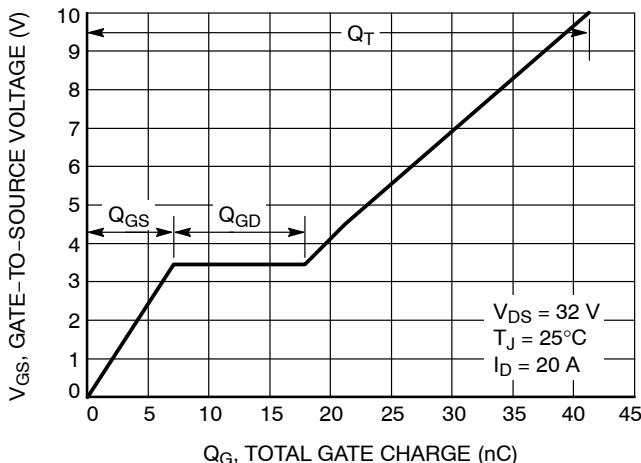
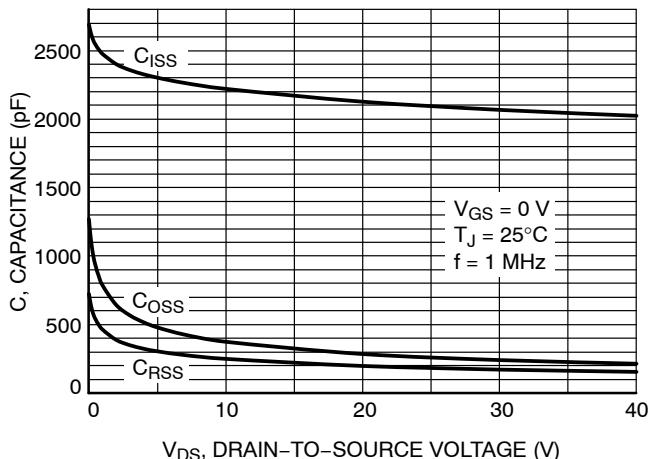
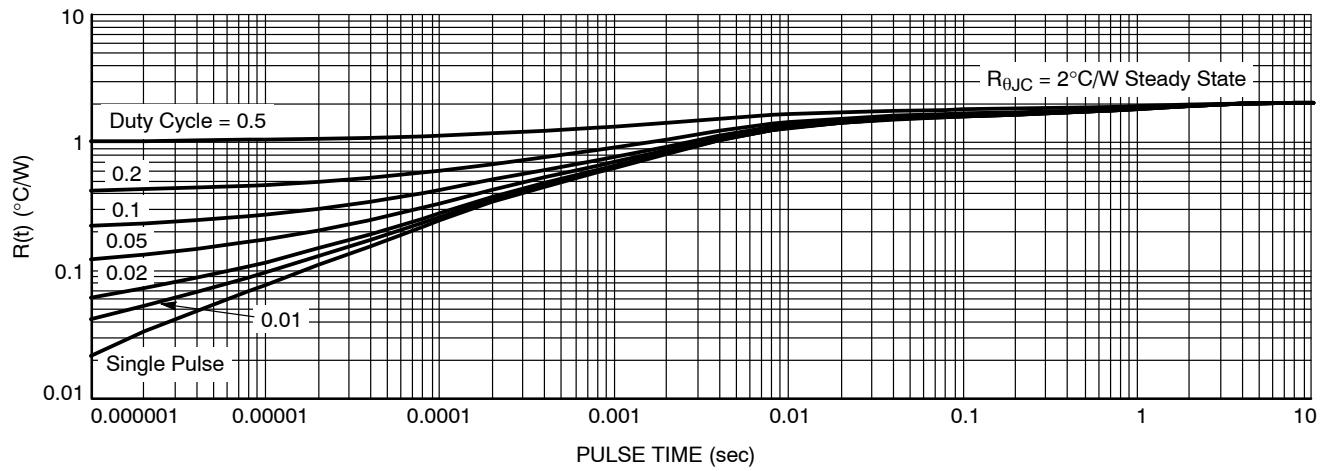


Figure 6. Drain-to-Source Leakage Current vs. Voltage

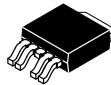
TYPICAL CHARACTERISTICS



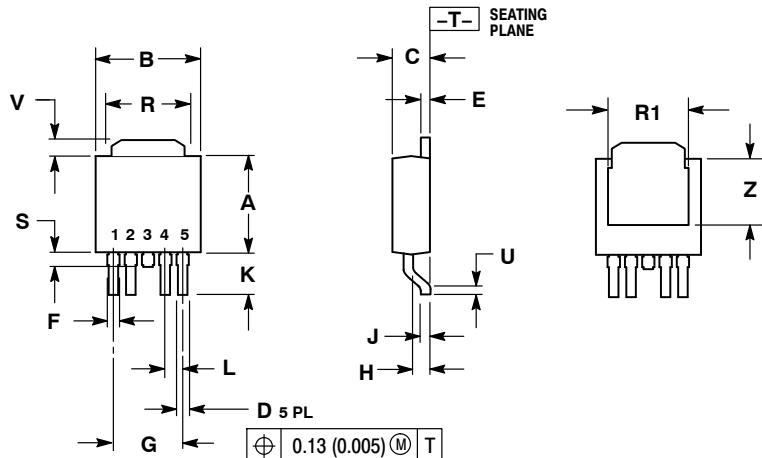
TYPICAL CHARACTERISTICS**Figure 13. Thermal Response**

**DPAK-5, CENTER LEAD CROP
CASE 175AA
ISSUE B**

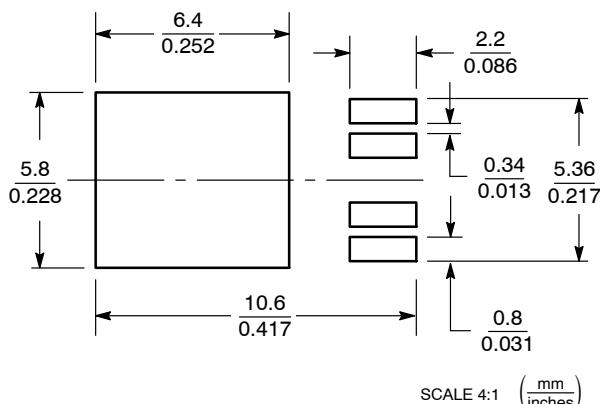
DATE 15 MAY 2014



SCALE 1:1



RECOMMENDED SOLDERING FOOTPRINT*



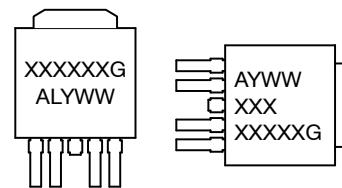
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180	BSC	4.56	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045	BSC	1.14	BSC
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

GENERIC MARKING DIAGRAMS*



IC Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb-Free indicator, "G" or microdot "■", may or may not be present

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