# NVDD5894NL

# Power MOSFET

## 40 V, 10 mΩ, 64 A, Dual N−Channel DPAK−5L

**Features**

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- High Current Capability
- Avalanche Energy Specified
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 40 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3) | Steady State | $T_C$ = 25°C | $I_D$ | 64 | A |
| | | $T_C$ = 100°C | | 45 | |
| Power Dissipation $R_{\theta JC}$ (Note 1) | | $T_C$ = 25°C | $P_D$ | 75 | W |
| | | $T_C$ = 100°C | | 38 | |
| Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3) | Steady State | $T_A$ = 25°C | $I_D$ | 14 | A |
| | | $T_A$ = 100°C | | 10 | |
| Power Dissipation $R_{\theta JA}$ (Notes 1 & 2) | | $T_A$ = 25°C | $P_D$ | 3.8 | W |
| | | $T_A$ = 100°C | | 1.9 | |
| Pulsed Drain Current | $T_A$ = 25°C, $t_p$ = 10 μs | | $I_{DM}$ | 324 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{stg}$ | −55 to +175 | °C |
| Source Current (Body Diode) | | | $I_S$ | 75 | A |
| Single Pulse Drain−to−Source Avalanche Energy ($T_J$ = 25°C, $I_{L(pk)}$ = 25 A, L = 0.3 mH) | | | $E_{AS}$ | 94 | mJ |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**THERMAL RESISTANCE MAXIMUM RATINGS**

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Case − Steady State (Drain) | $R_{\theta JC}$ | 2.0 | °C/W |
| Junction−to−Ambient − Steady State (Note 2) | $R_{\theta JA}$ | 40 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 $mm^2$, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

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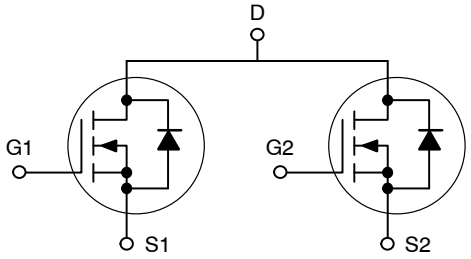
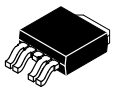
| $V_{(BR)DSS}$ | $R_{DS(on)}$ Max | $I_D$ Max |
|---|---|---|
| 40 V | 10 mΩ @ 10 V | 64 A |
| | 14.5 mΩ @ 4.5 V | |

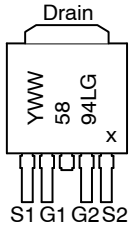
**Dual N−Channel**



**DPAK 5−LEAD**
**CASE 175AA**

**MARKING DIAGRAM & PIN ASSIGNMENT**




Y = Year
WW = Work Week
5894L = Specific Device Code
G = Pb−Free Package

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NVDD5894NLT4G | DPAK−5 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 40 | | | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 40 V | $T_J$ = 25°C | | | 1 | μA |
| | | | $T_J$ = 125°C | | | 100 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 4) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | | 1.5 | | 2.5 | V |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 50 A | | | 8.3 | 10 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 20 A | | | 11.2 | 14.5 | |
| Forward Transconductance | $g_{FS}$ | $V_{DS}$ = 15 V, $I_D$ = 10 A | | | 8.8 | | S |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, f = 1 MHz, $V_{DS}$ = 25 V | | | 2103 | | pF |
| Output Capacitance | $C_{oss}$ | | | | 259 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | | 183 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 32 V, $I_D$ = 20 A | | | 21 | | nC |
| | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 32 V, $I_D$ = 20 A | | | 41 | | |
| Threshold Gate Charge | $Q_{G(TH)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 32 V, $I_D$ = 20 A | | | 1.7 | | nC |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 6.9 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 11.3 | | |
| Plateau Voltage | $V_{GP}$ | | | | 3.5 | | V |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 32 V, $I_D$ = 20 A, $R_G$ = 2.5 Ω | | | 12.4 | | ns |
| Rise Time | $t_r$ | | | | 30.2 | | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | | 36 | | |
| Fall Time | $t_f$ | | | | 54 | | |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V, $I_S$ = 20 A | $T_J$ = 25°C | | 0.88 | 1.0 | V |
| | | | $T_J$ = 125°C | | 0.76 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, $dI_S/dt$ = 100 A/μs, $I_S$ = 20A | | | 22.8 | | ns |
| Charge Time | $t_a$ | | | | 11.2 | | |
| Discharge Time | $t_b$ | | | | 11.6 | | |
| Reverse Recovery Charge | $Q_{RR}$ | | | | 13.7 | | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

## TYPICAL CHARACTERISTICS

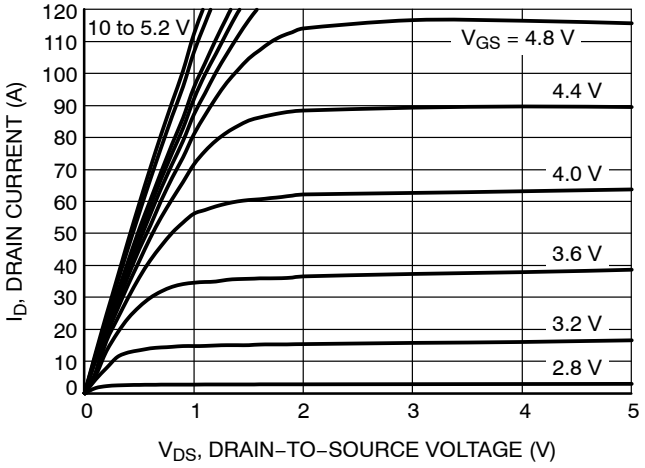



**Figure 1. On−Region Characteristics**

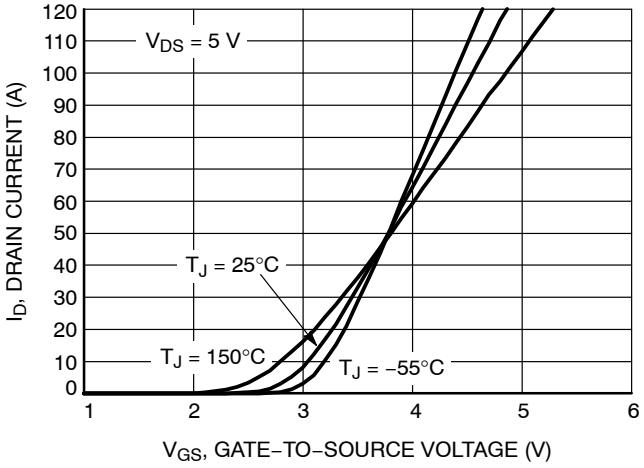



**Figure 2. Transfer Characteristics**

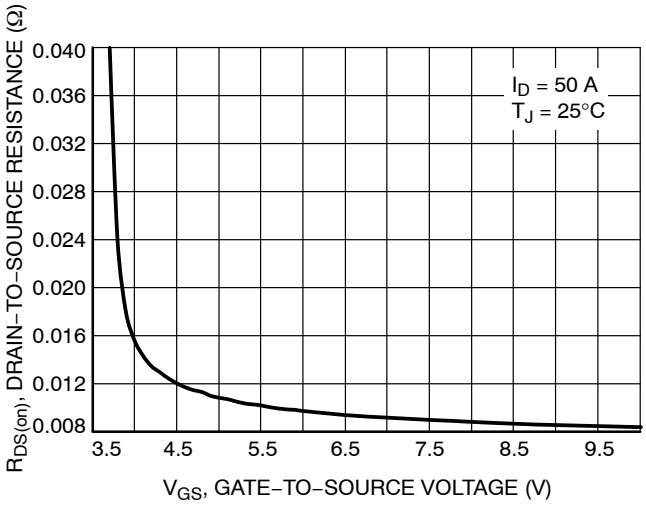



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

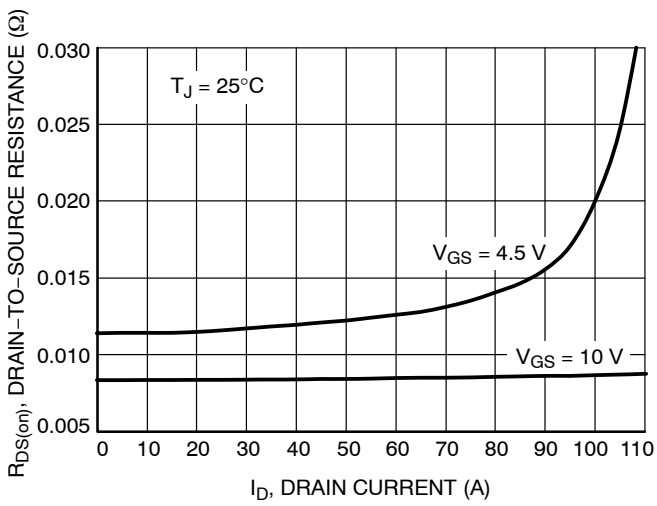



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

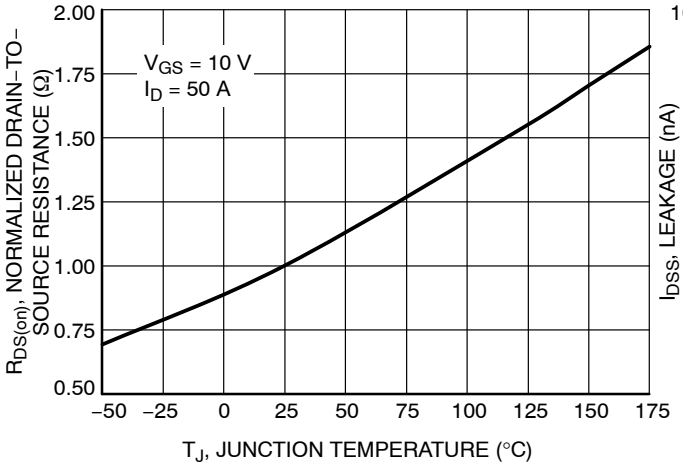



**Figure 5. On−Resistance Variation with Temperature**

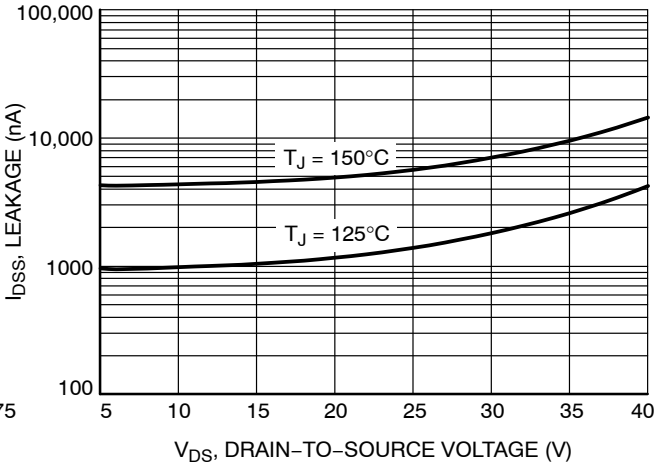



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL CHARACTERISTICS

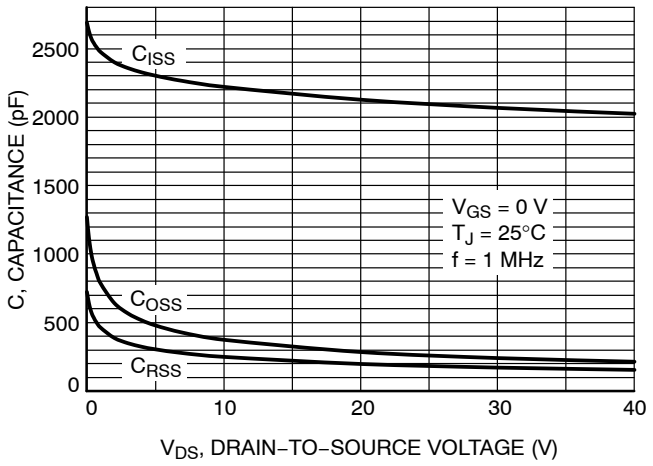



**Figure 7. Capacitance Variation**

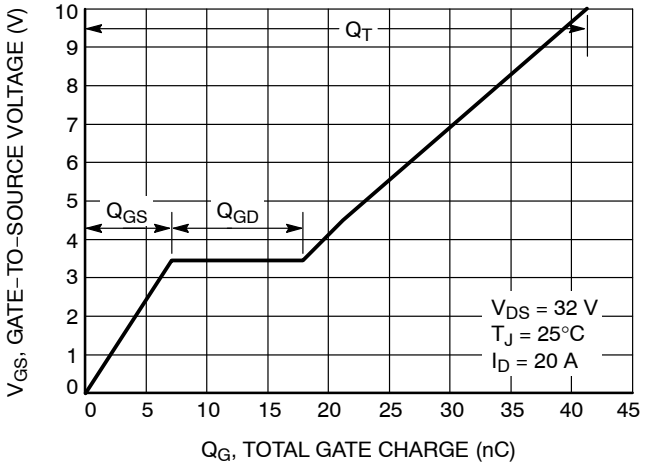



**Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

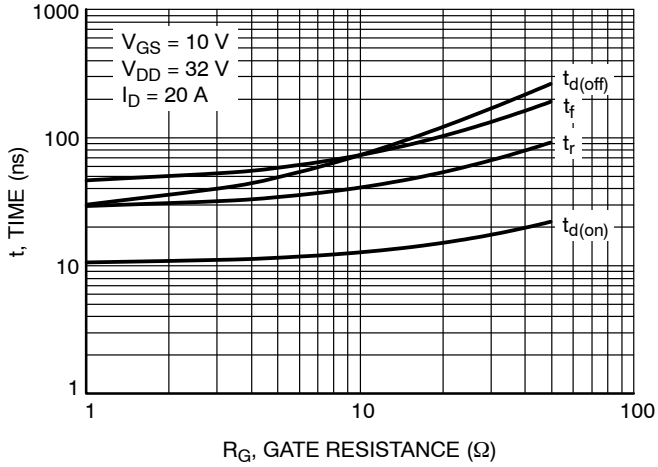



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

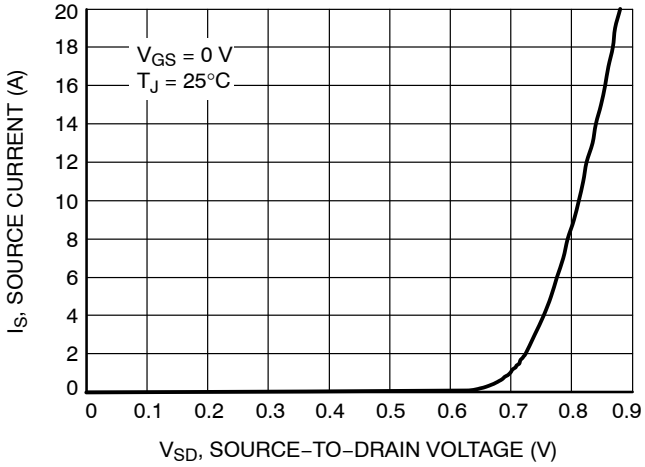



**Figure 10. Diode Forward Voltage vs. Current**

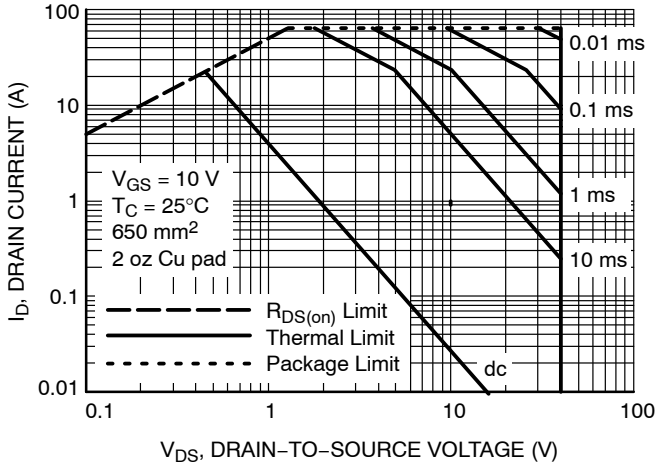



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

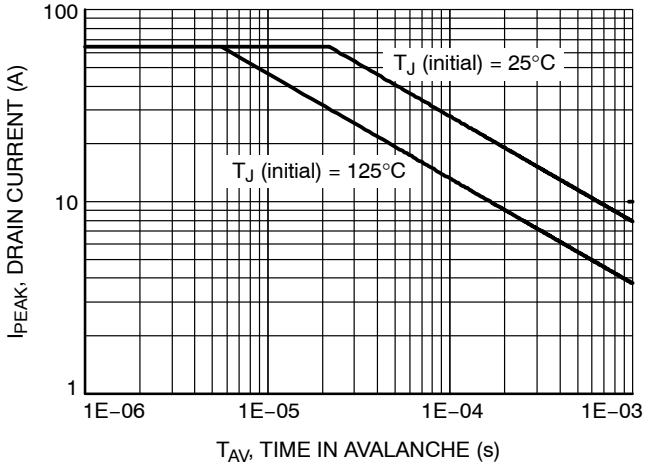



**Figure 12. Avalanche Characteristics**

## TYPICAL CHARACTERISTICS

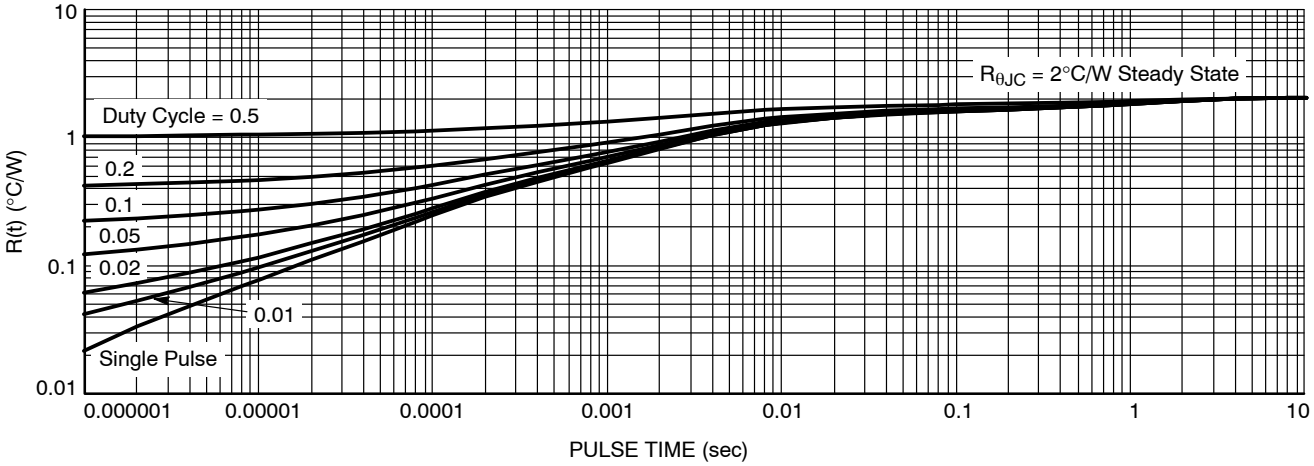



**Figure 13. Thermal Response**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

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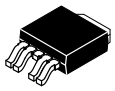
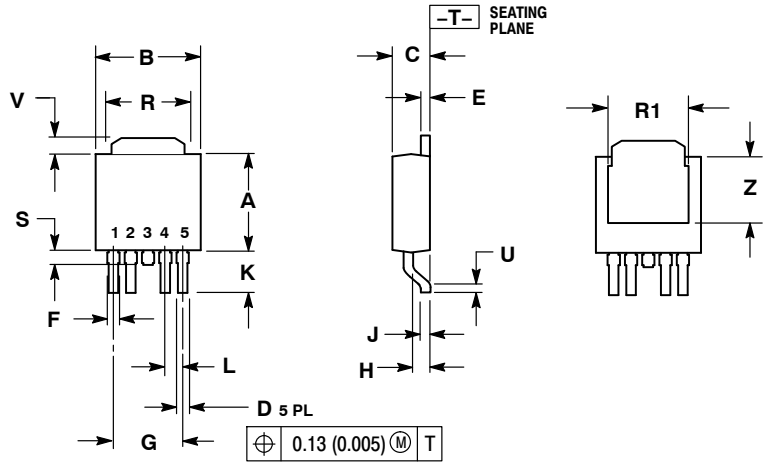


**DPAK−5, CENTER LEAD CROP**
CASE 175AA
ISSUE B

DATE 15 MAY 2014

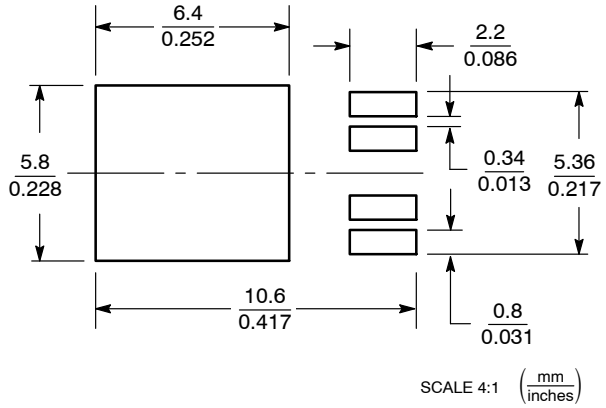
**SCALE 1:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.245 | 5.97 | 6.22 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.020 | 0.028 | 0.51 | 0.71 |
| E | 0.018 | 0.023 | 0.46 | 0.58 |
| F | 0.024 | 0.032 | 0.61 | 0.81 |
| G | 0.180 BSC | | 4.56 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.102 | 0.114 | 2.60 | 2.89 |
| L | 0.045 BSC | | 1.14 BSC | |
| R | 0.170 | 0.190 | 4.32 | 4.83 |
| R1 | 0.185 | 0.210 | 4.70 | 5.33 |
| S | 0.025 | 0.040 | 0.63 | 1.01 |
| U | 0.020 | −−− | 0.51 | −−− |
| V | 0.035 | 0.050 | 0.89 | 1.27 |
| Z | 0.155 | 0.170 | 3.93 | 4.32 |

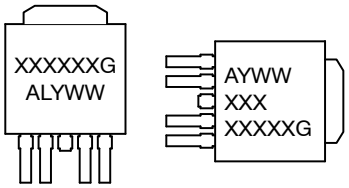
### RECOMMENDED SOLDERING FOOTPRINT*




SCALE 4:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAMS*




**IC** **Discrete**

| | |
|---|---|
| XXXXXX | = Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON12855D** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **DPAK−5 CENTER LEAD CROP** | **PAGE 1 OF 1** |

## PUBLICATION ORDERING INFORMATION

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Phone: 011 421 33 790 2910

**Europe, Middle East and Africa Technical Support:**
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For additional information, please contact your local Sales Representative

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