

NTLJD2104P

Power MOSFET

-12 V, -4.3 A, μ COOL™ Dual P-Channel, 2x2 mm, WDFN package

Features

- WDFN 2x2 mm Package with Exposed Drain Pads for Excellent Thermal Conduction
- Lowest $R_{DS(on)}$ in 2x2 mm Package
- Footprint Same as SC-88 Package
- Low Profile (<0.8 mm) for Easy Fit in Thin Environments
- Bidirectional Current Flow with Common Source Configuration
- These are Pb-Free Devices

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment
- Li Ion Battery Charging and Protection Circuits
- Dual High Side Load Switch

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	−12	V
Gate-to-Source Voltage			V _{GS}	±8.0	V
Continuous Drain Current (Note 1)	Steady State	T _J = 25°C	I _D	−3.5	A
		T _J = 85°C		−2.5	
	t ≤ 5 s	T _J = 25°C		−4.3	
Power Dissipation (Note 1)	Steady State	T _J = 25°C	P _D	1.5	W
	t ≤ 5 s			2.3	
Continuous Drain Current (Note 2)	Steady State	T _J = 25°C	I _D	−2.4	A
		T _J = 85°C		−1.7	
Power Dissipation (Note 2)			T _J = 25°C	P _D	0.7
Pulsed Drain Current	t _p = 10 μs		I _{DM}	−20	A
Operating Junction and Storage Temperature			T _J , T _{STG}	−55 to 150	°C
Source Current (Body Diode) (Note 2)			I _S	−1.5	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T _L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

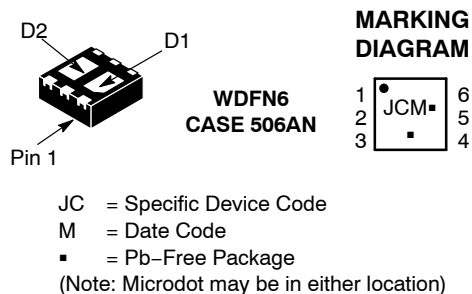
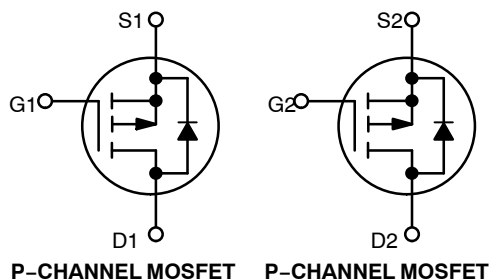
1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size of 30 mm², 2 oz. Cu.



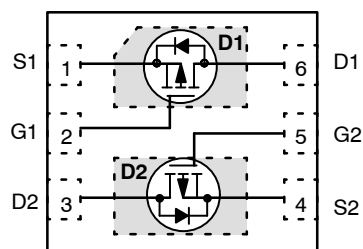
ON Semiconductor®

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$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
-12 V	60 m Ω @ -4.5 V	-3.0 A
	85 m Ω @ -2.5 V	-3.0 A
	110 m Ω @ -1.8 V	-0.7 A
	140 m Ω @ -1.5 V	-0.5 A
	190 m Ω @ -1.3 V	-0.2 A
	230 m Ω @ -1.2 V	-0.2 A



PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
SINGLE OPERATION (SELF-HEATED)			
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	83	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	177	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	54	

DUAL OPERATION (EQUALLY HEATED)

Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	58	°C/W
Junction-to-Ambient – Steady State Min Pad (Note 4)	$R_{\theta JA}$	133	
Junction-to-Ambient – $t \leq 5$ s (Note 3)	$R_{\theta JA}$	40	

3. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces).
4. Surface Mounted on FR4 Board using the minimum recommended pad size (30 mm², 2 oz Cu).

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = -250$ μ A	-12			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	$I_D = -250$ μ A, Ref to 25°C		-7.0		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -12$ V, $V_{GS} = 0$ V	$T_J = 25^\circ\text{C}$		-1.0	μ A
			$T_J = 85^\circ\text{C}$		-10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 8.0$ V			± 100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = -250$ μ A	-0.35	-0.6	-0.8	V
Gate Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			2.4		mV/°C
Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -4.5$, $I_D = -3.0$ A		60	90	m Ω
		$V_{GS} = -2.5$, $I_D = -3.0$ A		85	120	
		$V_{GS} = -1.8$, $I_D = -0.7$ A		110	150	
		$V_{GS} = -1.5$, $I_D = -0.5$ A		140	200	
		$V_{GS} = -1.3$, $I_D = -0.2$ A		190		
		$V_{GS} = -1.2$, $I_D = -0.2$ A		230		
Forward Transconductance	g_{FS}	$V_{DS} = -10$ V, $I_D = -3.0$ A		6.0		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C_{ISS}	$V_{GS} = 0$ V, $f = 1.0$ MHz, $V_{DS} = -6.0$ V		467		pF
Output Capacitance	C_{OSS}			125		
Reverse Transfer Capacitance	C_{RSS}			79		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5$ V, $V_{DS} = -6.0$ V, $I_D = -3.0$ A		5.5	8.0	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.3		
Gate-to-Source Charge	Q_{GS}			0.8		
Gate-to-Drain Charge	Q_{GD}			1.5		
Gate Resistance	R_G			12.2		

5. Pulse Test: Pulse Width ≤ 300 μ s, Duty Cycle $\leq 2\%$.
6. Switching characteristics are independent of operating junction temperatures.

NTLJD2104P

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -6.0\text{ V},$ $I_D = -3.0\text{ A}, R_G = 2.0\ \Omega$		6.6		ns
Rise Time	t_r			12.3		
Turn-Off Delay Time	$t_{d(OFF)}$			14		
Fall Time	t_f			16.2		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Recovery Voltage	V _{SD}	V _{GS} = 0 V, I _S = -1.0 A	T _J = 25°C		-0.7	-1.0	V
			T _J = 85°C		-0.65		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _{SD} /d _t = 100 A/μs, I _S = -1.0 A			23	45	ns
Charge Time	t _a				8.0		
Discharge Time	t _b				15		
Reverse Recovery Time	Q _{RR}				10	20	nC

5. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

6. Switching characteristics are independent of operating junction temperatures.

ORDERING INFORMATION

Device	Package	Shipping [†]
NTLJD2104PTBG	WDFN6 (Pb-Free)	3000 / Tape & Reel
NTLJD2104PTAG	WDFN6 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

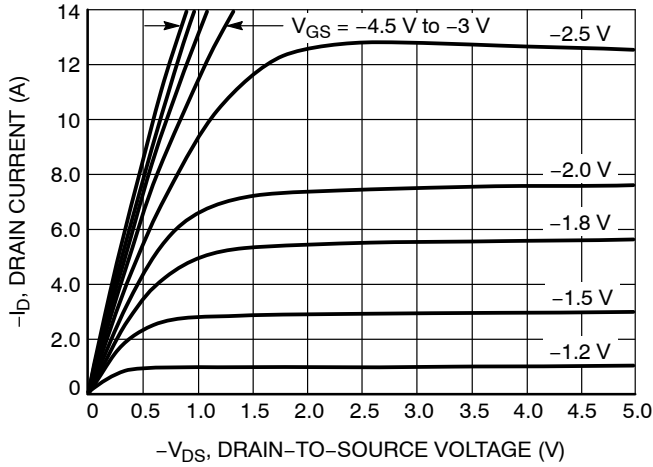


Figure 1. On-Region Characteristics

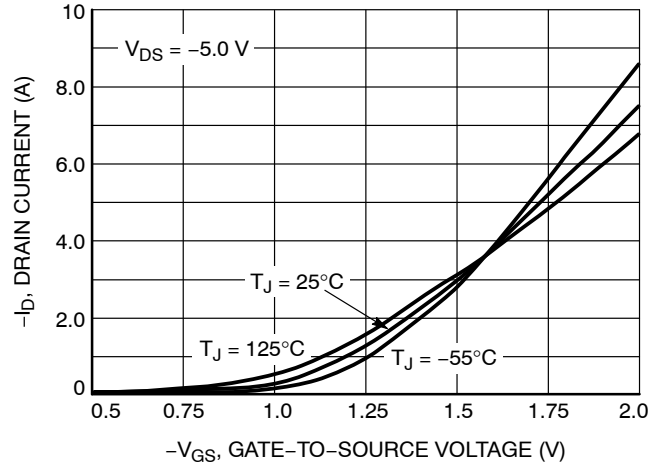


Figure 2. Transfer Characteristics

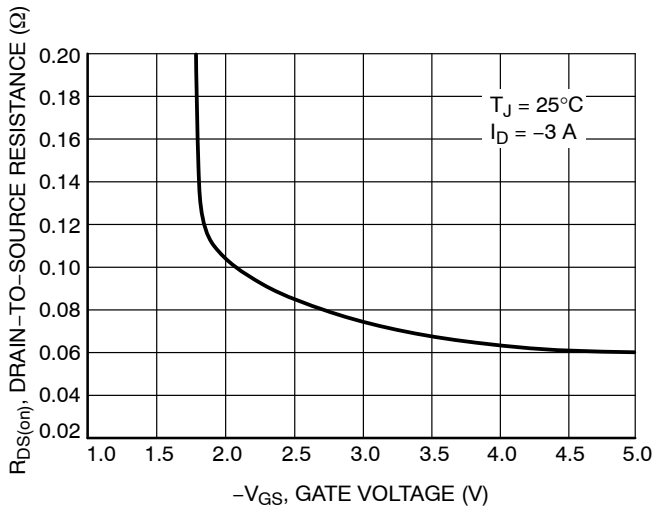


Figure 3. On-Resistance vs. Gate-to-Source Voltage

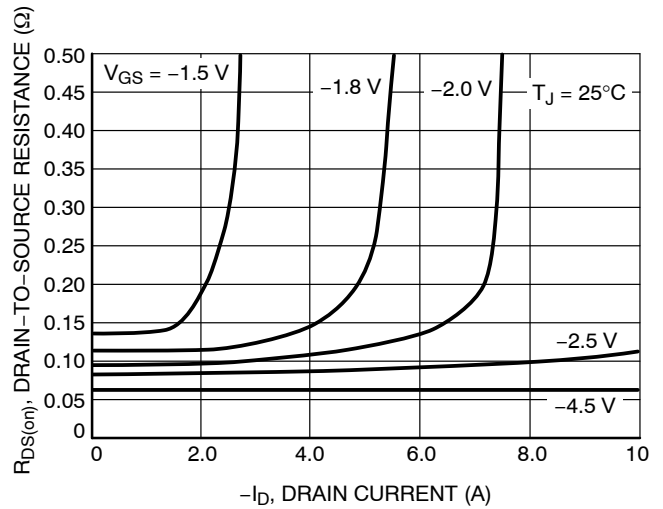


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

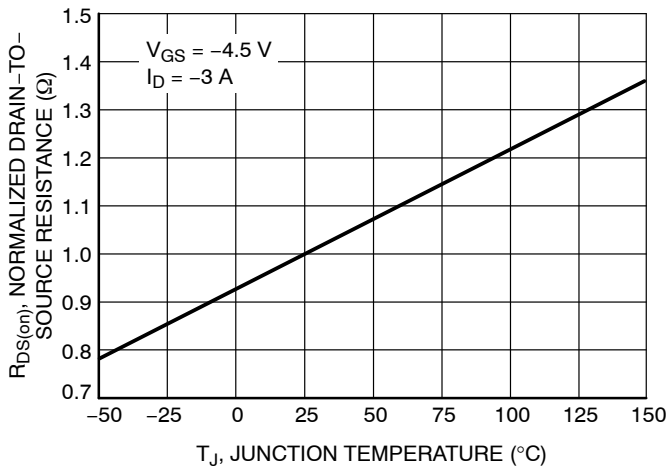


Figure 5. On-Resistance Variation with Temperature

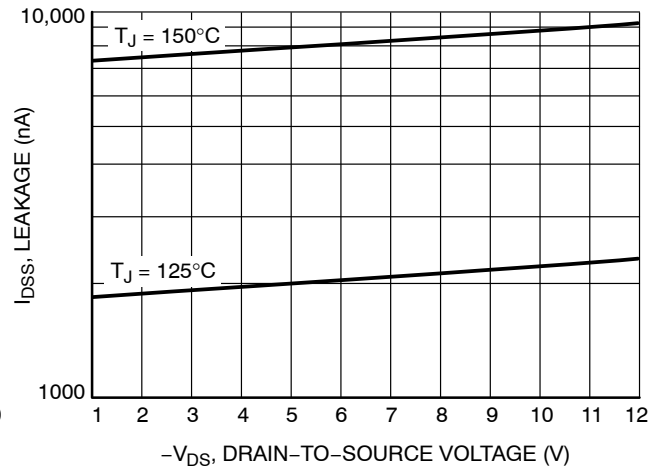


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

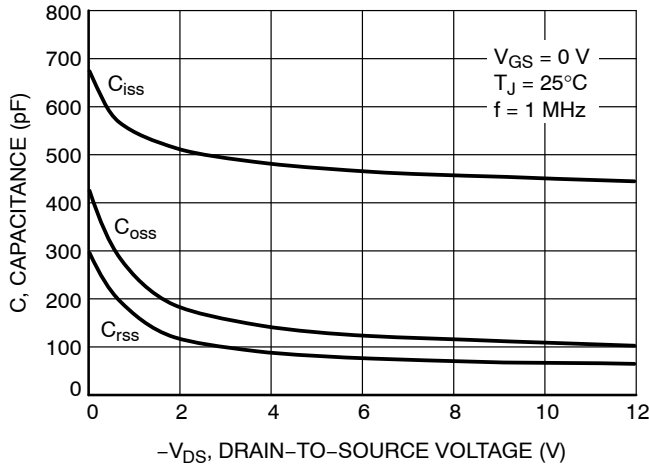


Figure 7. Capacitance Variation

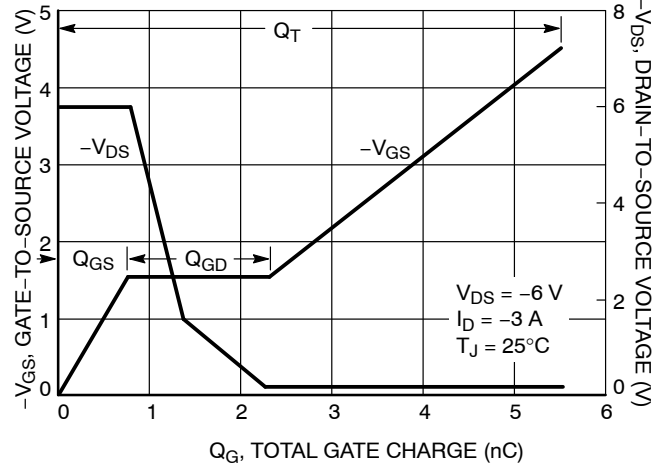


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

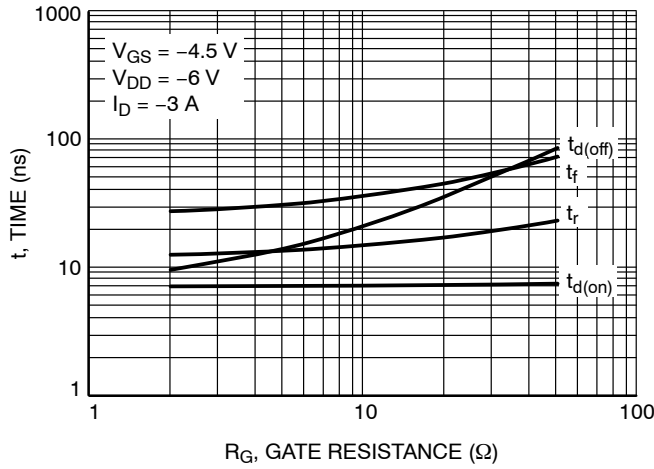


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

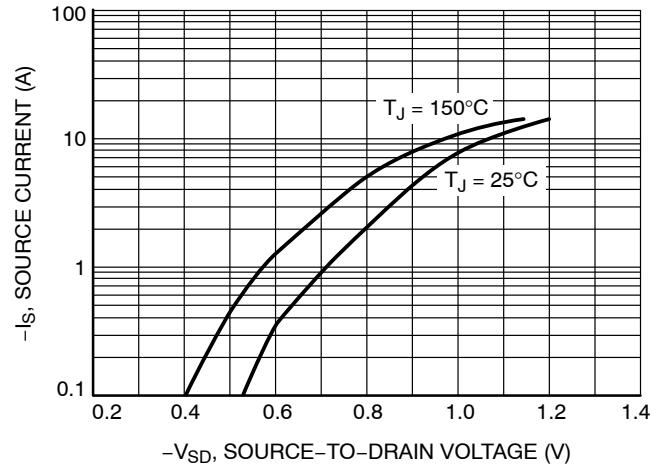


Figure 10. Diode Forward Voltage vs. Current

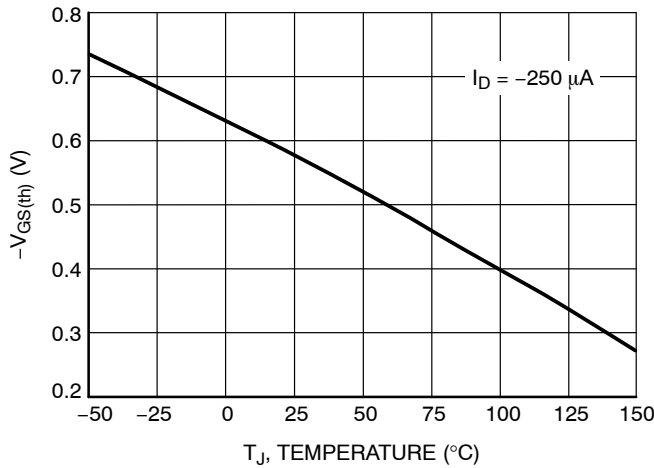


Figure 11. Threshold Voltage

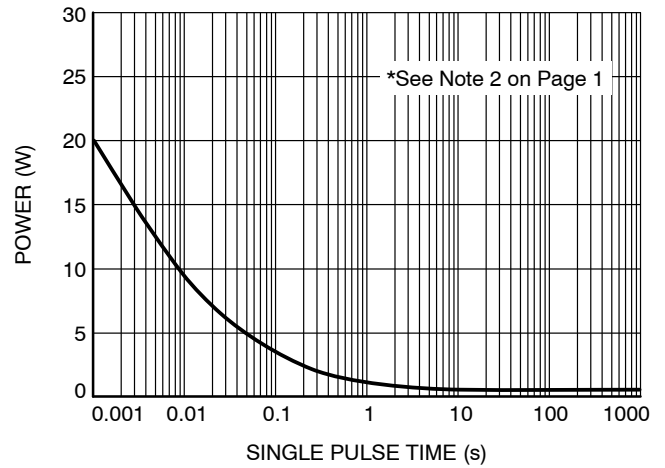


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS

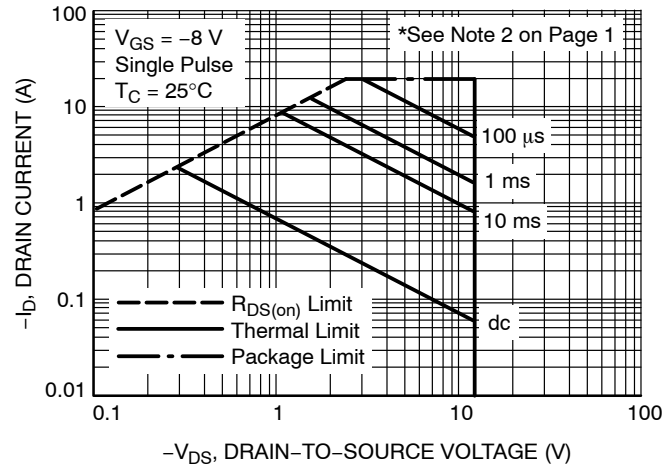


Figure 13. Maximum Rated Forward Biased Safe Operating Area

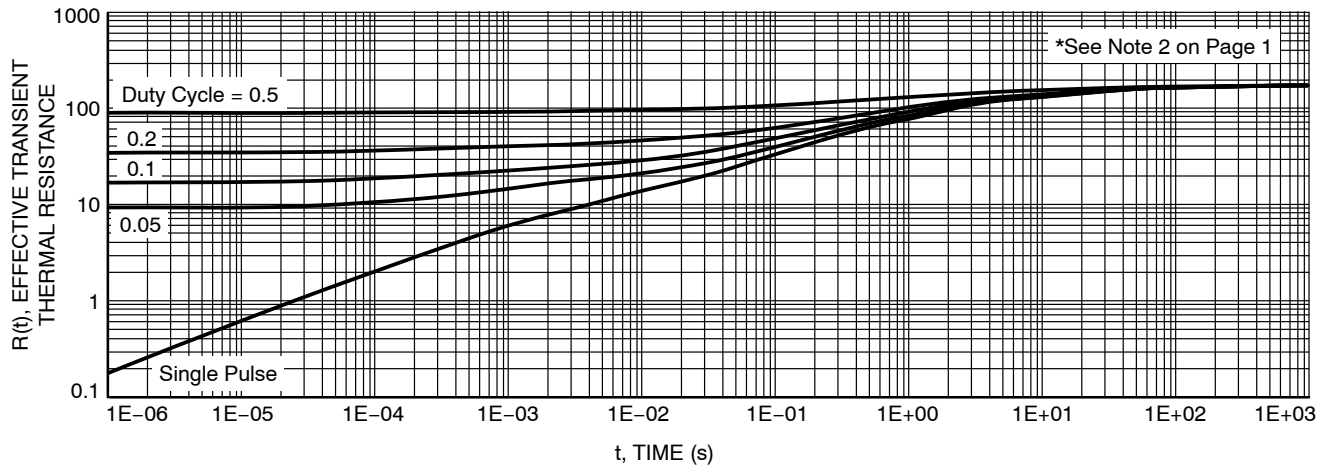
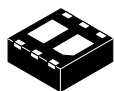


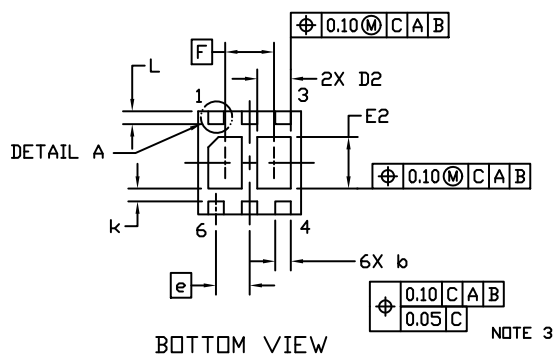
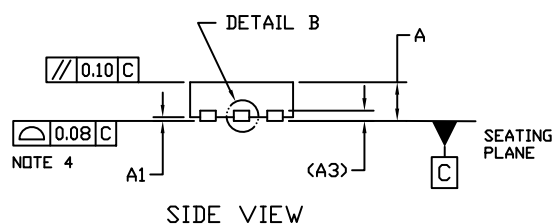
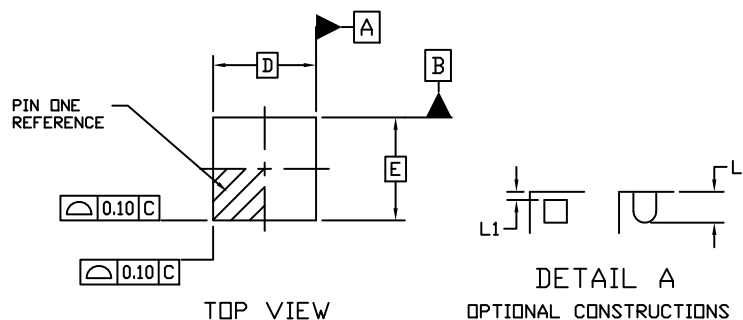
Figure 14. FET Thermal Response

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



WDFN6 2x2, 0.65P
CASE 506AN
ISSUE H

DATE 25 JAN 2022



GENERIC MARKING DIAGRAM*



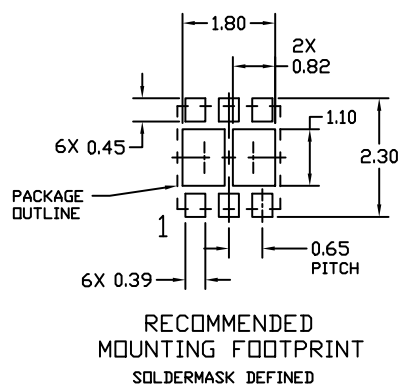
XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION **b** APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN.	MAX.
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.95 BSC	
k	0.25 REF	
L	0.20	0.30
L1	---	0.10



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DESCRIPTION:	WDFN6 2x2, 0.65P	PAGE 1 OF 1

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