GENERAL DESCRIPTION

OB6683 integrates a transition mode power factor correction (TM PFC) controller and a Quasi-Resonant (QR) controller in one chip. The PFC controller provides a cost effective solution for optimizing the power factor. The QR controller provides higher efficiency and lower EMI compared to conventional PWM system.

OB6683 provides high level integration and high performance than conventional PFC/PWM system. The built-in TM PFC controller optimizes power conversion efficiency with reduced system cost. The intelligent PFC switching ON and OFF, zero current detection and frequency limitation mechanism enable a better efficiency under any load conditions.

OB6683 features many built-in green functions to optimize power conversion efficiency at all power levels. This holds for QR operation at high power levels, as well as PFM operation at lower power levels, and 'Extended Burst Mode' operation at very low power or zero power (Standby) levels. At low power levels, OB6683 can turn off the PFC stage. In this way, low standby together with low system cost can be achieved.

The device is also integrated many functions of protection, such as X-CAP discharge, Brown-in/out protection, VCC Under Voltage Lockout (UVLO), Cycle-by-Cycle Current Limiting for PFC and QR Stage (OCP), Output Over Voltage Protection for PFC and QR Stage (OVP), Open Loop Protection for PFC and QR Stage (OLP), Programmable Over Temperature Protection (OTP), Built-in Soft Start in QR Stage, VCC Over Voltage Protection, Gate Clamp , Pin Floating Protection, and External Latch Triggering, etc. Therefore it can protect the system from damage due to occasional failure.

OB6683 is offered in SOP-16 packages.

FEATURES

- Integrated PFC Controller and QR Controller
- Transition Mode PFC Controller
- Multi-Mode Operation for QR Stage
- Line Voltage Compensation for QR Stage
- Enhanced Dynamic Response for PFC Stage
- PFC Light Load Turn Off Control
- Audio Noise Free Operation
- Valley Switching Operation with Valley lockout
- External Latch Triggering for Both Converters
- Minimum OFF time for Ringing Suppression
- Maximum ON Time Limit for QR Stage
- Built-in 4ms Soft Start for QR Stage
- Internal Leading Edge Blanking for QR Stage
- Internal Leading Edge Blanking for PFC Stage
- Built-in X-CAP Discharge

PROTECTIONS

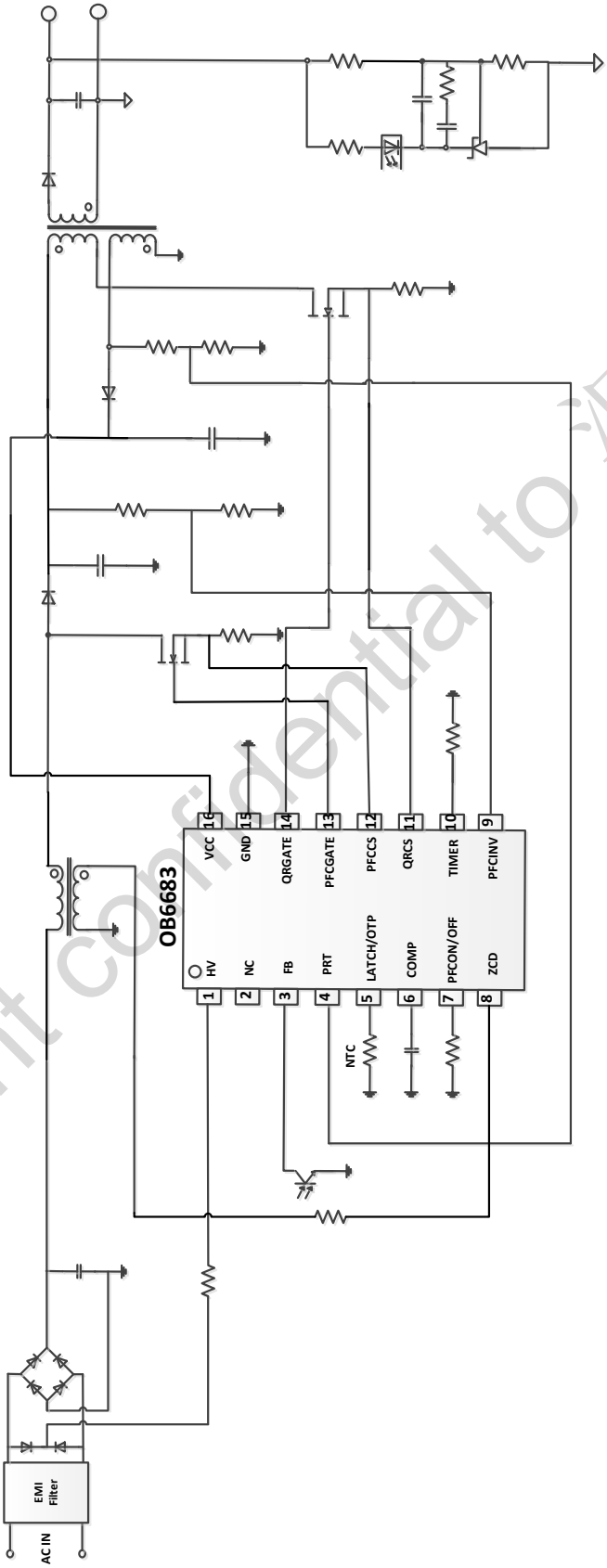
- Output Over Voltage Protection for PFC stage
- Output Over Voltage Protection for QR stage
- Output Diode Short Protection for QR stage
- VCC Over Voltage Protection
- Under Voltage Lockout with Hysteresis
- Over Load Protection for QR stage
- Cycle-by-Cycle Current Limiting for PFC stage
- Cycle-by-Cycle Current Limiting for QR stage
- Brownout Protection (BOP)
- PFC Inductor Short Circuit Protection
- Programmable Over Temperature Protection
- Internal Over Temperature Protection

APPLICATIONS

Offline AC/DC flyback converter for

- General LED Lighting
- LCD Monitor/TV/PC
- Notebook
- ACDC High Power Adapter
- Open Frame SMPS

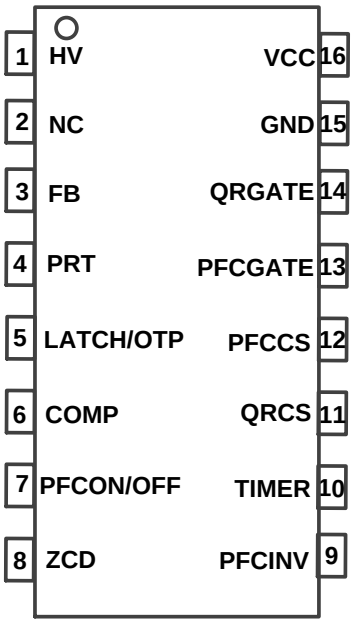
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The pin map of OB6683 SOP16 package is shown as below.



Ordering Information

Part Number	Description
OB6683CGP	16 Pin SOP, Halogen free in Tube
OB6683CGPA	16 Pin SOP, Halogen free in T&R

Package Dissipation Rating

Package	RθJA (℃/W)	RθJC (℃/W)
SOP16	99	14

Absolute Maximum Ratings

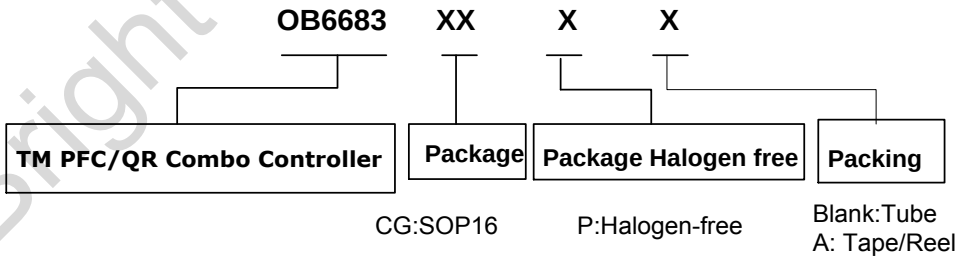
Parameter	Value
HV input Voltage	-0.3 to 700V
VCC input Voltage	30V
FB Input Voltage	-0.3 to 7V
PRT Input Voltage	-0.3 to 7V
LATCH/OTP Input Voltage	-0.3 to 7V
COMP Input Input Voltage	-0.3 to 7V
PFCON/OFF Input Voltage	-0.3 to 7V
ZCD Input Voltage	-0.3 to 7V
PFCINV Input Voltage	-0.3 to 7V
TIMER Input Voltage	-0.3 to 7V
QRCS Input Voltage	-0.3 to 7V
PFCCS Input Voltage	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-40 to 150 ℃
Min/Max Storage Temperature T_{stg}	-55 to 150 ℃
Lead Temperature (Soldering, 10secs)	260 ℃

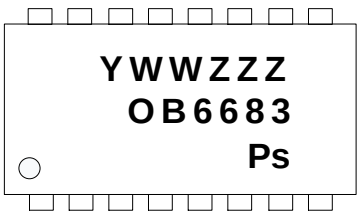
Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Recommended operating condition

Symbol	Parameter	Range
VCC	VCC Supply Voltage	12 to 25V

Marking Information





Y: Year Code

WW: Week Code (01-52)

ZZZ: Lot Code

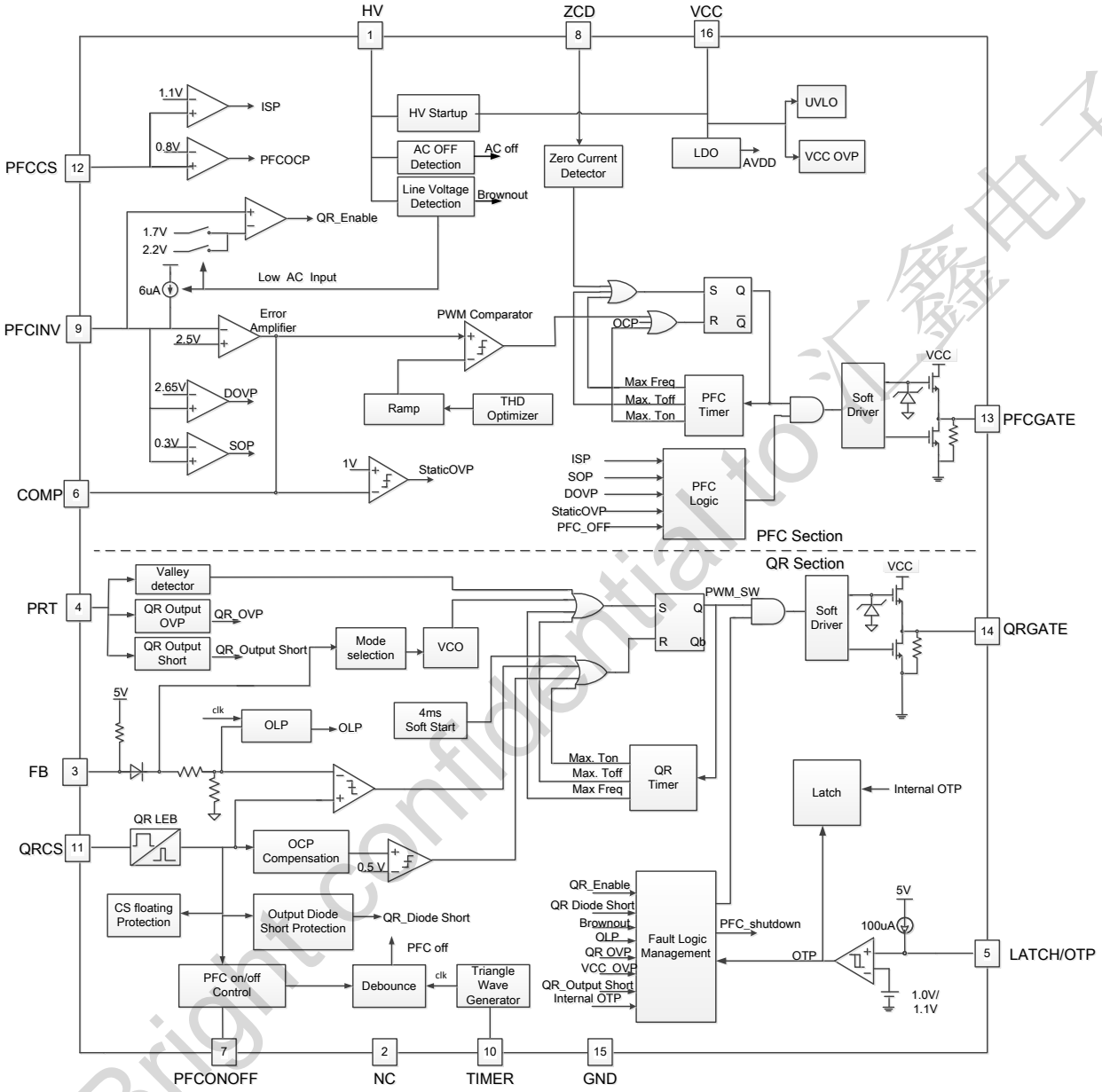
P:Halogen-free

s: Internal code

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	HV	I	Connected to the line input via resistors and diodes for startup and x-cap discharge, this PIN allows the brownout detection as well.
2	NC		No connect.
3	FB	I	Feedback input pin. The PWM duty cycle of QR stage is determined by voltage level into this pin and the current-sense signal at QRCS pin
4	PRT	I	Zero current detection and over voltage protection for QR stage
5	LATCH/OTP	I/O	External latch protection pin.
6	COMP	I/O	Output of the error amplifier for PFC voltage loop compensation
7	PFCON/OFF	I/O	Threshold voltage setting for PFC ON/OFF loading control
8	ZCD	I	Zero current detection for PFC stage.
9	PFCINV	I	Inverting input of the error amplifier (EA). The information at the output of the PFC stage is fed to the pin through a resistor divider.
10	TIMER	I/O	Timer setting for open loop protection and PFC light load turn off.
11	QRCS	I	QR stage current sense input pin.
12	PFCCS	I	PFC current sense input.
13	PFCGATE	O	PFC stage totem pole gate driver output.
14	QRGATE	O	QR stage totem pole gate driver output.
15	GND	P	Ground
16	VCC	P	Chip power supply pin.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

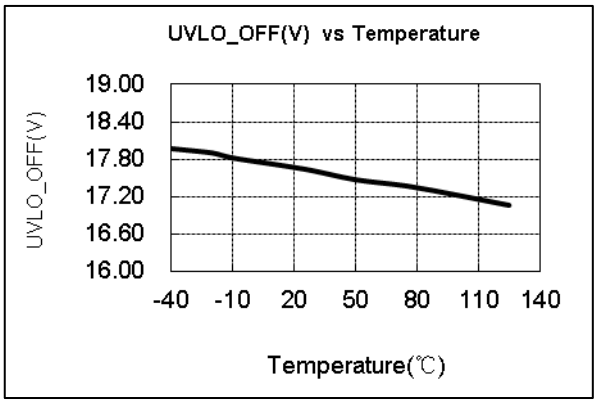
(T_A = 25℃, VCC=20V if not otherwise noted)

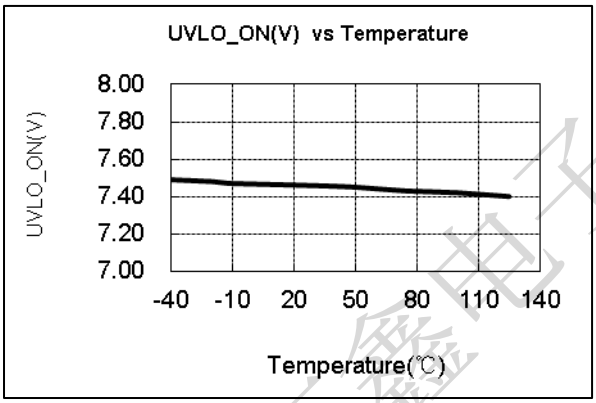
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
High Voltage Supply (HV pin)						
IHV1	High-Voltage Current Source for VCC startup	VCC =5V, Measure current into VCC	2			mA
IHV2	High-Voltage Current Source for VCC startup	VCC=0.5V,Measure current into VCC			0.85	mA
IHVXCAP	X-Cap Discharge Current			3		mA
VBNI	Brown-in level	HV resistor=20k ohm		79		V
VBNO	Brown-out level	HV resistor=20k ohm		70		V
Supply Voltage (VCC pin)						
I_VCC_op	Operation current with switching	VDD=20V,FB=2V,measure I(VCC),when two gates switching		2.5		mA
UVLO(ON)	VCC under voltage Lockout Enter		6.9	7.4	7.9	V
UVLO(OFF)	VCC under voltage lockout exit		15.2	16.2	17.2	V
VCC_OVP	VCC over voltage protection enter	Slowly ramp VCC, until no gate switching.	26.5	28	29.5	V
TD_rst	Restart time for protection occurs			1.4		s
PFC ON/OFF Voltage (PFC ON/OFF pin)						
I_PFCONOFF	Source current of PFCONOFF			106		uA
Over Temperature Protection (LATCH/OTP pin)						
I_OTP	Output current of LATCH/OTP pin			100		uA
VTH_OTP_in	OTP Enter Trip level			1.0		V
$V_{TH\_OTP\_off}$	OTP Exit Trip level			1.1		V
On Chip OTP (Internal Thermal Shutdown)						
Tshutdown	OTP Level			150		℃
Trecovery	OTP exit			125		℃
PFC Section						
Error Amplifier						
Vinv	Voltage Feedback Input Threshold		2.46	2.50	2.54	V
Iinv_source	Source current of PFCINV	VAC>165V			0.2	uA
	Source current of PFCINV	VAC<150V		6		uA
Gm	EA transconductance		150	200	-250	uS
Icomp	Max. EA output source current under normal operation			20		uA
	Max. EA output sink current under normal operation			20		uA
Vcomp	Upper Clamp Voltage			5.2		V
	Lower clamping voltage		0.85	0.95	1.05	V

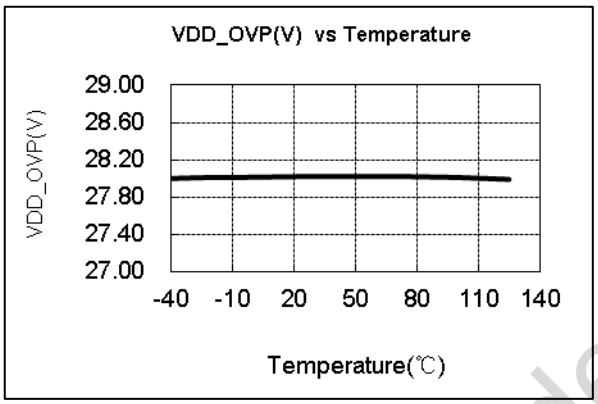
VQR_Enable	QR Start work Voltage	VAC>165V		1.7		V
	QR Start work Voltage	VAC<150V		2.2		V
PFC MAX ON/OFF Time						
Ton_pfc_max	Maximum on time		25	40	55	us
Toff_pfc_max	Maximum off time		40	60	80	us
Current Sense Comparator (PFC_CS pin)						
Vth_OCP	Low AC voltage input	VAC<150V		0.65		V
	High AC voltage input	VAC>165V		0.45		V
T_PFC_LEB	PFC leading edge blanking time			250		ns
Zero Current Detection (ZCD pin)						
Vth_ZCD	Input threshold voltage rising edge			1.2		V
Vzcd_hys	ZCD detection hysteresis voltage			0.5		V
SET PFC OFF debounce in Light Load(Timer)						
Tpfc_off	PFC turn off debounce time	R_{timerF}=51K ohm		1		s
PFC Over Voltage Protection (PFC OVP)						
Vth_pfc_ovp	INV threshold, PFC output over voltage protection (OVP)		2.55	2.65	2.75	V
Vpfc_ovp_hys	PFC OVP hysteresis			100		mV
Gate Driver for PFC (PFCDRIVER pin)						
VOL_PFC	PFC_OUT low level	Io = 30 mA			1	V
VOH_PFC	PFC_OUT high level	Io = 30 mA	7			V
V_Clamp_pfc	PFC_OUT clamping voltage	VCC=25V		11.7		V
Tr_pfc	PFC_OUT rising time	CL= 1nF at PFC_OUT		80		ns
Tf_pfc	PFC_OUT falling time	CL= 1nF at PFC_OUT		20		ns
QR Section						
Feedback Input(FB pin)						
VFB gain	VFB/VCS			4.5		V/V
VFB_Open	FB open loop voltage		4.5	5.0	5.5	V
ZFB_IN	Input impedance			30		KΩ
VFB_pfm	FB voltage in which system works in QR PFM mode			1.45 ~ 2.45		V
Vth_burst_H	The threshold exit burst mode			1.28		V
Vth_burst_L	The threshold enter burst mode			1.18		V
QR Current Sense Comparator (QRCS pin)						
V_{TH}_OCP	internal current limiting threshold			0.5		V
I_compensation	Only High AC flow into CS			100		uA
T_D_OC	QR OCP control delay	CL=1nF at QR_OUT		100		ns
T_QR_LEB	QR leading edge blanking time			300		ns
Demagnetization Detection (PRT pin)						
Voutput_ovp	Demagnetization comparator threshold voltage		2.85	3.0	3.15	V
Td_output_ovp	Hysteresis for PRT OVP comparator			7		Cycles

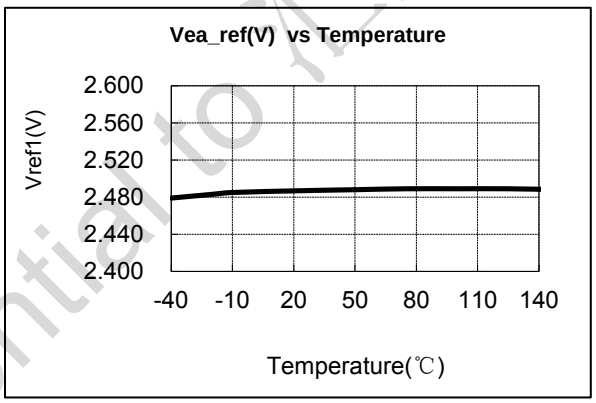
Td_ovp_blanking	Suppression of the transformer ringing at start of QR secondary stroke			2.2		us
V_{vally}	Valley detection threshold			80		mV
Voutshort	The threshold of output short			0.75		V
QR Soft Start						
Tss	soft startup time			4.0		ms
Oscillator for QR Switching Frequency						
F_QR_burst	Burst mode switching frequency			22		KHz
F_QR_max	Maximum QR frequency			120		KHz
Favg_inc	The frequency threshold of increasing valley			90		KHz
Favg_dec	The frequency threshold of decreasing valley			55		KHz
F_QR_min	Minimum QR frequency			50		KHz
Ton_QR_max	Maximum on time			15		us
QR Over Load Protection (QR OLP)						
V_{TH}_PL	Power Limiting FB Threshold Voltage			4.4		V
T_D_PL	Power limiting Debounce Time	R_{timerF}=51K ohm		60		ms
Gate Driver for QR (QR_OUT pin)						
VOL_QR	QR_OUT low level	Io = 30 mA			1	V
VOH_QR	QR_OUT high level	Io = 30 mA	7			V
V_Clamp_qr	QR_OUT clamping voltage	VCC=25V		11.7		V
Tr_qr	QR_OUT rising time	CL = 1nF at QR_OUT		200		ns
Tf_qr	QR_OUT falling time	CL= 1nF at QR_OUT		50		ns

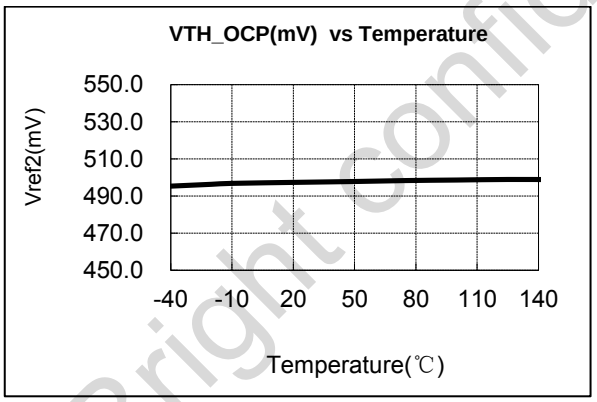
CHARACTERIZATION PLOTS

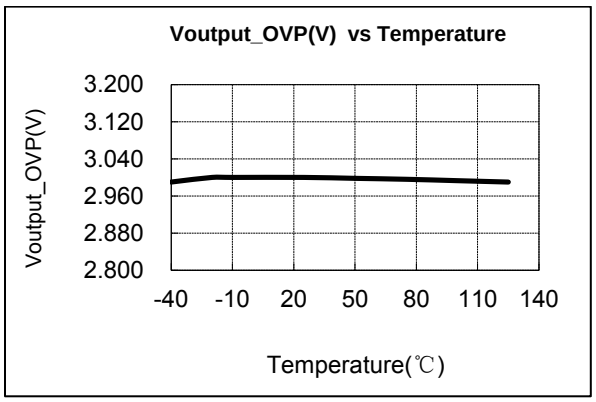


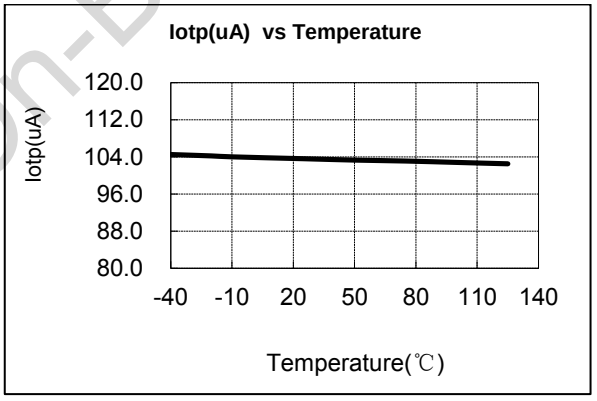


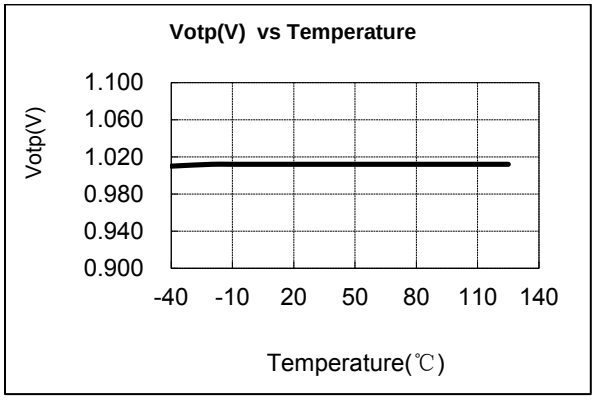












OPERATION DESCRIPTION

GENERAL CONTROL AND FEATURE

Integrated TM PFC Controller and QR Controller in One Chip

OB6683 integrates a transition mode power factor collection (TM PFC) controller and a quasi-resonant (QR) controller in one chip.

In TM PFC control, the inductor current is allowed to completely go to zero before the next switching cycle of the power MOSFET is initiated. Therefore, the reverse recovery loss of output boost diode is minimized. Also TM PFC can provide low harmonic distortion and high power factor.

Quasi-Resonant (QR) control can provide lower EMI and higher power conversion efficiency compared to conventional hard-switched converter with a fixed switching frequency.

The built-in advanced energy saving with high level protection features of OB6683 provide simple and cost effective solutions for the power supplies of 75 Watts or greater.

Internal High-Voltage Startup Circuit and UVLO

The traditional circuit provides the startup current through a startup resistor to power up the PWM controller. However, it consumes too much power to meet the power saving requirement. OB6683 is implemented with a high-voltage startup circuit to minimize power loss on startup circuit. During a startup phase, a high voltage current source sinks current from AC Line or Neutral to provide the startup current and charge the VCC capacitor. The resistor connected to HV recommended for 20K.

An UVLO comparator is embedded to detect the voltage across VCC pin to ensure the supply voltage is high enough to power on the OB6683 and in addition to drive the power MOSFET.A hysteresis is provided to prevent the OB6683 shutdown by the voltage dip during startup

During the start-up, the HV pin voltage rises and the VCC capacitor is charged, as shown in Figure1. When the HV voltage reaches VBNI (typically 79V), the PFC section of the chip starts to work. The PFCGATE start to switch after Tdelay time. Consequently, the PFCINV voltage starts to rise. When the PFCINV voltage reaches VQr_Enable, the QR section of the chip starts to work and QRGATE start to switch.

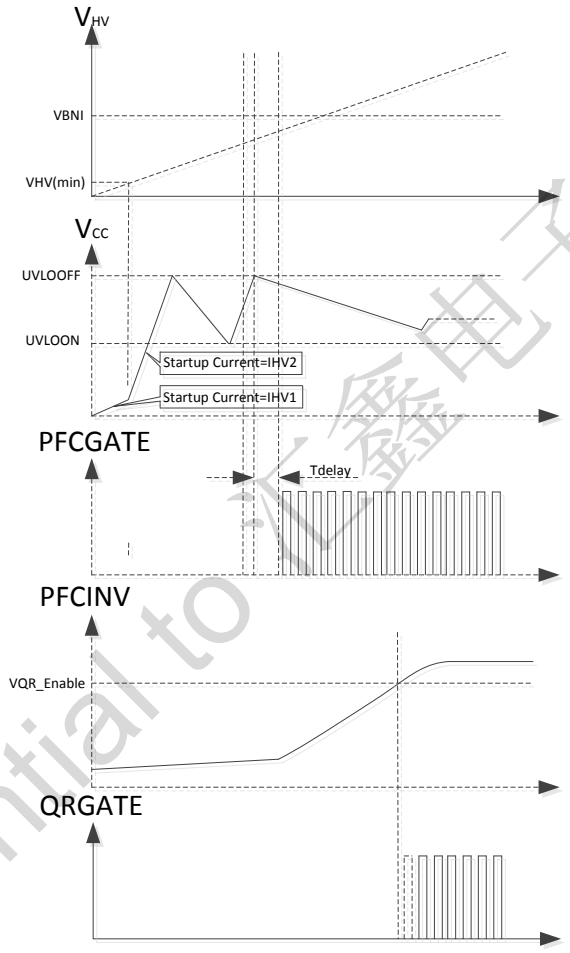


Figure 1

Over Temperature Protection with Latch Shutdown (LATCH/OTP pin)

A NTC resistor in series with a regular resistor should be connected between LATCH/OTP pin and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal 100uA current source flowing through the resistors, the voltage at LATCH/OTP pin becomes lower at high temperature. The internal OTP circuit is triggered and shuts down the MOSFET when the sensed input voltage is lower than 1.0V. OTP is a latched shutdown.

External latch trip point

By externally forcing a level on pin LATCH/OTP (e.g.., with a signal coming from a temperature sensor) less than 1.0V, OB6683 can be permanently latched-off.

FUNCTIONAL DESCRIPTION for TM PFC

Error Amplifier

Connected to a resistor divider from output line, the inverting input of the Error Amplifier (EA) is

compared to an internal reference voltage (2.5V) to set the regulation on output voltage.
The EA output is externally connected for loop compensation. It is usually realized with a type II filter which connected between the ground and EA output. The system loop bandwidth is set below 20 Hz to suppress the AC ripple of the line voltage.

Zero Current Detection (ZCD pin)
OB6683 performs zero current detection (ZCD) by using an auxiliary winding of the PFC boost inductor in series with an external resistor. When the stored energy of the PFC boost inductor is fully released to the output, the voltage at ZCD pin decreases. When ZCD pin voltage falls below 0.7V, an internal ZCD comparator is triggered and a new PFC switching cycle is initiated following the ZCD triggering. If no zero current triggering signal is detected on ZCD pin, OB6683 will generate a restart signal in 60 usec (typ.) after the last PFC driver signal.

Output Overvoltage Protection
OB6683 offers two level OVP protection including dynamic OVP for output fast transient protection and static OVP for output stead-state protection.
When output voltage exceeds 424V which correspond to a INV voltage larger than 2.65V, the GATE output is turned off and OB6683 is disabled. Only when INV voltage reach below 2.55V, the operation of OB6683 is resumed.
When DOVP event lasts long enough, the Error Amplifier Output, COMP, will saturate and stay low. Static OVP comparator is activated and power MOSFET Gate is off when COMP voltage is dropped below 1V. Normal operation is resumed when Error Amplifier goes back to its linear region after output voltage drops.

Current Sensing Comparator and Leading Edge Blanking
Cycle-by-cycle current limiting is provided in OB6683's peak current mode control. The switch current is detected by a sense resistor into the sense pin. The switch-on spike is blanked out via an internal leading edge blanking (LEB) circuit. Another extra function of LEB is that it limits the system minimum on time, thus the THD of system at light load will be decreased.
The RS flip-flop ensures that only one single switch-on and switch-off pulse appears at the gate drive output during a given cycle..

PFC Gate Driver (PFCGATE Pin)
The output stage is designed to ensure zero cross-conduction current. This minimizes heat dissipation, increase efficiency, and enhance reliability. The output driver is also slew rate controlled to minimize EMI. The built-in 11.7V clamp at the gate output protects the MOSFET gate from high voltage stress.

FUNCTIONAL DESCRIPTION for QR

Multi-Mode Operation for QR
OB6683 integrates a multi-mode QR controller. The QR controller changes the mode of operation according to FB voltage, which reflects the line and load conditions, as shown in Figure2. The operation valley (1^{st},2^{nd},3^{rd},4^{th},5^{th},6^{th},7^{th},8^{th}) is locked once the valley is selected.

■ Under normal operating conditions (FB>2.45V), the system operates in QR mode. The frequency varies depending on the line voltage and the load conditions. Therefore, the system may actually work in DCM when 120KHz frequency clamping is reached. System design should be optimized such that the operation frequency is within the range specified at full loading conditions and in universal AC line input range.

■ At light load condition (1.45V<VFB<2.45V, the system operates in PFM (pulse frequency modulation) mode for high power conversion efficiency. In PFM mode, the "ON" time in a switching cycle is fixed and the system modulates the frequency according to the load conditions. Generally, in flyback converter, the decreasing of loading results in voltage level decreasing at FB pin. The controller monitors the voltage level at FB and control the switching frequency. However, the valley switching characteristic is still preserved in PFM mode. That is, when loading decreases, the system automatically skip more and more valleys and the switching frequency is thus reduced. In such way, a smooth frequency foldback is realized and high power conversion efficiency is achieved.

■ At zero load or very light load conditions , the system operates in On-Bright's proprietary "extended burst mode". In this condition, voltage at FB is below burst mode threshold level, Vth_burst_L. The Gate drive output switches only when VCC voltage drops below a preset level or FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extend. In extended burst mode, the switching frequency is fixed to 22KHz, in this way, possible audio noise is eliminated.

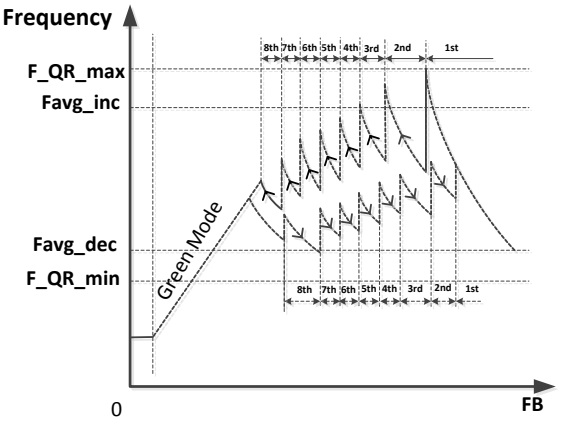


Figure 2

QR Demagnetization Detection (PRT pin)

The transformer core demagnetization is detected by monitoring the voltage activity on the auxiliary windings through PRT pin. This voltage features a flyback polarity. A new cycle starts when the power switch is activated, as shown in Fig.3. After the on time (determined by the QRCS voltage and FB), the switch is off and the flyback stroke starts. After the flyback stroke, the drain voltage shows an oscillation with a frequency of approximately $1/2\pi\sqrt{L_pC_d}$, where L_p is the primary self inductance of the transformer and C_d is the capacitance on the drain node.

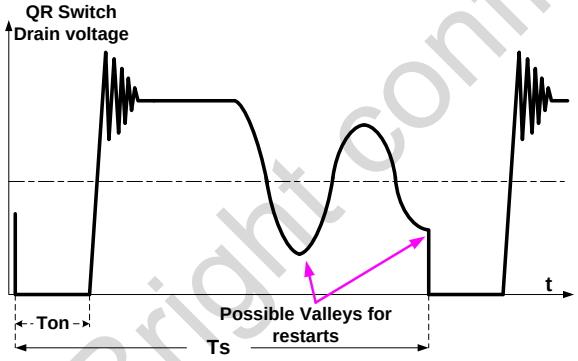


Figure 3

The typical detection level is fixed at 80mV at the PRT pin. Demagnetization is recognized by detection of a possible “valley” when the voltage at PRT is below 80mV in falling edge. PRT detection is suppressed during the ringing suppression time.

QR Current Sensing and Leading Edge Blanking (QR_CS pin)

Cycle-by-Cycle current limiting for the QR stage is offered in OB6683. The switch current is detected by a sense resistor into the QRCS pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state, the QR current limit comparator is disabled and cannot turn off the external MOSFET during the blanking period.

Built-in Soft Start for QR

The QR controller of OB6683 features a built-in 4ms soft start to soften the constraints occurring in the power supply during startup. It is activated after QR stage is enabled. As soon as QR stage begins to work after power on, the threshold voltage at QRCS pin is gradually increased from nearly zero to the maximum clamping level 0.5V in 4ms. Every system restart attempt is followed by a QR soft start sequence.

Ringing Suppression Timer

A ringing suppression timer Tsupp is implemented in the QR controller of OB6683. In normal operation, Tsupp starts when QRCS reaches the feedback voltage FB, the gate drive QRDRIVER is set to low. During Tsupp, gate drive QRDRIVER remains in low state and cannot turn power switch on again. The ringing suppression is necessary in applications where the transformer has a large leakage inductance, particularly at low output voltages or startup. In OB6683, the ringing suppression timer Tsupp is set to 2us internally.

Maximum Frequency Clamp in QR operation

According to the QR operation principle, the switching frequency is inversely proportional to the output power. Therefore, when the output power decreases, the switching frequency can become rather high without limiting. To meet EMI limit starting at 150KHz, the maximum switching frequency in OB6683 is internally limited to -120KHz.

Valley Lockout Operation

The operating frequency of a traditional QR flyback controller is inversely proportional to the system load. In other words ,a load reduction increases the operating frequency. A maximum frequency clamp can be useful to limit the operating frequency range. However, when used by itself, such an approach often causes instability since when this clamp is active, the controller tends to jump between two valleys, thus generating audible noise.

Instead, the OB6683 also incorporates a valley lockout circuitry to eliminate valley jumping. Once a valley is selected, the controller stays locked in this valley until the output power changes significantly.

Suppose the system works at the nth valley. when nth < = 8, the valley locking function is active. When n > 8, the function is disable..

When the system is locked at the nth (n <= 8) valley bottom, if the load is reduced, the frequency will rise. When the frequency is up to Favg_inc

(typically 90kHz), the timer inside the chip starts to count. When the timer is full, the chip will skip one more valley, and the system works at the nth + 1 valley. On the contrary, if the load increases, when the working frequency of the system will decrease. When the frequency is down to Favg_dec(typically 55KHz), the timer internally starts to count. When the timer is full, the system works at the nth-1 valley. If the system is open-loop, the chip automatically works at the first valley.

QR OCP Compensation

A proprietary OCP compensation for QR stage is provided for better OCP performance in the universal input range. There is 100uA current flowing from QRCS pin at high AC input. In this way, OCP point difference between high line input and low line input is minimized by adjusting the resistor between QRCS and MOSFET source.

QR Output Over Voltage Protection (PRT pin)

An output over voltage protection is implemented by sensing the auxiliary winding voltage at PRT pin during the flyback phase. The auxiliary winding voltage is a well-defined replica of the output voltage. The QR OVP works by sampling the plateau voltage at PRT pin during the flyback phase, as shown in Fig.4. A 2 us internal delay (plateau sampling) guarantees a clean plateau, provided that the leakage inductance ringing has been fully damped.

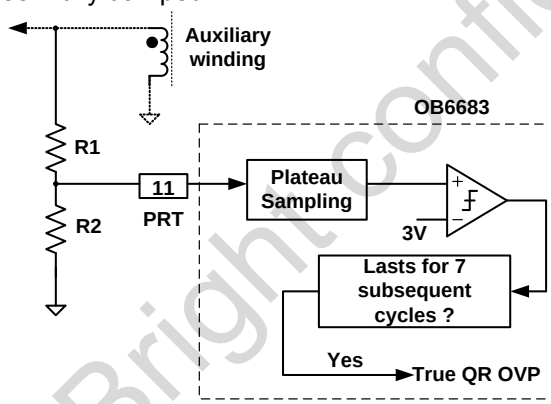


Figure 4

If the sampled plateau voltage exceeds the OVP trip level (3.0V), an internal counter starts counting subsequent OVP events. If OVP events are detected in successive 7 cycles, the controller assumes a true OVP and stops all switching operations. The counter has been added to prevent incorrect OVP detection which might occur during ESD or lightning events. If the output voltage exceeds the OVP trip level less than 7 successive cycles, the internal counter will be cleared and no fault is asserted.

QR Output Short Circuit Protection (PRT pin)

An output short circuit protection is implemented by sensing the auxiliary winding voltage at PRT pin during the flyback phase. The QR output short detection start working after delay 12mS when QR controller starts working. The QR output short protection works by sampling the plateau voltage at PRT pin during the flyback phase. If the sampled plateau voltage less than 0.75V ,the CS voltage is high than 0.45V, and FB is open , the controller assumes a true output short occurrence after successive 7 cycles and it enters restart mode and stops all switching operations. The special output short protection can minimize output short power consumption.

QR Over Load Operation (OLP)

When over load (for example, short circuit or open loop) in the QR stage occurs, the feedback current for QR FB pin is below minimum value and a fault is detected. If this fault is present for more than the T_{D_PL} time, the controller enters an auto-recovery soft burst mode. All pulses for PFC and QR are stopped, the controller will try to restart with the power on soft start after 1.4s. The SMPS enters the burst sequence and it resumes operation once the fault disappears. TD_PL time is set by external resistance of TIMER pin. When TIMER pin is externally connected to ground with 51K resistance, the typical value of TD_PL time is 60ms. This time is positively proportional to the Rtimer resistance. On the system board, the timer pin cannot be floated or shorted to the ground. It needs to be set with a proper value.

QR Gate Driver (QRGATE Pin)

The QRGATE pin is connected to the gate of an external QR power switch with 1A capability. An internal 11.7V clamp is added for MOSFET gate protection at high VCC voltage. When VCC voltage drops below UVLO(ON), the QRDRIVER pin is internally pull low to maintain the off state.

PFC Shut Down

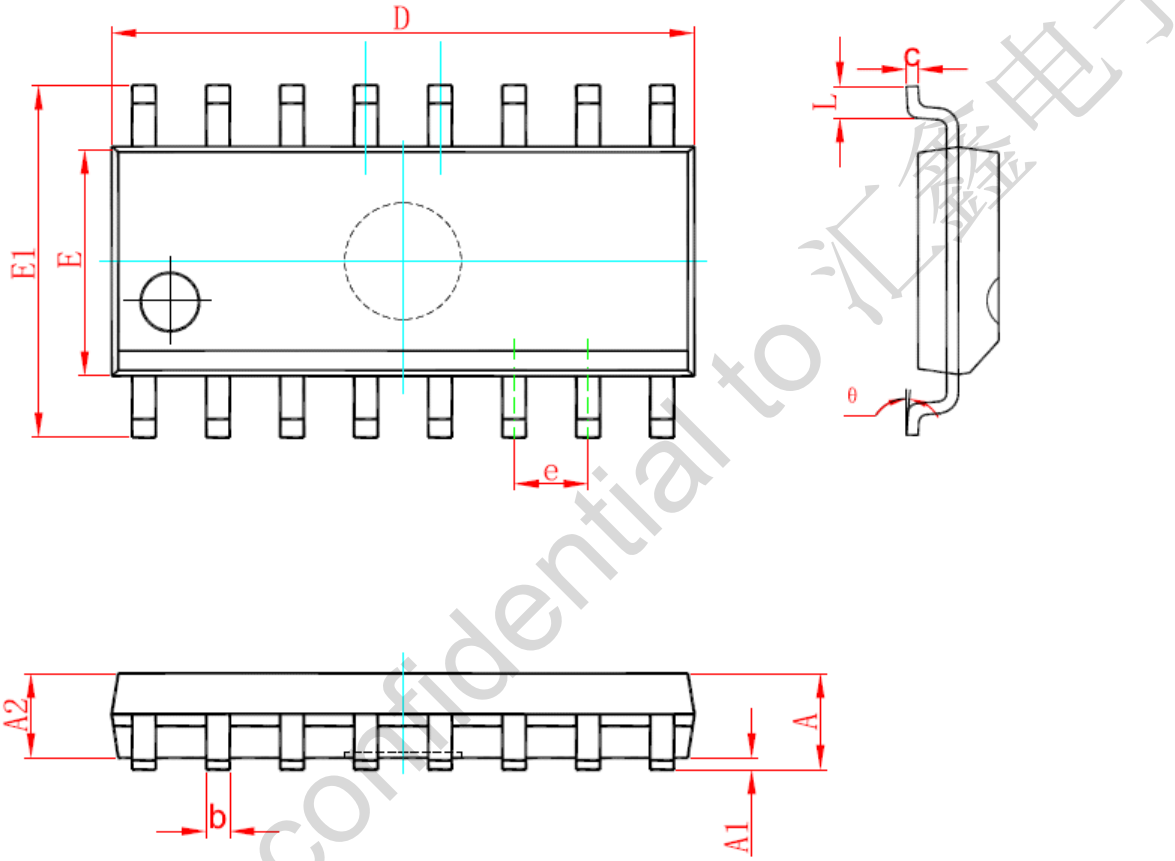
With the decrease of load ,OB6683 can realize PFC shut down function by connecting a resistance Rpfc to the ground from the PFCONOFF pin in order to improve efficiency. The output current of critical shutdown PFC can be evaluated by the following formula:

$I_{o_{shut}}(\mathrm{A}) = 4.5 \times 10^{-3} \times \frac{R_{pfc}(k\Omega)}{R_{cs}(\Omega)} \times \frac{N_p}{N_s}$ The PFC shutdown debounce time Tpfc_off is set by external resistance of TIMER pin. When TIMER pin is externally connected to ground with 51K resistance, the typical value of Tpfc_off is 1s. This time is positively proportional to the Rtimer resistance.

PACKAGE MECHANICAL DATA

16-Pin Plastic SOP (SOP16)

SOP16 PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.100	0.250	0.004	0.010
D	9.800	10.400	0.386	0.409
E	3.800	4.040	0.150	0.159
E1	5.800	6.240	0.228	0.246
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

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