NTMFS5832NL

MOSFET – Power
40 V, 111 A, 4.2 mΩ

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	20	A
		T_A = 70°C		16	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	3.1	W
		T_A = 70°C		1.9	
Continuous Drain Current $R_{\theta JC}$ (Note 1)		T_C = 25°C	I_D	111	A
		T_C = 70°C		89	
Power Dissipation $R_{\theta JC}$ (Note 1)		T_C = 25°C	P_D	96	W
		T_C = 70°C		61	
Pulsed Drain Current	t_p = 10 μs		I_{DM}	443	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +150	°C
Source Current (Body Diode)			I_S	111	A
Single Pulse Drain−to−Source Avalanche Energy (L = 0.1 mH)			EAS	134	mJ
			IAS	52	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS

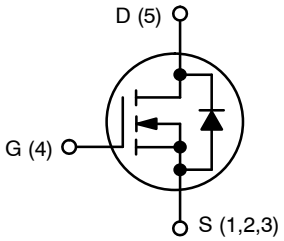
Parameter	Symbol	Value	Unit
Junction−to−Case (Drain) (Note 1)	$R_{\theta JC}$	1.3	°C/W
Junction−to−Ambient Steady State (Note 1)	$R_{\theta JA}$	40	
Junction−to−Ambient Steady State (Note 2)	$R_{\theta JA}$	75	

1. Surface−mounted on FR4 board using 1 sq−in pad (Cu area = 1.127 in sq [2 oz] inclusing traces).
2. Surface−mounted on FR4 board using 0.155 in sq (100mm^2) pad size.

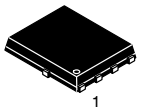
ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	4.2 mΩ @ 10 V	111 A
	6.5 mΩ @ 4.5 V	

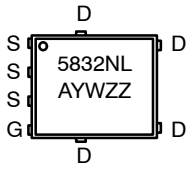


N−CHANNEL MOSFET



DFN5
(SO−8FL)
CASE 488AA
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

Device	Package	Shipping†
NTMFS5832NLT1G	DFN5 (Pb−Free)	1500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2012

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				34.2		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25 °C			1	μA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.0		3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				6.4		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 20 A		3.1	4.2	mΩ
		V_{GS} = 4.5 V	I_D = 20 A		5.0	6.5	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 20 A			21		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 25 V			2700		pF
Output Capacitance	C_{OSS}				360		
Reverse Transfer Capacitance	C_{RSS}				250		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 20 A			25		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 20 A			51		
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 20 A			2.0		
Gate−to−Source Charge	Q_{GS}				8.0		
Gate−to−Drain Charge	Q_{GD}				12.7		
Plateau Voltage	V_{GP}				3.2		V
Gate Resistance	R_G				1.2		Ω
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 20 V, I_D = 10 A, R_G = 1.0 Ω			13		ns
Rise Time	t_r				24		
Turn−Off Delay Time	$t_{d(OFF)}$				27		
Fall Time	t_f				8.0		
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 20 V, I_D = 10 A, R_G = 1.0 Ω			10		ns
Rise Time	t_r				18		
Turn−Off Delay Time	$t_{d(OFF)}$				32		
Fall Time	t_f				5.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 5 A	T_J = 25°C		0.73	1.2	V
			T_J = 125°C		0.57		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 10 A			28.6		ns
Charge Time	t_a				14		
Discharge Time	t_b				14.5		
Reverse Recovery Charge	Q_{RR}				23.4		nC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

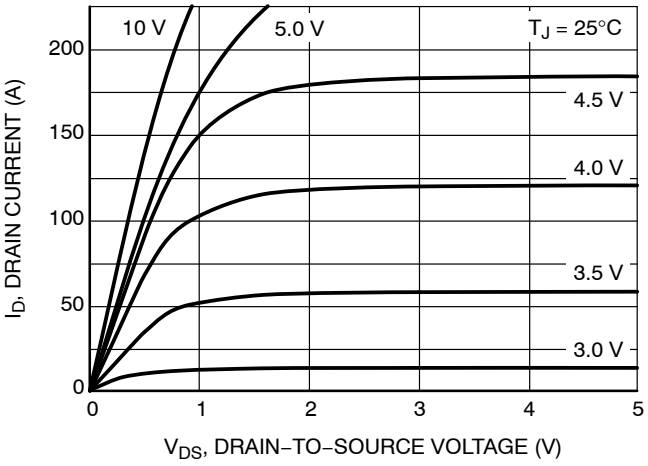


Figure 1. On−Region Characteristics

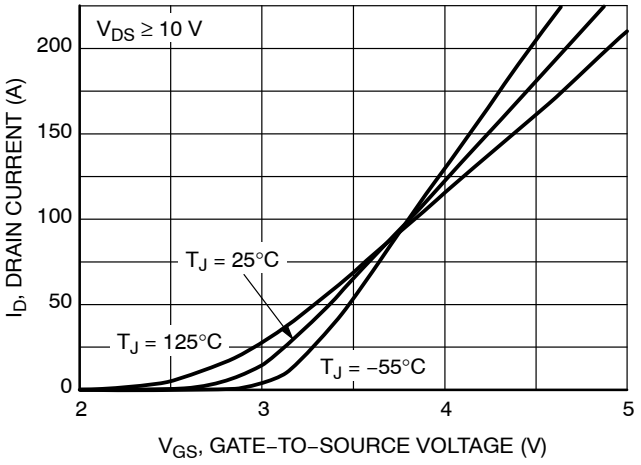


Figure 2. Transfer Characteristics

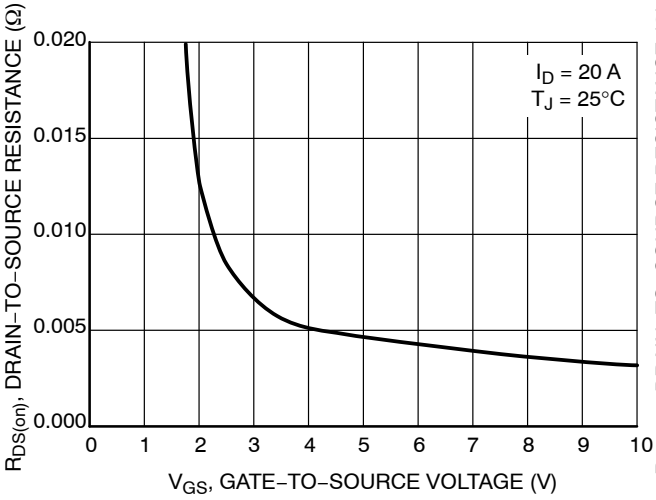


Figure 3. On−Resistance vs. Gate−to−Source Voltage

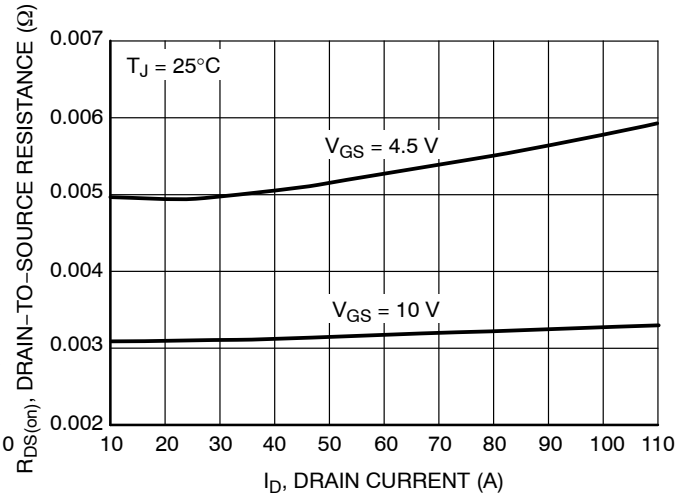


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

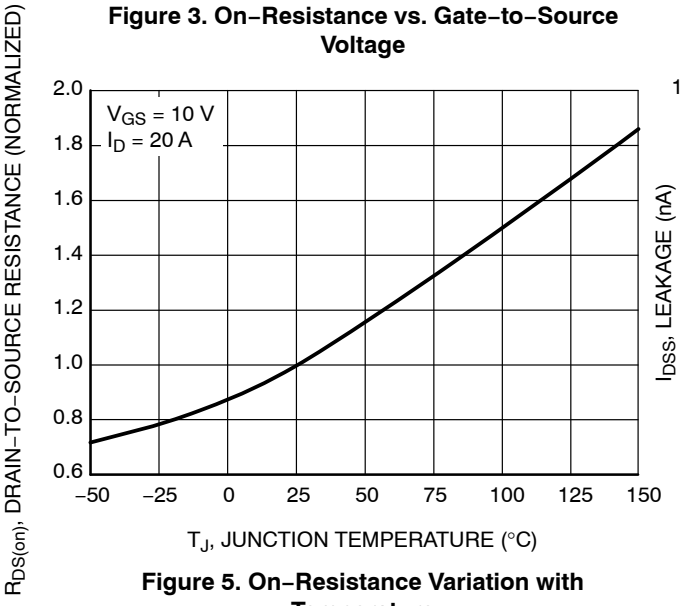


Figure 5. On−Resistance Variation with Temperature

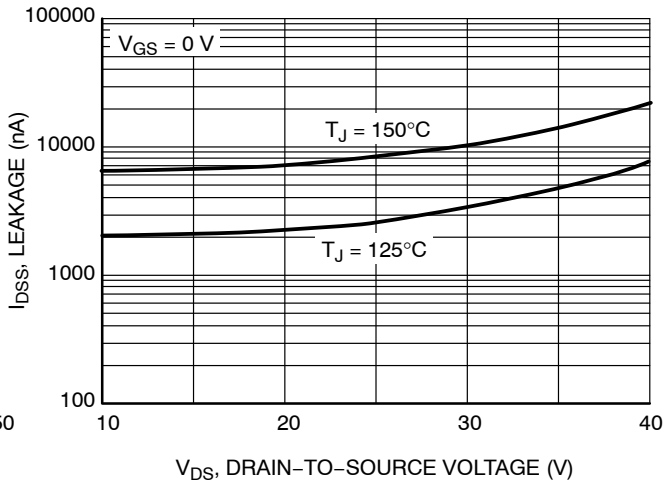


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

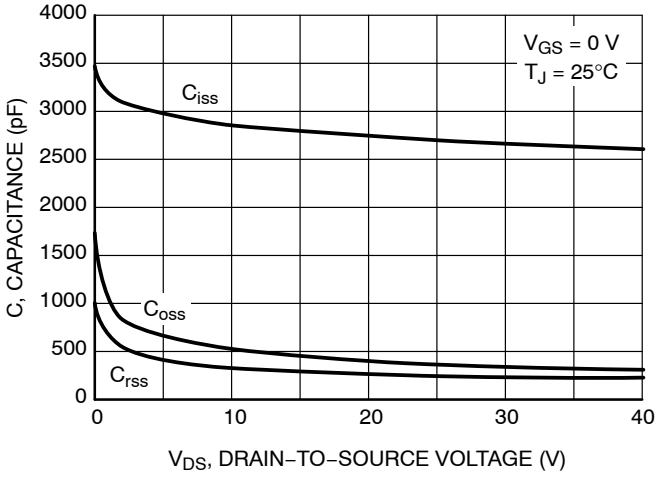


Figure 7. Capacitance Variation

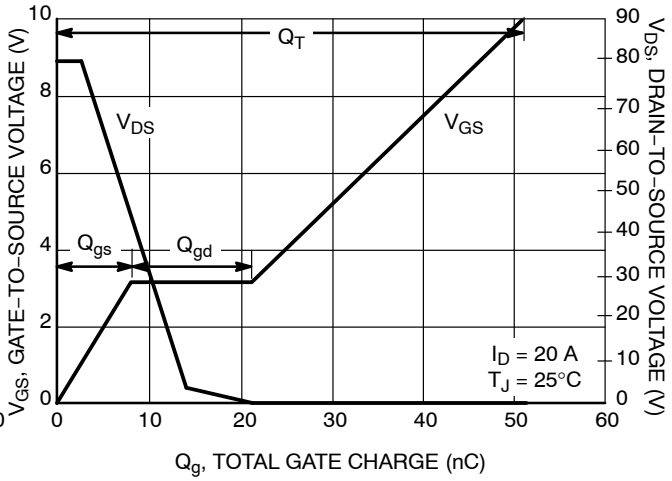


Figure 8. Gate−to−Source Voltage vs. Total Charge

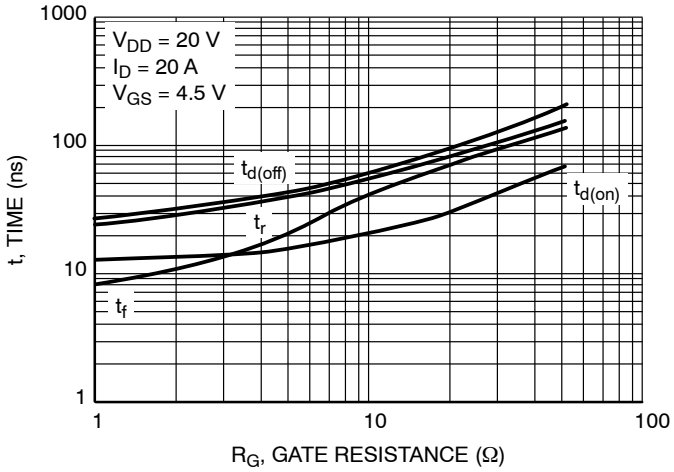


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

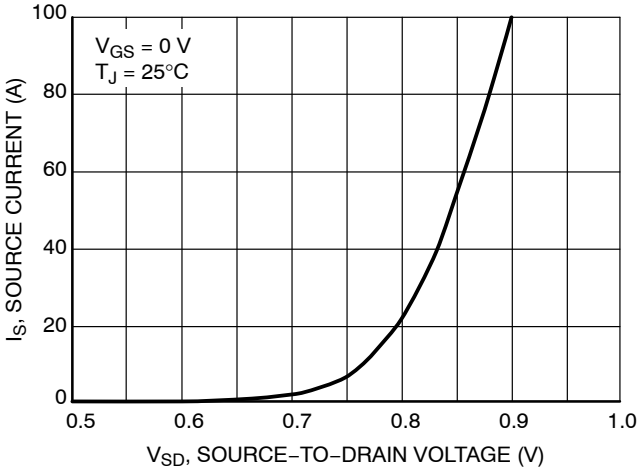


Figure 10. Diode Forward Voltage vs. Current

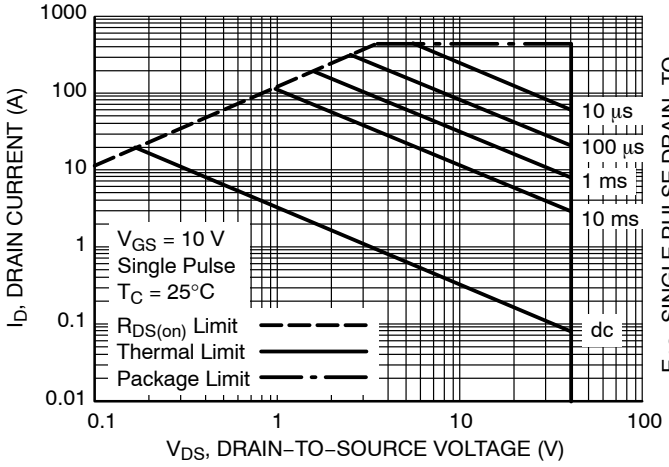


Figure 11. Maximum Rated Forward Biased Safe Operating Area

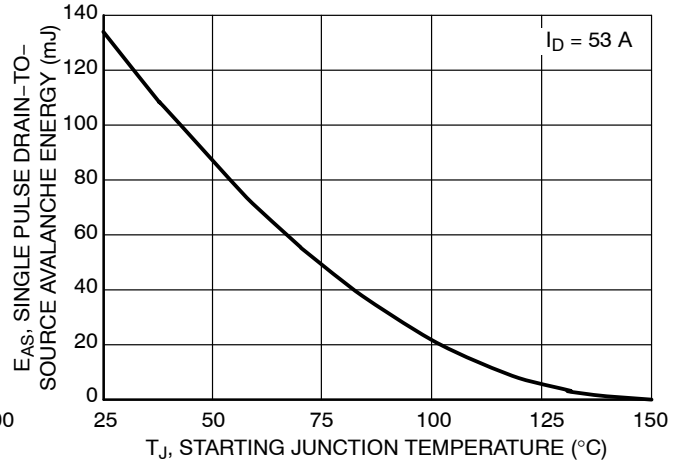


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL CHARACTERISTICS

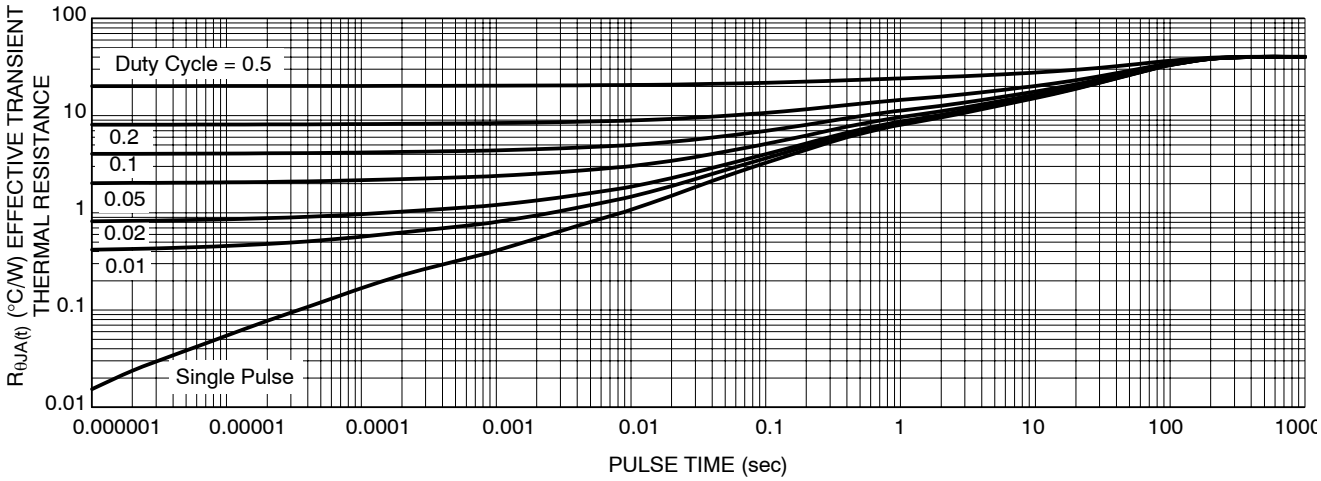
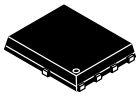


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

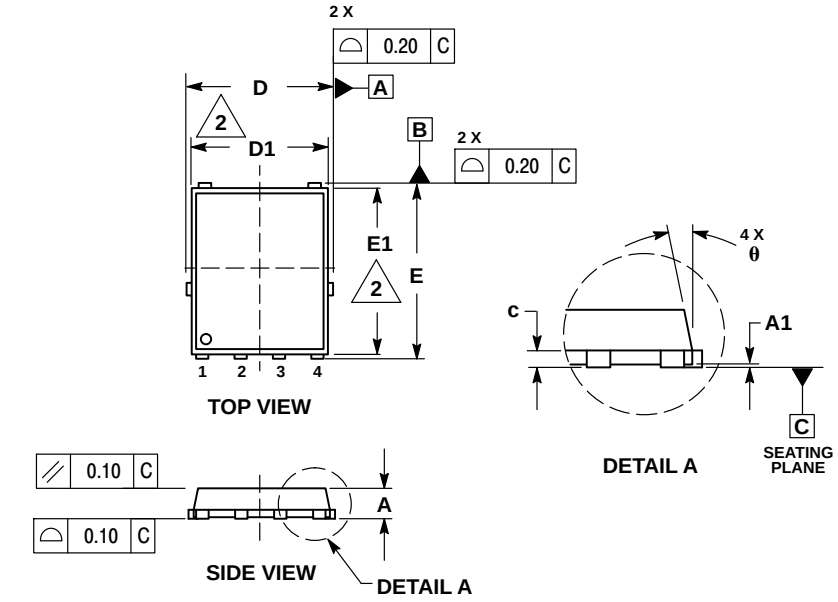
ON Semiconductor®



SCALE 2:1

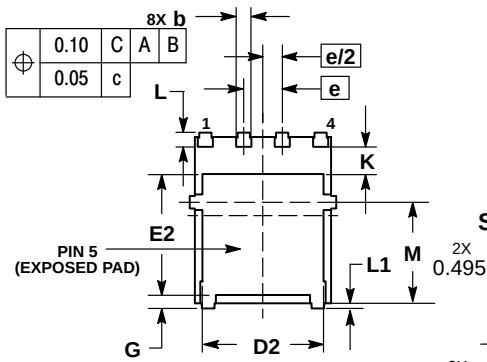
DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

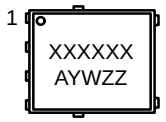


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	–––	12 °



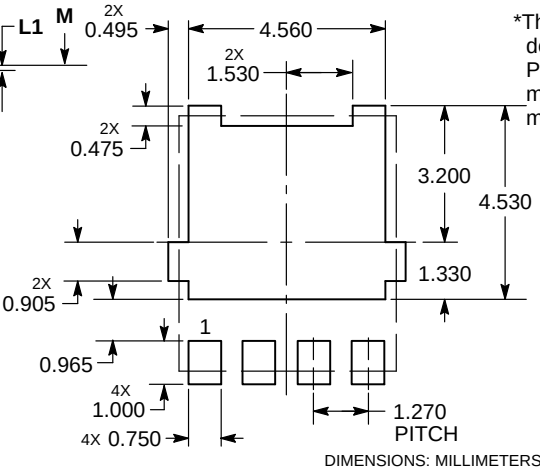
GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98AON14036D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DFN5 5x6, 1.27P (SO−8FL)**	**PAGE 1 OF 1**

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2018

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT
North American Technical Support:
Voice Mail: 1 800−282−9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:
Phone: 00421 33 790 2910
For additional information, please contact your local Sales Representative

◊