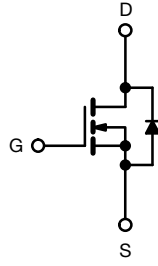
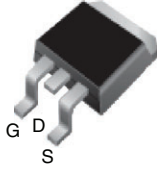


Power MOSFET

D²PAK (TO-263)


N-Channel MOSFET

| PRODUCT SUMMARY | |
|---------------------------|-----------------------------|
| V_{DS} (V) | 100 |
| $R_{DS(on)}$ (Ω) | $V_{GS} = 10\text{ V}$ 0.54 |
| Q_g max. (nC) | 8.3 |
| Q_{gs} (nC) | 2.3 |
| Q_{gd} (nC) | 3.8 |
| Configuration | Single |

FEATURES

- Surface-mount
- Available in tape and reel
- Dynamic dv/dt rating
- Repetitive avalanche rated
- 175 °C operating temperature
- Fast switching
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK (TO-263) is a surface-mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK (TO-263) is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application.

| ORDERING INFORMATION | | | |
|---------------------------------|-----------------------------|------------------------------|------------------------------|
| Package | D ² PAK (TO-263) | D ² PAK (TO-263) | D ² PAK (TO-263) |
| Lead (Pb)-free and halogen-free | SiHF510S-GE3 | SiHF510STRL-GE3 ^a | SiHF510STRR-GE3 ^a |
| Lead (Pb)-free | IRF510SPbF | IRF510STRLPbF ^a | IRF510STRRPbF ^a |

Note

a. See device orientation

| ABSOLUTE MAXIMUM RATINGS ($T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | |
|---|------------------|-----------------------------------|------|
| PARAMETER | SYMBOL | LIMIT | UNIT |
| Drain-source voltage | V_{DS} | 100 | V |
| Gate-source voltage | V_{GS} | ± 20 | |
| Continuous drain current | V_{GS} at 10 V | $T_C = 25\text{ }^\circ\text{C}$ | A |
| | | $T_C = 100\text{ }^\circ\text{C}$ | |
| Pulsed drain current ^a | I_{DM} | 20 | W/°C |
| Linear derating factor | | 0.29 | |
| Linear derating factor (PCB mount) ^e | | 0.025 | |
| Single pulse avalanche energy ^b | E_{AS} | 75 | mJ |
| Avalanche current ^a | I_{AR} | 5.6 | A |
| Repetitive avalanche energy ^a | E_{AR} | 4.3 | mJ |
| Maximum power dissipation | P_D | $T_C = 25\text{ }^\circ\text{C}$ | W |
| | | $T_A = 25\text{ }^\circ\text{C}$ | |
| Maximum power dissipation (PCB mount) ^e | | 3.7 | |
| Peak diode recovery dv/dt ^c | dv/dt | 5.5 | V/ns |
| Operating junction and storage temperature range | T_J, T_{stg} | -55 to +175 | °C |
| Soldering recommendations (peak temperature) ^d | For 10 s | 300 | |

Notes

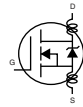
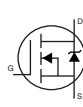
- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- $V_{DD} = 25\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 4.8\text{ mH}$, $R_\theta = 25\text{ }^\circ\text{C/W}$, $I_{AS} = 5.6\text{ A}$ (see fig. 12)
- $I_{SD} \leq 5.6\text{ A}$, $di/dt \leq 75\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^\circ\text{C}$
- 1.6 mm from case
- When mounted on 1" square PCB (FR-4 or G-10 material)



| THERMAL RESISTANCE RATINGS | | | | |
|--|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum junction-to-ambient | R_{thJA} | - | 62 | °C/W |
| Maximum junction-to-ambient (PCB mount) ^a | R_{thJA} | - | 40 | |
| Maximum junction-to-case (drain) | R_{thJC} | - | 3.5 | |

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

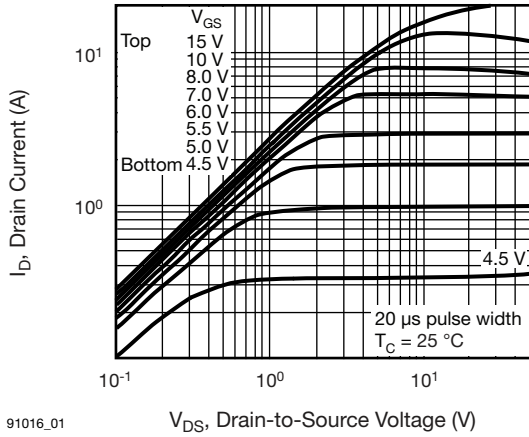
| SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted) | | | | | | | |
|---|---------------------|---|--|------|------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-source breakdown voltage | V_{DS} | $V_{GS} = 0, I_D = 250\ \mu\text{A}$ | | 100 | - | - | V |
| V_{DS} temperature coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\ \text{mA}$ | | - | 0.12 | - | V/°C |
| Gate-source threshold voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ | | 2.0 | - | 4.0 | V |
| Gate-source leakage | I_{GSS} | $V_{GS} = \pm 20\ \text{V}$ | | - | - | ± 100 | nA |
| Zero gate voltage drain current | I_{DSS} | $V_{DS} = 100\ \text{V}, V_{GS} = 0\ \text{V}$ | | - | - | 25 | μA |
| | | $V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 150\text{ }^\circ\text{C}$ | | - | - | 250 | |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS} = 10\ \text{V}$ | $I_D = 3.4\ \text{A}^b$ | - | - | 0.54 | Ω |
| Forward transconductance | g_{fs} | $V_{DS} = 50\ \text{V}, I_D = 3.4\ \text{A}^b$ | | 1.3 | - | - | S |
| Dynamic | | | | | | | |
| Input capacitance | C_{iss} | $V_{GS} = 0\ \text{V}, V_{DS} = 25\ \text{V}, f = 1.0\ \text{MHz}$, see fig. 5 | | - | 180 | - | μF |
| Output capacitance | C_{oss} | | | - | 81 | - | |
| Reverse transfer capacitance | C_{rss} | | | - | 15 | - | |
| Total gate charge | Q_g | $V_{GS} = 10\ \text{V}$ | $I_D = 5.6\ \text{A}, V_{DS} = 80\ \text{V}$, see fig. 6 and fig. 13 ^b | - | - | 8.3 | nC |
| Gate-source charge | Q_{gs} | | | - | - | 2.3 | |
| Gate-drain charge | Q_{gd} | | | - | - | 3.8 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD} = 50\ \text{V}, I_D = 5.6\ \text{A}, R_g = 24\ \Omega, R_D = 8.4\ \Omega$, see fig. 10 ^b | | - | 6.9 | - | ns |
| Rise time | t_r | | | - | 16 | - | |
| Turn-off delay time | $t_{d(off)}$ | | | - | 15 | - | |
| Fall time | t_f | | | - | 9.4 | - | |
| Gate input resistance | R_g | $f = 1\ \text{MHz}$, open drain | | 2.5 | - | 11.6 | Ω |
| Internal drain inductance | L_D | Between lead, 6 mm (0.25") from package and center of die contact  | | - | 4.5 | - | nH |
| Internal source inductance | L_S | | | - | 7.5 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous source-drain diode current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | | - | - | 5.6 | A |
| Pulsed diode forward current ^a | I_{SM} | | | - | - | 20 | |
| Body diode voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 5.6\ \text{A}, V_{GS} = 0\ \text{V}^b$ | | - | - | 2.5 | V |
| Body diode reverse recovery time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = 5.6\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}^b$ | | - | 100 | 200 | ns |
| Body diode reverse recovery charge | Q_{rr} | | | - | 0.44 | 0.88 | μC |
| Forward turn-on time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width $\leq 300\ \mu\text{s}$; duty cycle $\leq 2\ \%$

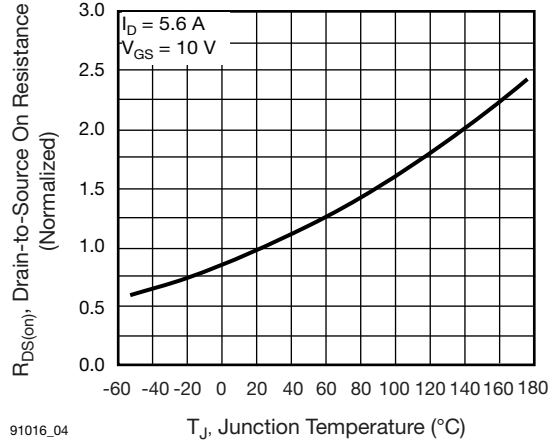


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



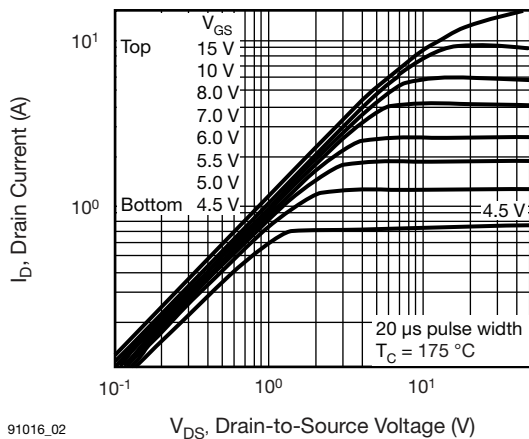
91016_01

Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$



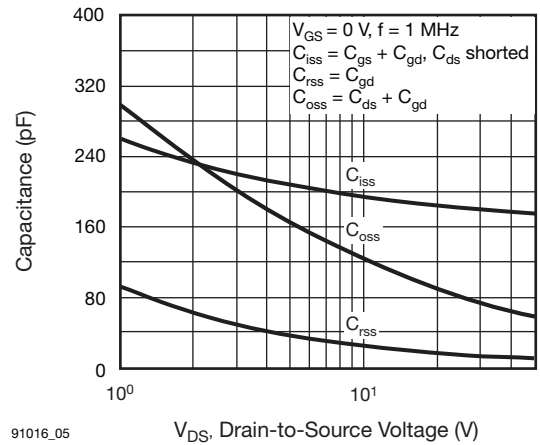
91016_04

Fig. 4 - Normalized On-Resistance vs. Temperature



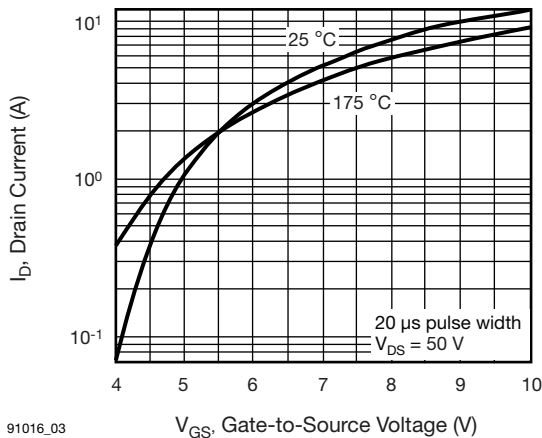
91016_02

Fig. 2 - Typical Output Characteristics, $T_C = 175\text{ }^\circ\text{C}$



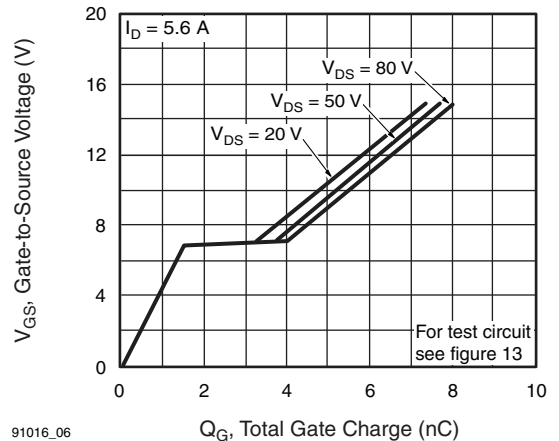
91016_05

Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



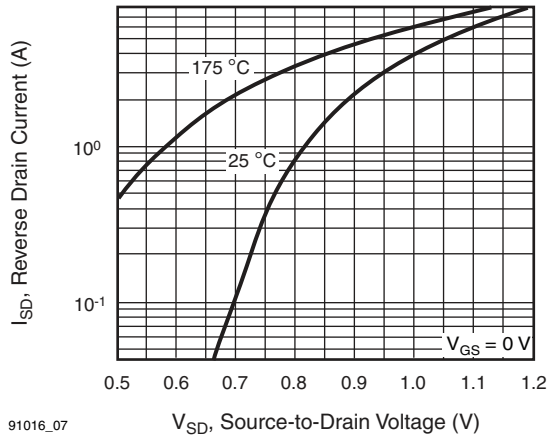
91016_03

Fig. 3 - Typical Transfer Characteristics



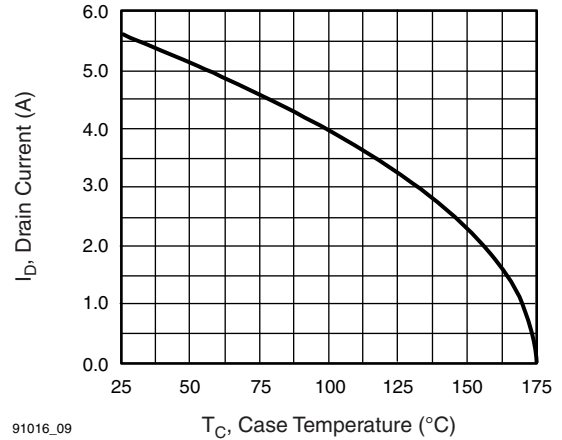
91016_06

Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



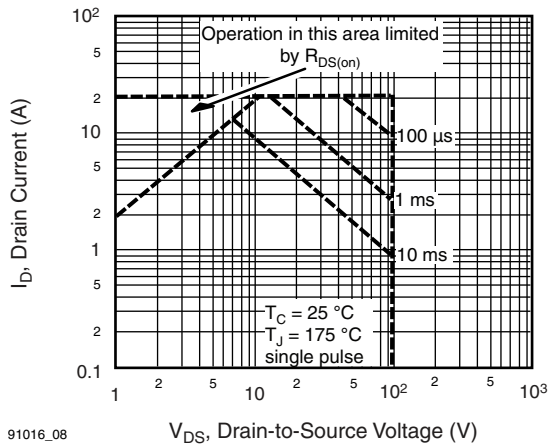
91016_07

Fig. 7 - Typical Source-Drain Diode Forward Voltage



91016_09

Fig. 9 - Maximum Drain Current vs. Case Temperature



91016_08

Fig. 8 - Maximum Safe Operating Area

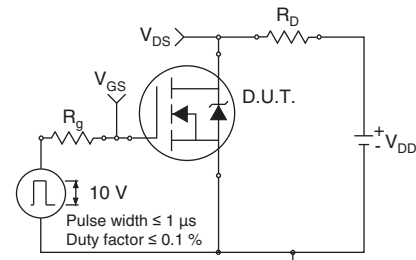


Fig. 10a - Switching Time Test Circuit

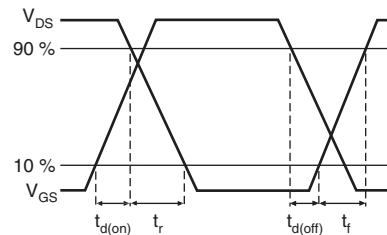
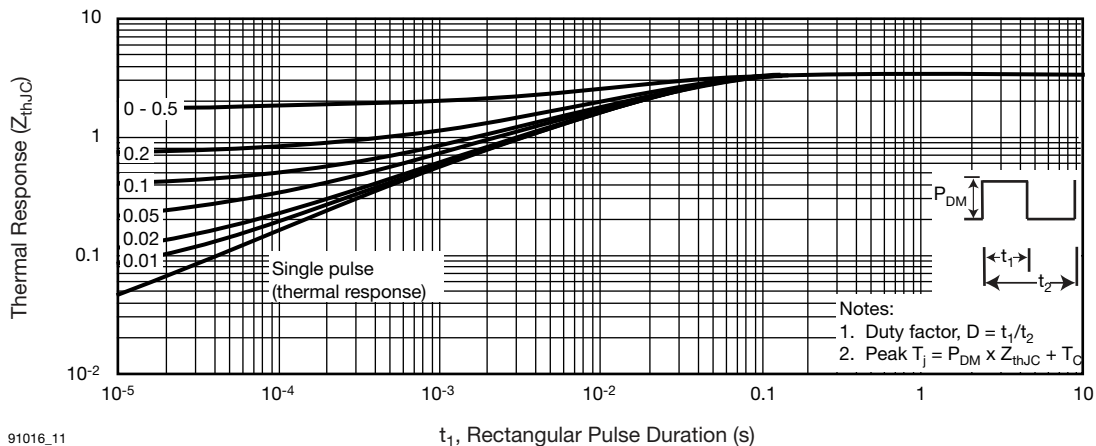


Fig. 10b - Switching Time Waveforms



91016_11

Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

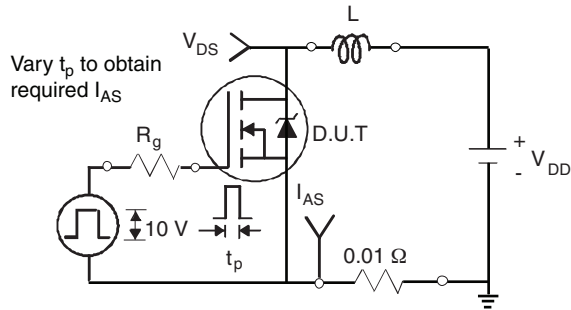


Fig. 12a - Unclamped Inductive Test Circuit

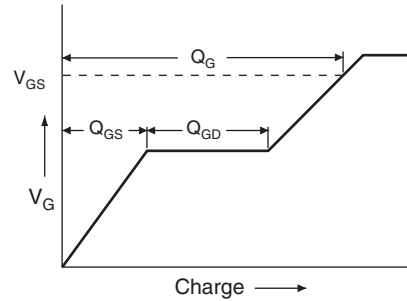


Fig. 13a - Basic Gate Charge Waveform

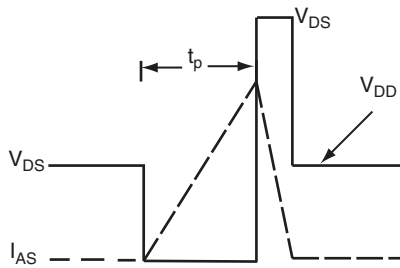


Fig. 12b - Unclamped Inductive Waveforms

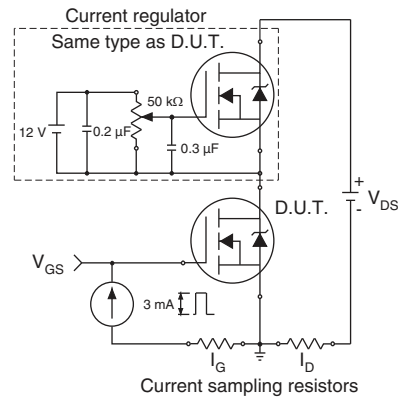


Fig. 13b - Gate Charge Test Circuit

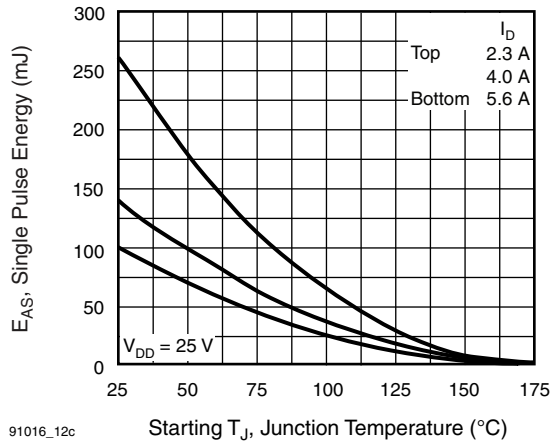
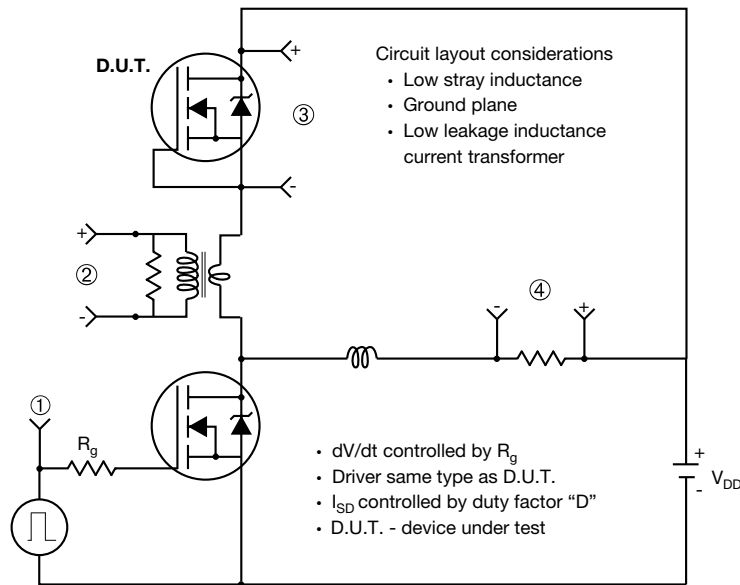


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

Peak Diode Recovery dV/dt Test Circuit



Note
 a. $V_{GS} = 5\text{ V}$ for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91016.

TO-263AB (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|------|--------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.06 | 4.83 | 0.160 | 0.190 |
| A1 | 0.00 | 0.25 | 0.000 | 0.010 |
| b | 0.51 | 0.99 | 0.020 | 0.039 |
| b1 | 0.51 | 0.89 | 0.020 | 0.035 |
| b2 | 1.14 | 1.78 | 0.045 | 0.070 |
| b3 | 1.14 | 1.73 | 0.045 | 0.068 |
| c | 0.38 | 0.74 | 0.015 | 0.029 |
| c1 | 0.38 | 0.58 | 0.015 | 0.023 |
| c2 | 1.14 | 1.65 | 0.045 | 0.065 |
| D | 8.38 | 9.65 | 0.330 | 0.380 |

| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|-------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| D1 | 6.86 | - | 0.270 | - |
| E | 9.65 | 10.67 | 0.380 | 0.420 |
| E1 | 6.22 | - | 0.245 | - |
| e | 2.54 BSC | | 0.100 BSC | |
| H | 14.61 | 15.88 | 0.575 | 0.625 |
| L | 1.78 | 2.79 | 0.070 | 0.110 |
| L1 | - | 1.65 | - | 0.066 |
| L2 | - | 1.78 | - | 0.070 |
| L3 | 0.25 BSC | | 0.010 BSC | |
| L4 | 4.78 | 5.28 | 0.188 | 0.208 |

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Hyperlinks included in this datasheet may direct users to third-party websites. These links are provided as a convenience and for informational purposes only. Inclusion of these hyperlinks does not constitute an endorsement or an approval by Vishay of any of the products, services or opinions of the corporation, organization or individual associated with the third-party website. Vishay disclaims any and all liability and bears no responsibility for the accuracy, legality or content of the third-party website or for that of subsequent links.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.