

NSS20300MR6T1G

20 V, 5 A, Low $V_{CE(sat)}$ PNP Transistor

ON Semiconductor's e²PowerEdge family of low $V_{CE(sat)}$ transistors are miniature surface mount devices featuring ultra low saturation voltage ($V_{CE(sat)}$) and high current gain capability. These are designed for use in low voltage, high speed switching applications where affordable efficient energy control is important.

Typical application are DC-DC converters and power management in portable and battery powered products such as cellular and cordless phones, PDAs, computers, printers, digital cameras and MP3 players. Other applications are low voltage motor controls in mass storage products such as disc drives and tape drives. In the automotive industry they can be used in air bag deployment and in the instrument cluster. The high current gain allows e²PowerEdge devices to be driven directly from PMU's control outputs, and the Linear Gain (Beta) makes them ideal components in analog amplifiers.

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$)

Rating	Symbol	Max	Unit
Collector-Emitter Voltage	V_{CEO}	-20	Vdc
Collector-Base Voltage	V_{CBO}	-30	Vdc
Emitter-Base Voltage	V_{EBO}	-6.0	Vdc
Collector Current - Continuous	I_C	-3.0	Adc
Collector Current - Peak	I_{CM}	-5.0	A
Electrostatic Discharge	ESD	HBM Class 3B MM Class C	

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation, $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D (Note 1)	545 4.3	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 1)	230	$^\circ\text{C}/\text{W}$
Total Device Dissipation $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D (Note 2)	1.06 8.5	W mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$ (Note 2)	118	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Lead #1	$R_{\theta JL}$ (Note 1) $R_{\theta JL}$ (Note 2)	48 40	$^\circ\text{C}/\text{W}$ $^\circ\text{C}/\text{W}$
Total Device Dissipation (Single Pulse < 10 sec.)	$P_{D\text{single}}$ (Note 2)	1.75	W
Junction and Storage Temperature Range	T_J, T_{stg}	-55 to +150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

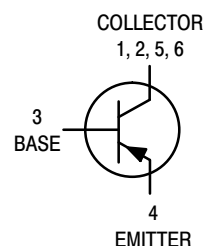
- FR-4 @ 100 mm², 2 oz copper traces.
- FR-4 @ 500 mm², 2 oz copper traces.



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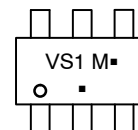
<http://onsemi.com>

**20 VOLTS
5.0 AMPS
PNP LOW $V_{CE(sat)}$ TRANSISTOR
EQUIVALENT $R_{DS(on)}$ 78 m Ω**



TSOP-6
CASE 318G
STYLE 6

DEVICE MARKING



VS1 = Specific Device Code
M = Date Code
■ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
NSS20300MR6T1G	TSOP-6 (Pb-Free)	3000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NSS20300MR6T1G

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typical	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I _C = –10 mAdc, I _B = 0)	V _{(BR)CEO}	–20		–	Vdc
Collector–Base Breakdown Voltage (I _C = –0.1 mAdc, I _E = 0)	V _{(BR)CBO}	–30		–	Vdc
Emitter–Base Breakdown Voltage (I _E = –0.1 mAdc, I _C = 0)	V _{(BR)EBO}	–6.0		–	Vdc
Collector Cutoff Current (V _{CB} = –20 Vdc, I _E = 0)	I _{CBO}	–		–0.1	μAdc
Collector–Emitter Cutoff Current (V _{CES} = –20 Vdc)	I _{CES}	–		–0.1	μAdc
Emitter Cutoff Current (V _{EB} = –6.0 Vdc)	I _{EBO}	–		–0.1	μAdc
ON CHARACTERISTICS					
DC Current Gain ⁽¹⁾ (I _C = –1.0 A, V _{CE} = –1.5 V) (I _C = –1.5 A, V _{CE} = –2.0 V) (I _C = –2.0 A, V _{CE} = –2.0 V)	h _{FE}	100 100 100	230	– 400 –	
Collector–Emitter Saturation Voltage (Note 3) (I _C = –0.10 A, I _B = –0.010 A) (I _C = –1.0 A, I _B = –0.010 A) (I _C = –2.0 A, I _B = –0.02 A)	V _{CE(sat)}	– – –	–0.010 –0.127 –0.250	–0.015 –0.145 –0.320	V
Base–Emitter Saturation Voltage (Note 3) (I _C = –1A, I _B = –0.010 A)	V _{BE(sat)}	–	–	–0.85	V
Base–Emitter Turn–on Voltage (Note 3) (I _C = –2.0 A, V _{CE} = –3.0 V)	V _{BE(on)}	–	–	–0.875	V
Cutoff Frequency (I _C = –100 mA, V _{CE} = –5.0 V, f = 100 MHz)	f _T	100	–	–	MHz
Input Capacitance (V _{EB} = –0.5 V, f = 1.0 MHz)	C _{IBO}	–		650	pF
Output Capacitance (V _{CB} = –3.0 V, f = 1.0 MHz)	C _{OBO}	–		100	pF

3. Pulsed Condition: Pulse Width ≤ 300 μsec, Duty Cycle ≤ 2%.

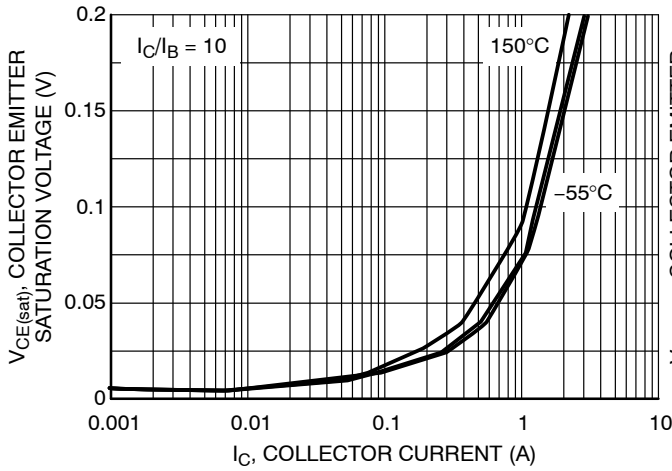


Figure 1. Collector Emitter Saturation Voltage versus Collector Current

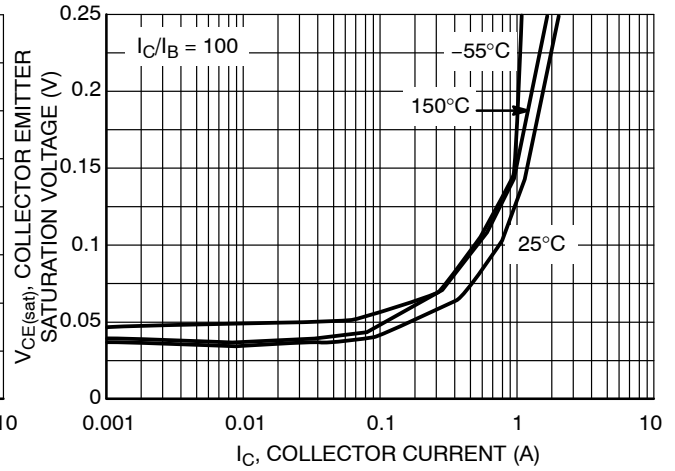


Figure 2. Collector Emitter Saturation Voltage versus Collector Current

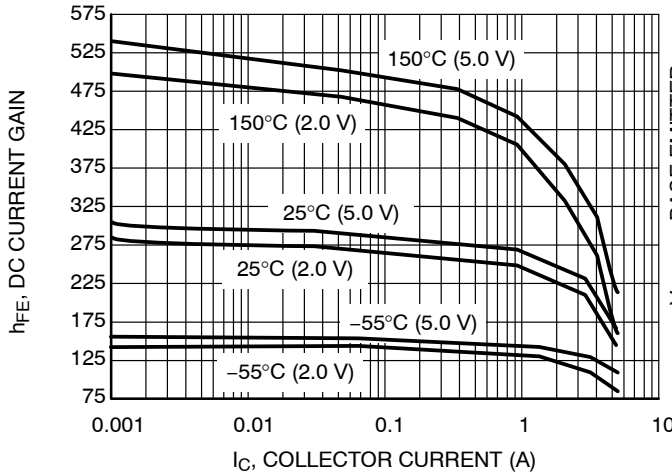


Figure 3. DC Current Gain versus Collector Current

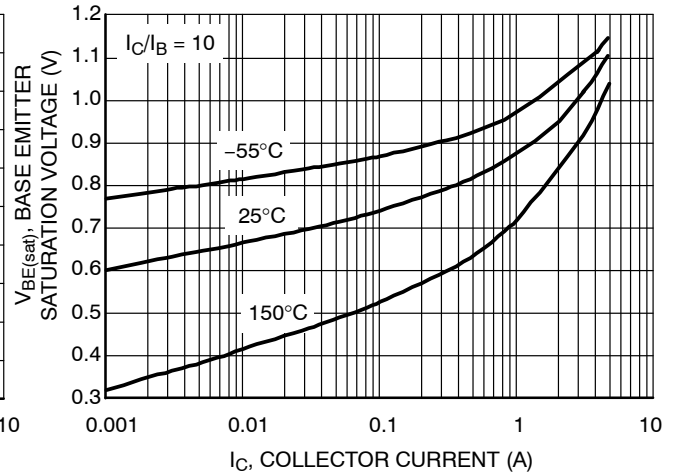


Figure 4. Base Emitter Saturation Voltage versus Collector Current

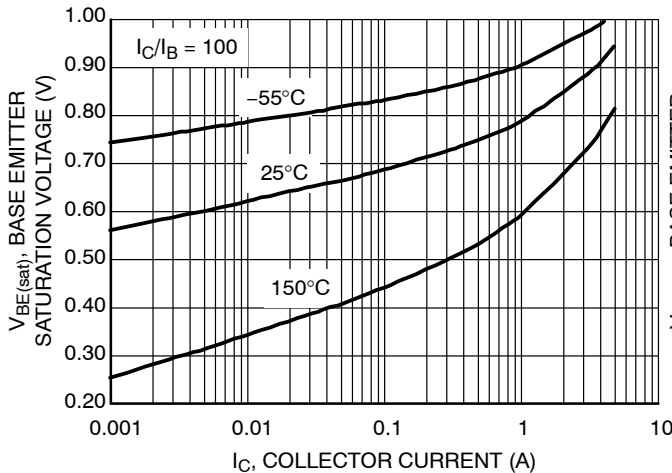


Figure 5. Base Emitter Saturation Voltage versus Collector Current

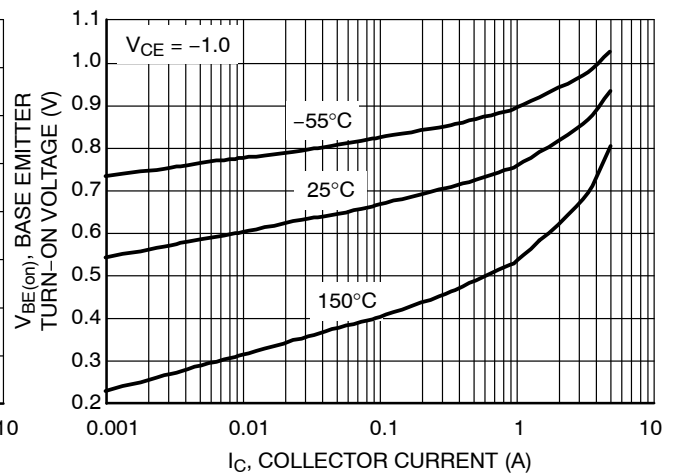


Figure 6. Base Emitter Turn-On Voltage versus Collector Current

NSS20300MR6T1G

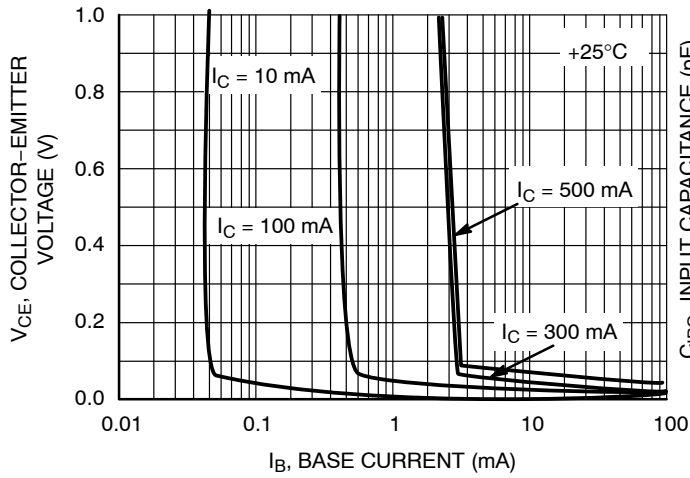


Figure 7. Saturation Region

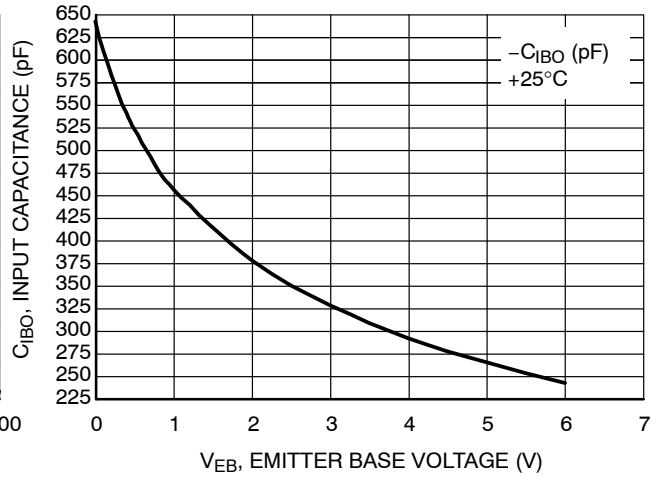


Figure 8. NSS20300MR6T1G Input Capacitance

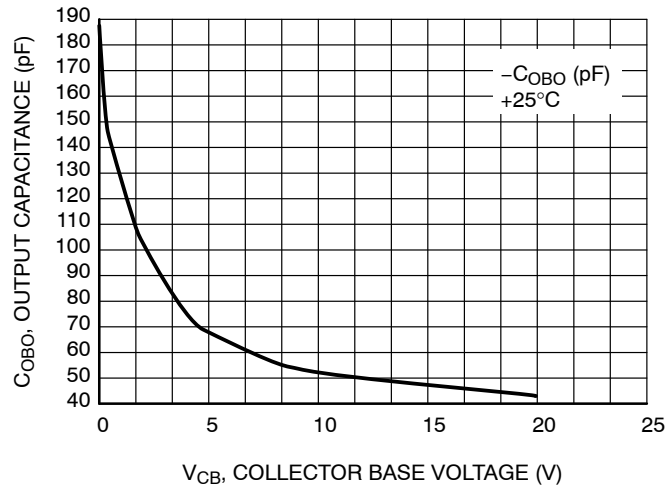


Figure 9. NSS20300MR6T1G Output Capacitance

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



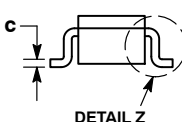
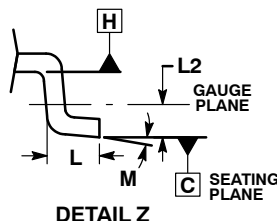
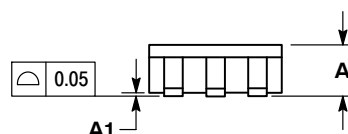
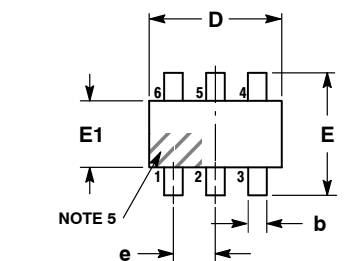
SCALE 2:1

TSOP-6

CASE 318G-02

ISSUE V

DATE 12 JUN 2012



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	—	10°

STYLE 1:

- PIN 1. DRAIN
- PIN 2. DRAIN
- PIN 3. GATE
- PIN 4. SOURCE
- PIN 5. DRAIN
- PIN 6. DRAIN

STYLE 2:

- PIN 1. EMITTER 2
- PIN 2. BASE 1
- PIN 3. COLLECTOR 1
- PIN 4. EMITTER 1
- PIN 5. BASE 2
- PIN 6. COLLECTOR 2

STYLE 3:

- PIN 1. ENABLE
- PIN 2. N/C
- PIN 3. R BOOST
- PIN 4. Vz
- PIN 5. V in
- PIN 6. V out

STYLE 4:

- PIN 1. N/C
- PIN 2. V in
- PIN 3. NOT USED
- PIN 4. GROUND
- PIN 5. ENABLE
- PIN 6. LOAD

STYLE 5:

- PIN 1. EMITTER 2
- PIN 2. BASE 2
- PIN 3. COLLECTOR 1
- PIN 4. EMITTER 1
- PIN 5. BASE 1
- PIN 6. COLLECTOR 2

STYLE 6:

- PIN 1. COLLECTOR
- PIN 2. COLLECTOR
- PIN 3. BASE
- PIN 4. EMITTER
- PIN 5. COLLECTOR
- PIN 6. COLLECTOR

STYLE 7:

- PIN 1. COLLECTOR
- PIN 2. COLLECTOR
- PIN 3. BASE
- PIN 4. N/C
- PIN 5. COLLECTOR
- PIN 6. EMITTER

STYLE 8:

- PIN 1. Vbus
- PIN 2. D(in)
- PIN 3. D(in)+
- PIN 4. D(out)+
- PIN 5. D(out)
- PIN 6. GND

STYLE 9:

- PIN 1. LOW VOLTAGE GATE
- PIN 2. DRAIN
- PIN 3. SOURCE
- PIN 4. DRAIN
- PIN 5. DRAIN
- PIN 6. HIGH VOLTAGE GATE

STYLE 10:

- PIN 1. D(OUT)+
- PIN 2. GND
- PIN 3. D(OUT)-
- PIN 4. D(IN)-
- PIN 5. VBUS
- PIN 6. D(IN)+

STYLE 11:

- PIN 1. SOURCE 1
- PIN 2. DRAIN 2
- PIN 3. DRAIN 2
- PIN 4. SOURCE 2
- PIN 5. GATE 1
- PIN 6. DRAIN 1/GATE 2

STYLE 12:

- PIN 1. I/O
- PIN 2. GROUND
- PIN 3. I/O
- PIN 4. I/O
- PIN 5. VCC
- PIN 6. I/O

STYLE 13:

- PIN 1. GATE 1
- PIN 2. SOURCE 2
- PIN 3. GATE 2
- PIN 4. DRAIN 2
- PIN 5. SOURCE 1
- PIN 6. DRAIN 1

STYLE 14:

- PIN 1. ANODE
- PIN 2. SOURCE
- PIN 3. GATE
- PIN 4. CATHODE/DRAIN
- PIN 5. CATHODE/DRAIN
- PIN 6. CATHODE/DRAIN

STYLE 15:

- PIN 1. ANODE
- PIN 2. SOURCE
- PIN 3. GATE
- PIN 4. DRAIN
- PIN 5. N/C
- PIN 6. CATHODE

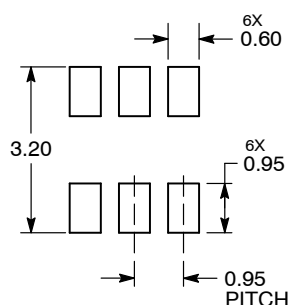
STYLE 16:

- PIN 1. ANODE/CATHODE
- PIN 2. BASE
- PIN 3. EMITTER
- PIN 4. COLLECTOR
- PIN 5. ANODE
- PIN 6. CATHODE

STYLE 17:

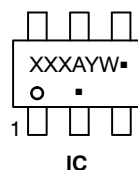
- PIN 1. EMITTER
- PIN 2. BASE
- PIN 3. ANODE/CATHODE
- PIN 4. ANODE
- PIN 5. CATHODE
- PIN 6. COLLECTOR

RECOMMENDED SOLDERING FOOTPRINT*

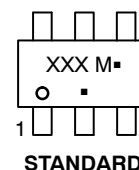


DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



IC



STANDARD

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb-Free Package

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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