

# NDF02N60Z, NDD02N60Z

## N-Channel Power MOSFET 600 V, 4.8 $\Omega$

### Features

- Low ON Resistance
- Low Gate Charge
- ESD Diode–Protected Gate
- 100% Avalanche Tested
- These Devices are Pb–Free, Halogen Free/BFR Free and are RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	NDF	NDD	Unit
Drain-to-Source Voltage	$V_{DS}$	600		V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$I_D$	2.4	2.2	A
Continuous Drain Current $R_{\theta JC}$ $T_A = 100^\circ\text{C}$ (Note 1)	$I_D$	1.6	1.4	A
Pulsed Drain Current, $V_{GS} @ 10\text{ V}$	$I_{DM}$	10	9	A
Power Dissipation $R_{\theta JC}$	$P_D$	24	57	W
Gate-to-Source Voltage	$V_{GS}$	$\pm 30$		V
Single Pulse Avalanche Energy, $I_D = 2.4\text{ A}$	$E_{AS}$	120		mJ
ESD (HBM) (JESD 22–A114)	$V_{ESD}$	2500		V
RMS Isolation Voltage ( $t = 0.3\text{ sec.}$ , R.H. $\leq 30\%$ , $T_A = 25^\circ\text{C}$ ) (Figure 17)	$V_{ISO}$	4500		V
Peak Diode Recovery (Note 2)	$dv/dt$	4.5		V/ns
Continuous Source Current (Body Diode)	$I_S$	2.4		A
Maximum Temperature for Soldering Leads	$T_L$	260		$^\circ\text{C}$
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	–55 to 150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

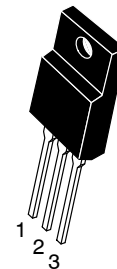
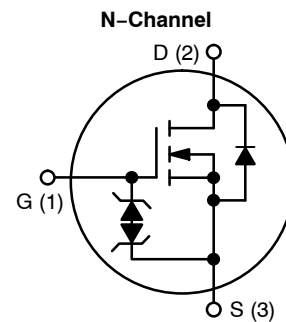
1. Limited by maximum junction temperature
2.  $I_{SD} = 2.4\text{ A}$ ,  $di/dt \leq 100\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ ,  $T_J = +150^\circ\text{C}$



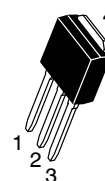
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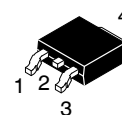
$V_{DSS}$	$R_{DS(on)} \text{ (MAX) @ } 1\text{ A}$
600 V	4.8 $\Omega$



NDF02N60ZG,  
NDF02N60ZH  
TO-220FP  
CASE 221AH



NDD02N60Z-1G  
IPAK  
CASE 369D



NDD02N60ZT4G  
DPAK  
CASE 369AA

### ORDERING AND MARKING INFORMATION

See detailed ordering, marking and shipping information on page 7 of this data sheet.

# NDF02N60Z, NDD02N60Z

## THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	4.9 2.2	°C/W
Junction-to-Ambient Steady State	$R_{\theta JA}$	51 41 80	

3. Insertion mounted

4. Surface mounted on FR4 board using 1" sq. pad size, (Cu area = 1.127 in sq [2 oz] including traces).

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	$BV_{DSS}$	600			V
Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D = 1\text{ mA}$	$\Delta BV_{DSS}/\Delta T_J$		0.6		V/°C
Drain-to-Source Leakage Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	$I_{DSS}$			1	μA
					50	
Gate-to-Source Forward Leakage	$V_{GS} = \pm 20\text{ V}$	$I_{GSS}$			±10	μA

### ON CHARACTERISTICS (Note 5)

Static Drain-to-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 1.0\text{ A}$	$R_{DS(on)}$		4.0	4.8	Ω
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 50\text{ μA}$	$V_{GS(th)}$	3.0	4.0	4.5	V
Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 1.2\text{ A}$	$g_{FS}$		1.7		S

### DYNAMIC CHARACTERISTICS

Input Capacitance (Note 6)	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	$C_{iss}$	215	274	325	pF
Output Capacitance (Note 6)		$C_{oss}$	25	34	45	
Reverse Transfer Capacitance (Note 6)		$C_{rss}$	4.0	7.0	10	
Total Gate Charge (Note 6)	$V_{DD} = 300\text{ V}, I_D = 2.4\text{ A},$ $V_{GS} = 10\text{ V}$	$Q_g$	5.0	10	16	nC
Gate-to-Source Charge (Note 6)		$Q_{gs}$	1.5	2.4	4.0	
Gate-to-Drain ("Miller") Charge (Note 6)		$Q_{gd}$	3.5	5.3	8.0	
Plateau Voltage		$V_{GP}$		6.4		V
Gate Resistance		$R_g$		4.9		Ω

### RESISTIVE SWITCHING CHARACTERISTICS

Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 2.4\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 5\text{ Ω}$	$t_{d(on)}$		9.0		ns
Rise Time		$t_r$		7.0		
Turn-Off Delay Time		$t_{d(off)}$		15		
Fall Time		$t_f$		7.0		

### SOURCE-DRAIN DIODE CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Diode Forward Voltage	$I_S = 2.4\text{ A}, V_{GS} = 0\text{ V}$	$V_{SD}$			1.6	V
Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$	$t_{rr}$		240		ns
Reverse Recovery Charge	$I_S = 2.4\text{ A}, di/dt = 100\text{ A/μs}$	$Q_{rr}$		0.7		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.

6. Guaranteed by design.

TYPICAL CHARACTERISTICS

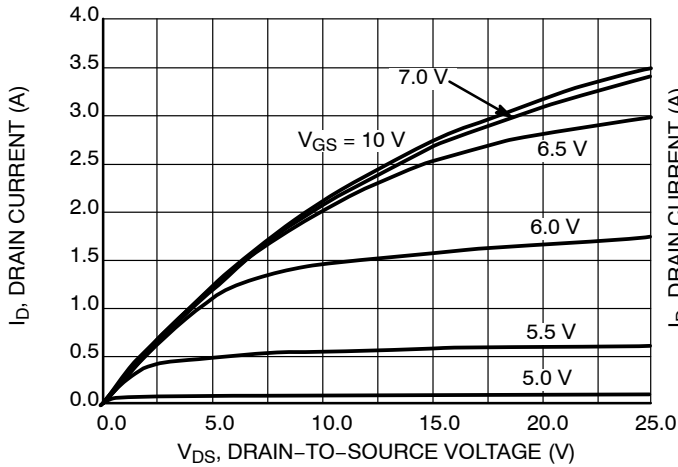


Figure 1. On-Region Characteristics

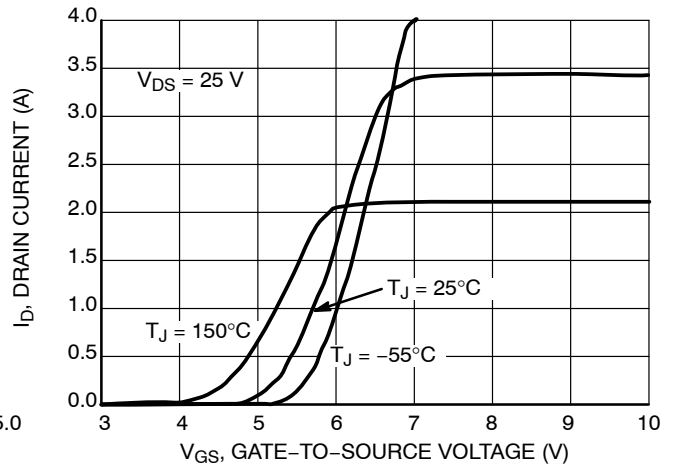


Figure 2. Transfer Characteristics

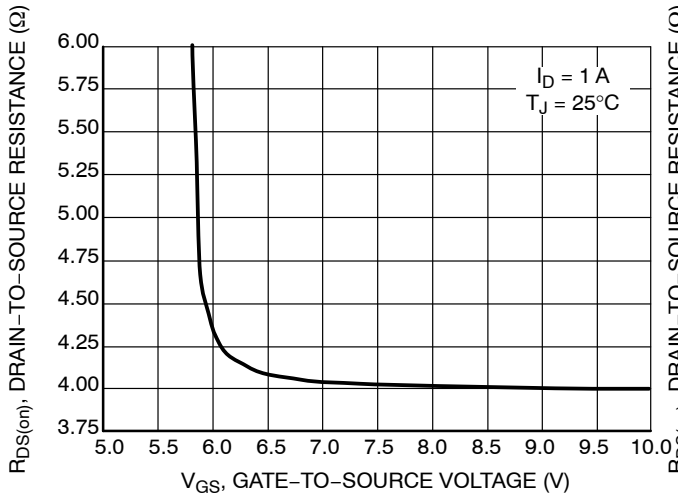


Figure 3. On-Region versus Gate-to-Source Voltage

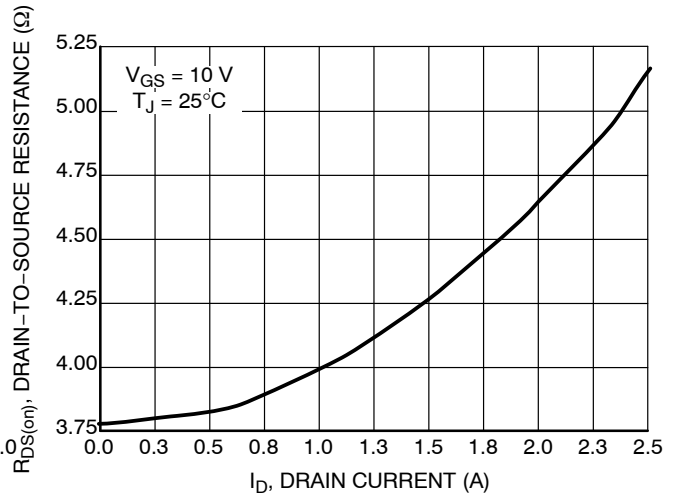


Figure 4. On-Resistance versus Drain Current and Gate Voltage

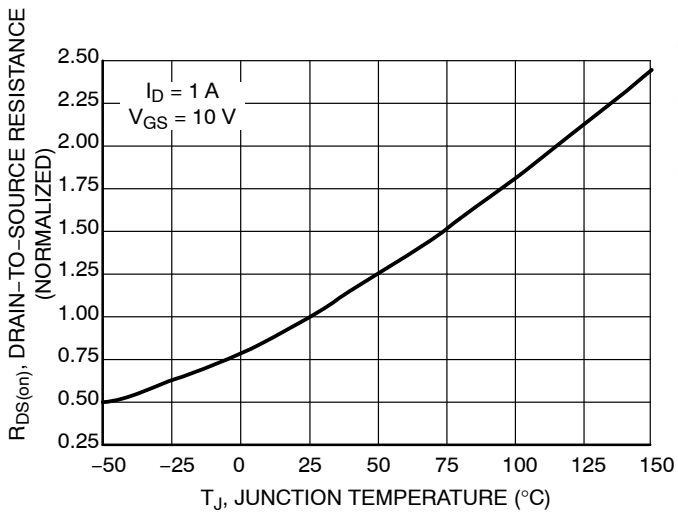


Figure 5. On-Resistance Variation with Temperature

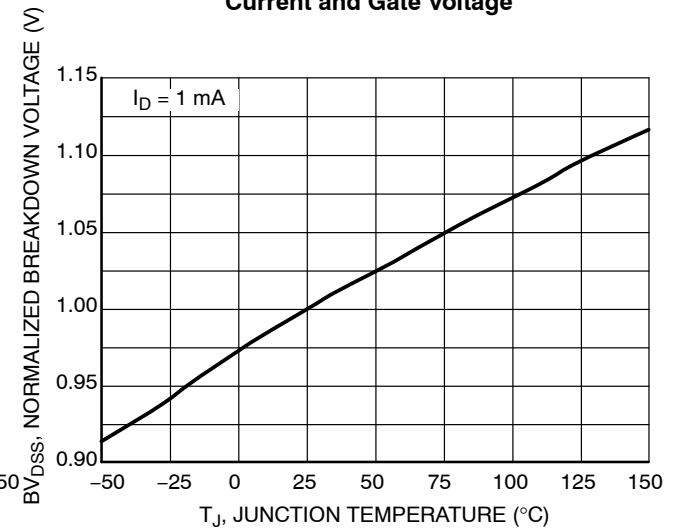


Figure 6.  $BV_{DSS}$  Variation with Temperature

TYPICAL CHARACTERISTICS

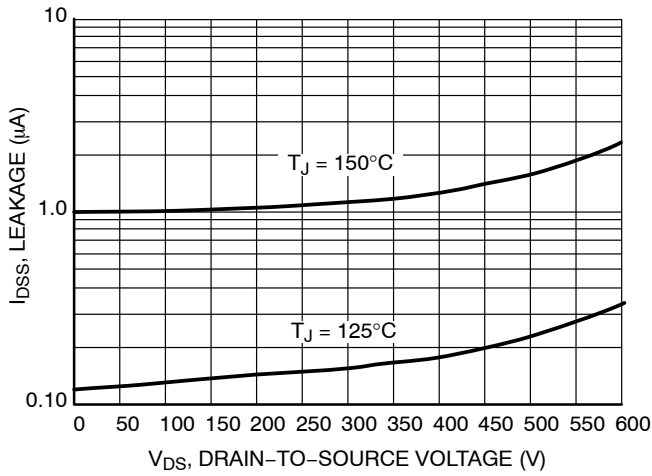


Figure 7. Drain-to-Source Leakage Current versus Voltage

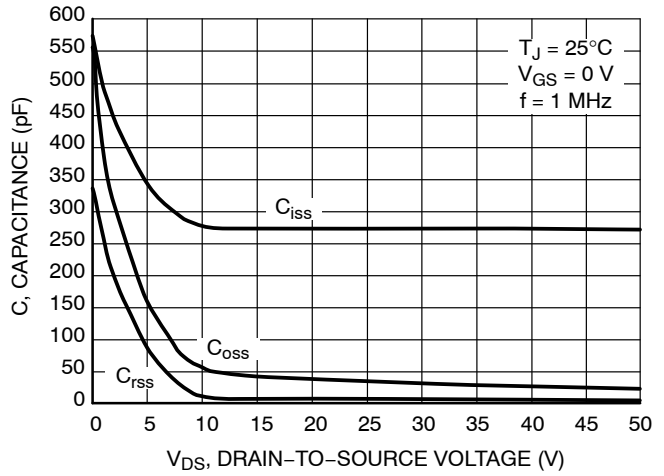


Figure 8. Capacitance Variation

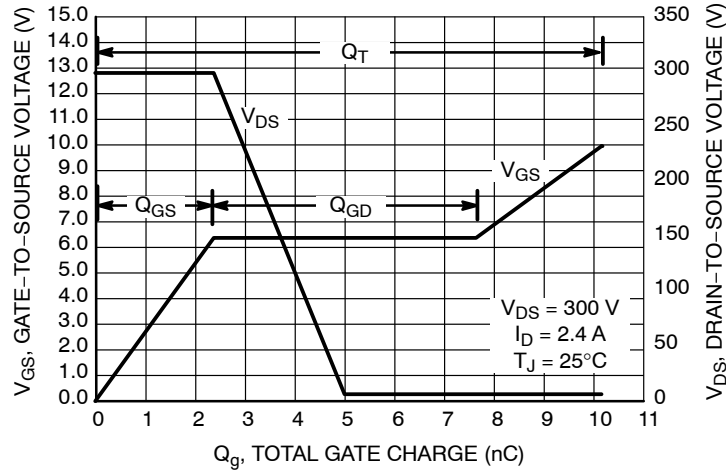


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

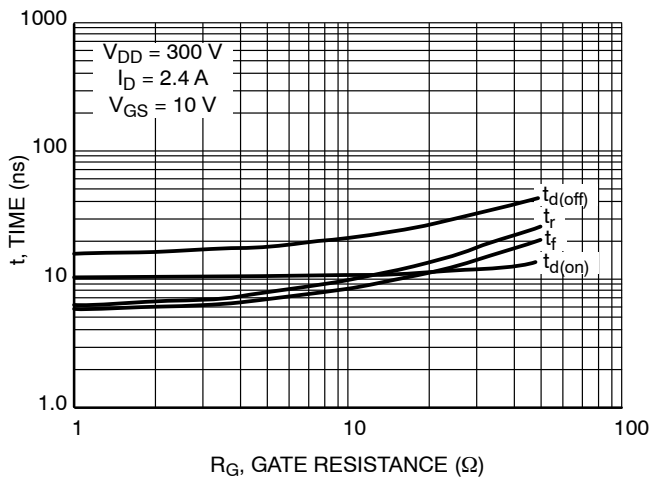


Figure 10. Resistive Switching Time Variation versus Gate Resistance

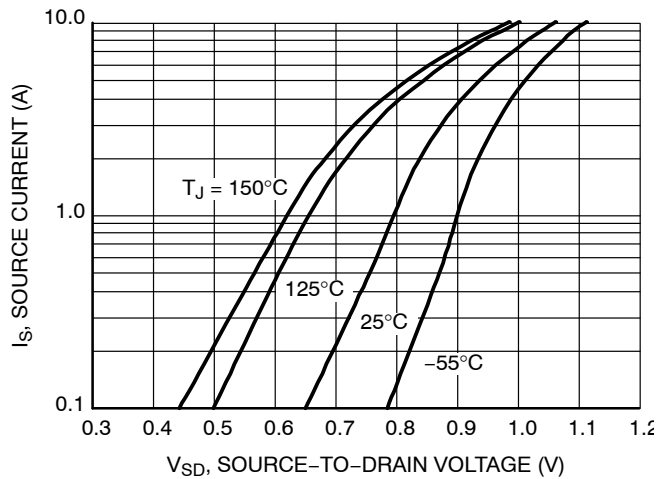


Figure 11. Diode Forward Voltage versus Current

# NDF02N60Z, NDD02N60Z

## TYPICAL CHARACTERISTICS

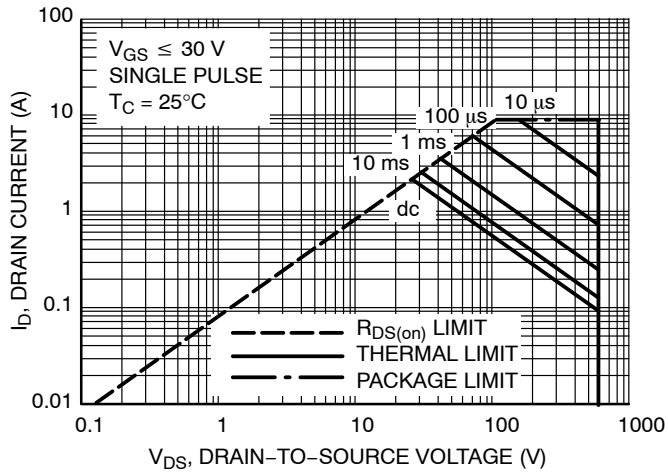


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDD02N60Z

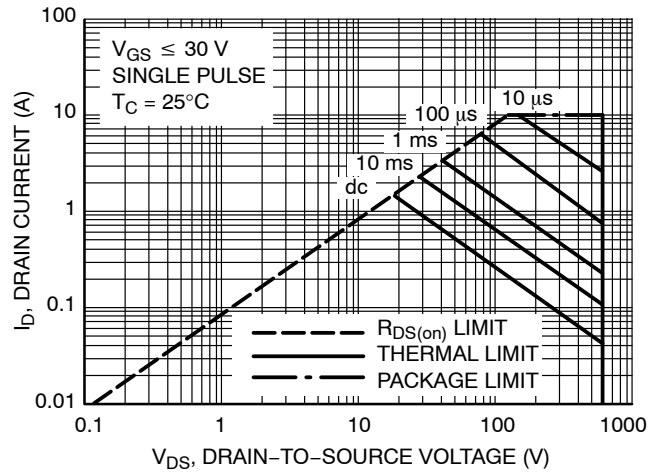


Figure 13. Maximum Rated Forward Biased Safe Operating Area NDF02N60Z

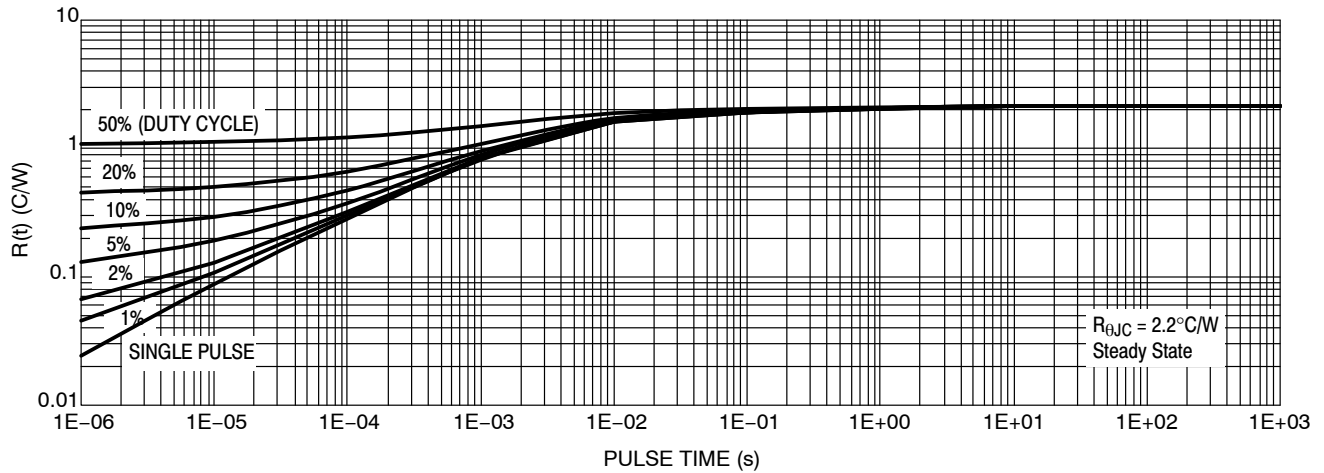


Figure 14. Thermal Impedance (Junction-to-Case) for NDD02N60Z

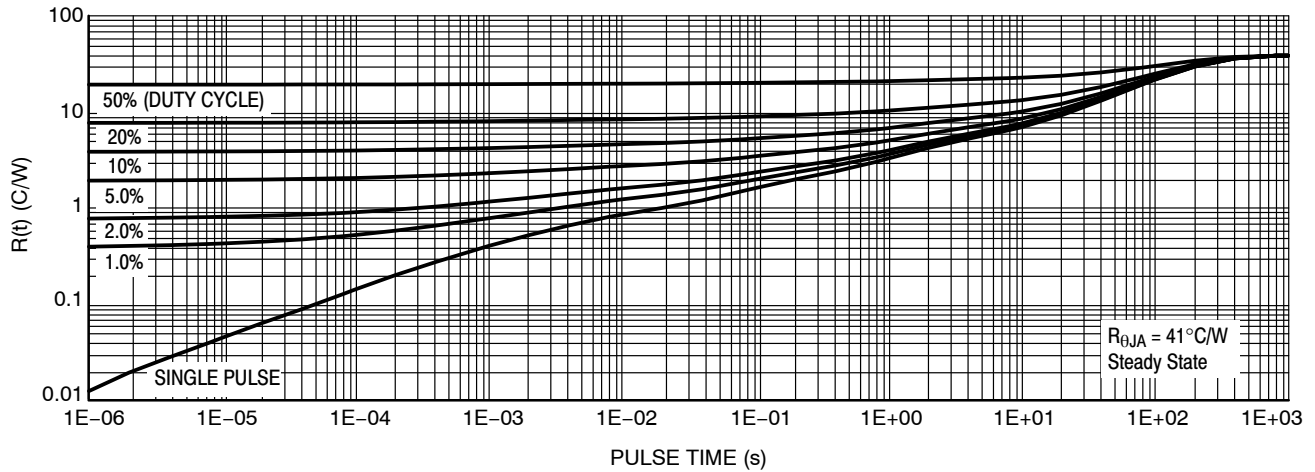
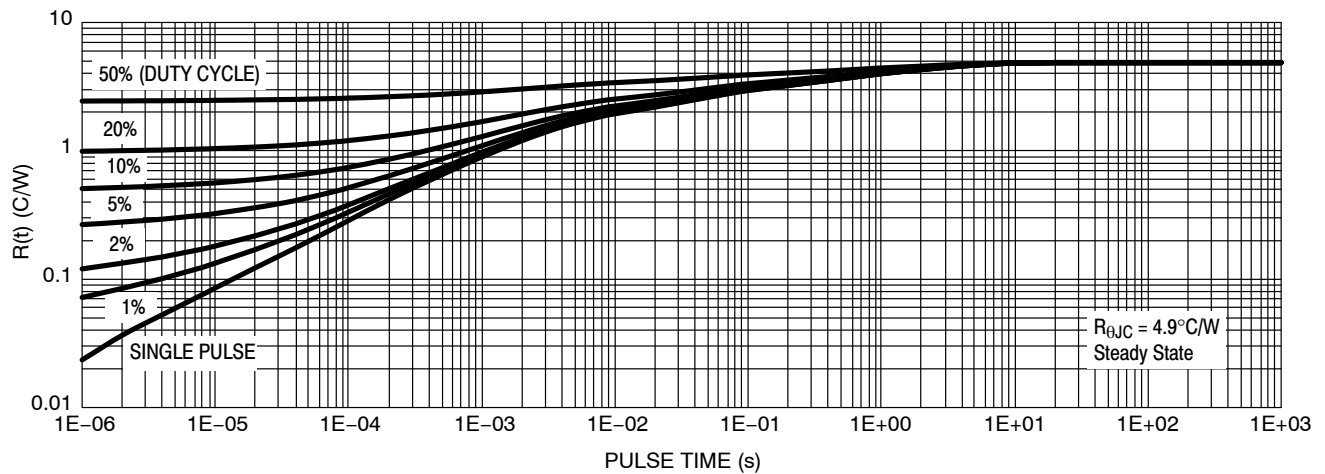
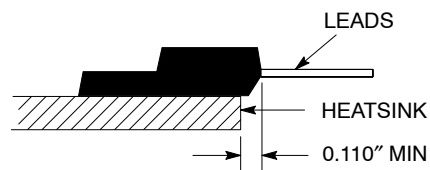


Figure 15. Thermal Impedance (Junction-to-Ambient) for NDD02N60Z

## NDF02N60Z, NDD02N60Z



**Figure 16. Thermal Impedance (Junction-to-Case) for NDF02N60Z**



**Figure 17. Isolation Test Diagram**

Measurement made between leads and heatsink with all leads shorted together.

\*For additional mounting information, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

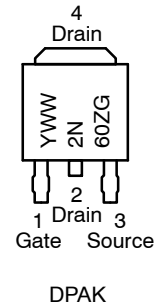
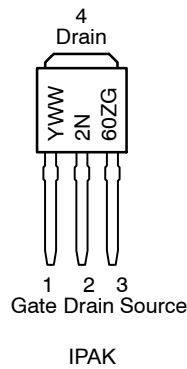
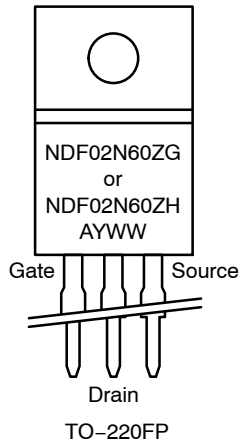
# NDF02N60Z, NDD02N60Z

## ORDERING INFORMATION

Order Number	Package	Shipping <sup>†</sup>
NDF02N60ZG	TO-220FP (Pb-Free, Halogen-Free)	50 Units / Rail
NDF02N60ZH	TO-220FP (Pb-Free, Halogen-Free)	50 Units / Rail
NDD02N60Z-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDD02N60ZT4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape and Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## MARKING DIAGRAMS



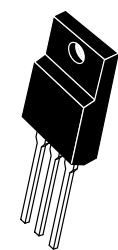
A = Location Code  
Y = Year  
WW = Work Week  
G, H = Pb-Free, Halogen-Free Package

### TO-220 FULLPACK, 3-LEAD

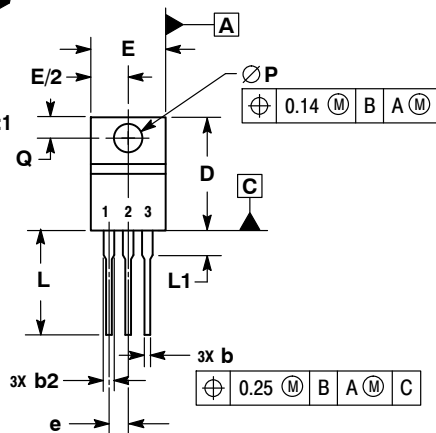
#### CASE 221AH

#### ISSUE F

DATE 30 SEP 2014

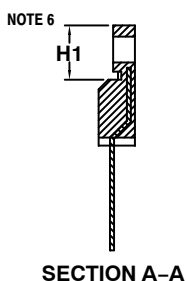
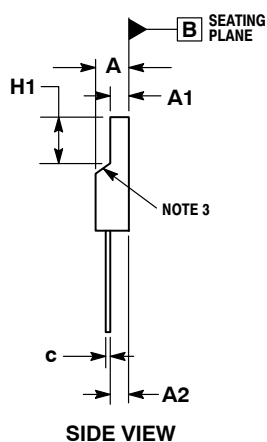
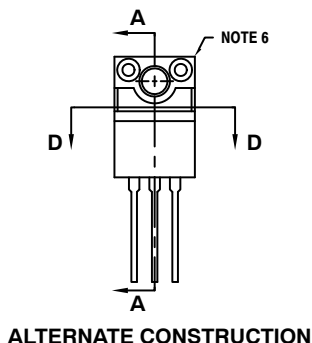


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FRONT VIEW

SECTION D-D

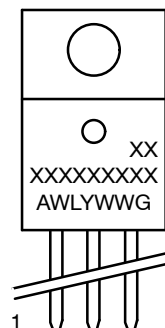


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR UNCONTROLLED IN THIS AREA.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.13 PER SIDE. THESE DIMENSIONS ARE TO BE MEASURED AT OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION. LEAD WIDTH INCLUDING PROTRUSION SHALL NOT EXCEED 2.00.
6. CONTOURS AND FEATURES OF THE MOLDED PACKAGE BODY MAY VARY WITHIN THE ENVELOPE DEFINED BY DIMENSIONS A1 AND H1 FOR MANUFACTURING PURPOSES.

DIM	MIN	MAX
A	4.30	4.70
A1	2.50	2.90
A2	2.50	2.90
b	0.54	0.84
b2	1.10	1.40
c	0.49	0.79
D	14.70	15.30
E	9.70	10.30
e	2.54 BSC	
H1	6.60	7.10
L	12.50	14.73
L1	---	2.80
P	3.00	3.40
Q	2.80	3.20

#### GENERIC MARKING DIAGRAM\*



A = Assembly Location  
 WL = Wafer Lot  
 Y = Year  
 WW = Work Week  
 G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.  
 Pb-Free indicator, "G" or microdot "▪", may or may not be present.

#### STYLE 1:

- PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE

#### STYLE 2:

- PIN 1. CATHODE
2. ANODE
3. GATE

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DESCRIPTION: TO-220 FULLPACK, 3-LEAD

PAGE 1 OF 1

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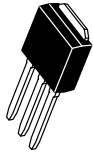


# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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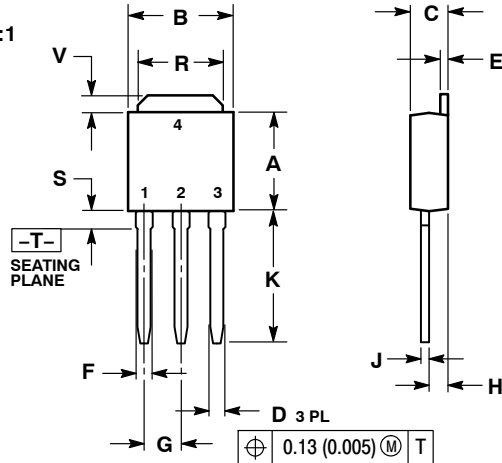
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### IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

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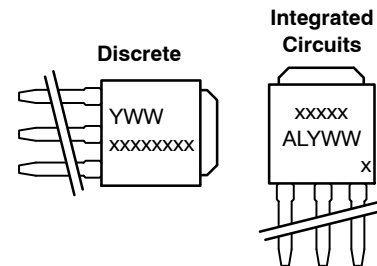
#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

### MARKING DIAGRAMS

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN
- STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE
- STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE
- STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2
- STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR



xxxxxxxx = Device Code  
A = Assembly Location  
IL = Wafer Lot  
Y = Year  
WW = Work Week

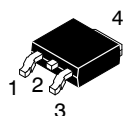
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DESCRIPTION:	IPAK (DPAK INSERTION MOUNT)	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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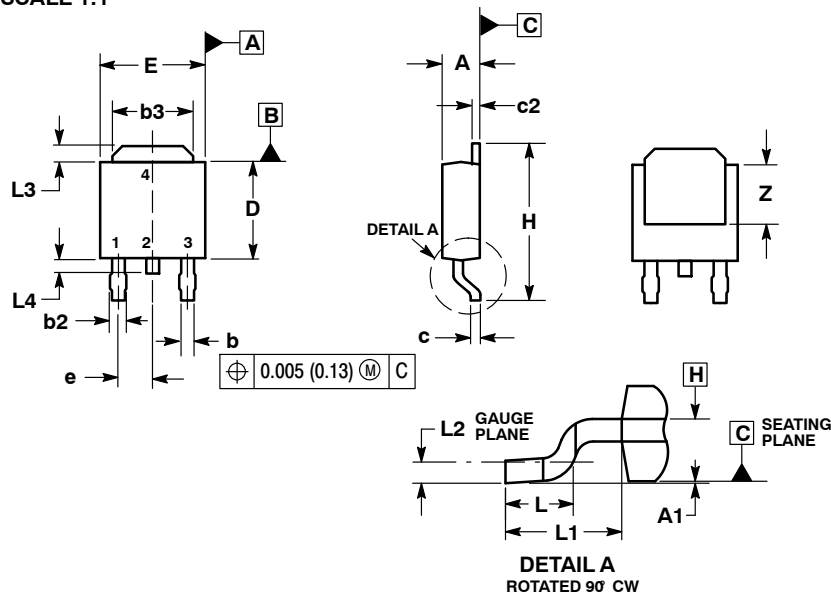
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### DPAK (SINGLE GAUGE)

#### CASE 369AA-01

#### ISSUE B

DATE 03 JUN 2010



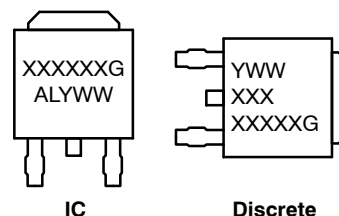
#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4		0.040		1.01
Z	0.155		3.93	

- STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR
- STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN
- STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE
- STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE
- STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE
- STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2
- STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

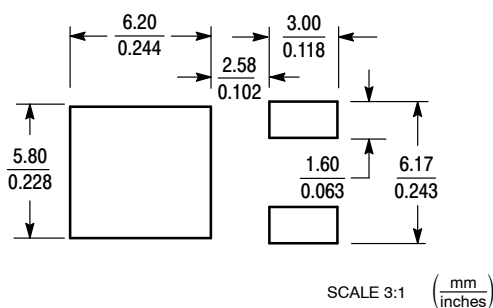
### GENERIC MARKING DIAGRAM\*



XXXXXX = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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