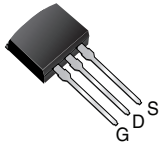
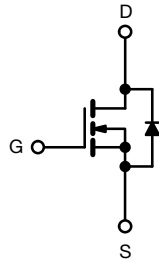
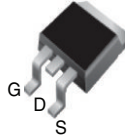


Power MOSFET

 I²PAK (TO-262)

 D²PAK (TO-263)


N-Channel MOSFET

FEATURES

- Surface-mount (IRFBF20S, SiHFBF20S)
- Low-profile through-hole (IRFBF20L, SiHFBF20L)
- Available in tape and reel (IRFBF20S, SiHFBF20S)
- Dynamic dV/dt rating
- 150 °C operating temperature
- Fast switching
- Fully avalanche rated
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS*
Available
HALOGEN
FREE
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

PRODUCT SUMMARY

V _{DS} (V)	900	
R _{DS(on)} (Ω)	V _{GS} = 10 V	8.0
Q _g max. (nC)	38	
Q _{gs} (nC)	4.7	
Q _{gd} (nC)	21	
Configuration	Single	

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The D²PAK is a surface-mount power package capable of the accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface-mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface-mount application. The through-hole version (IRFBF20L, SiHFBF20L) is available for low-profile applications.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHFBF20S-GE3	SiHFBF20STRL-GE3 ^a	SiHFBF20STRR-GE3 ^a	SiHFBF20L-GE3
Lead (Pb)-free	IRFBF20SPbF	IRFBF20STRLPbF ^a	IRFBF20STRRPbF ^a	IRFBF20LPbF

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage ^e	V _{DS}	900	V
Gate-source voltage ^e	V _{GS}	± 20	
Continuous drain current	V _{GS} at 10 V	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed drain current ^{a, e}	I _{DM}	6.8	
Linear derating factor		0.43	W/°C
Single pulse avalanche energy ^{b, e}	E _{AS}	180	mJ
Repetitive avalanche current ^a	I _{AR}	1.7	A
Repetitive avalanche energy ^a	E _{AR}	5.4	mJ
Maximum power dissipation	P _D	T _C = 25 °C	54
		T _A = 25 °C	3.1
Peak diode recovery dV/dt ^{c, e}	dV/dt	1.5	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d		300	
Mounting torque	6-32 or M3 screw	10	

Notes


- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- V_{DD} = 50 V; starting T_J = 25 °C, L = 117 mH, R_g = 25 Ω, I_{AS} = 1.7 A (see fig. 12)
- I_{SD} ≤ 1.7 A, di/dt ≤ 70 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C
- 1.6 mm from case
- Uses IRFBF20, SiHFBF20 data and test conditions



THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient (PCB mounted, steady-state) ^a	R _{thJA}	-	40	°C/W
Maximum junction-to-case	R _{thJC}	-	2.3	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material)

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0, I _D = 250 μA		900	-	-	V
V _{DS} temperature coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	1.1	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 900 V, V _{GS} = 0 V		-	-	100	μA
		V _{DS} = 720 V, V _{GS} = 0 V, T _J = 125 °C		-	-	500	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 1.0 A ^b	-	-	8.0	Ω
Forward transconductance	g _{fs}	V _{DS} = 50 V, I _D = 1.0 A ^b		0.6	-	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	490	-	pF
Output capacitance	C _{oss}			-	55	-	
Reverse transfer capacitance	C _{rss}			-	18	-	
Total gate charge	Q _g	V _{GS} = 10 V	I _D = 1.7 A, V _{DS} = 360 V, see fig. 6 and 13 ^b	-	-	38	nC
Gate-source charge	Q _{gs}			-	-	4.7	
Gate-drain charge	Q _{gd}			-	-	21	
Turn-on delay time	t _{d(on)}	V _{DD} = 450 V, I _D = 1.7 A, R _g = 18 Ω, V _{GS} = 10 V, see fig. 10 ^b		-	8.0	-	ns
Rise time	t _r			-	21	-	
Turn-off delay time	t _{d(off)}			-	56	-	
Fall time	t _f			-	32	-	
Gate input resistance	R _g	f = 1 MHz, open drain		0.6	-	3.4	Ω
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	1.7	A
Pulsed diode forward current ^a	I _{SM}			-	-	6.8	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = 1.7 A, V _{GS} = 0 V ^b		-	-	1.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = 1.7 A, dI/dt = 100 A/μs ^b		-	350	530	ns
Body diode reverse recovery charge	Q _{rr}			-	0.85	1.3	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %
- c. Uses IRFBF20/SiHF20 data and test conditions



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

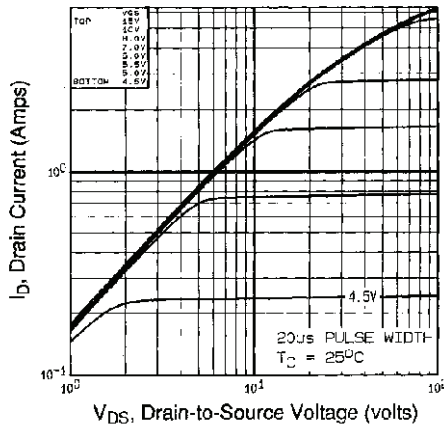


Fig. 1 - Typical Output Characteristics

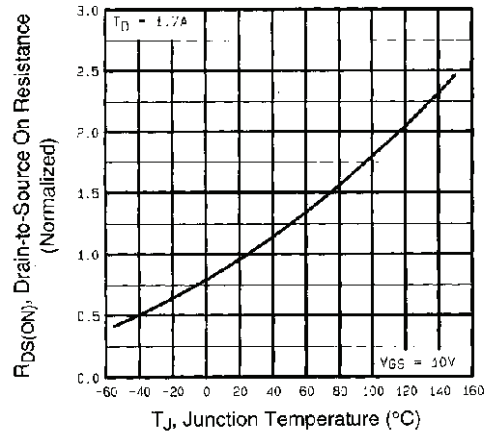


Fig. 4 - Normalized On-Resistance vs. Temperature

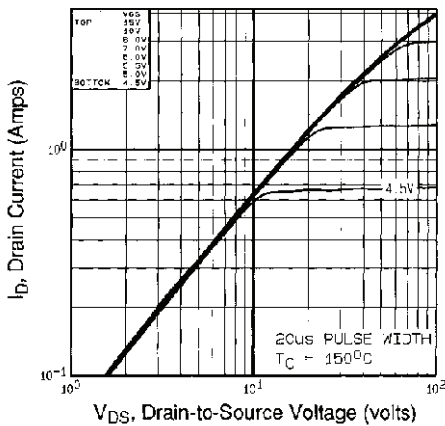


Fig. 2 - Typical Output Characteristics

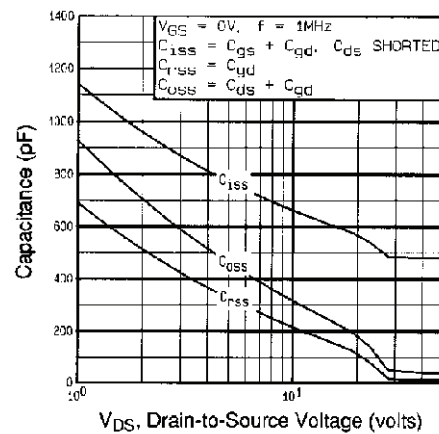


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

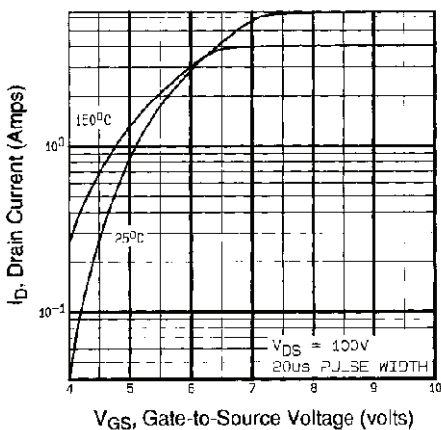


Fig. 3 - Typical Transfer Characteristics

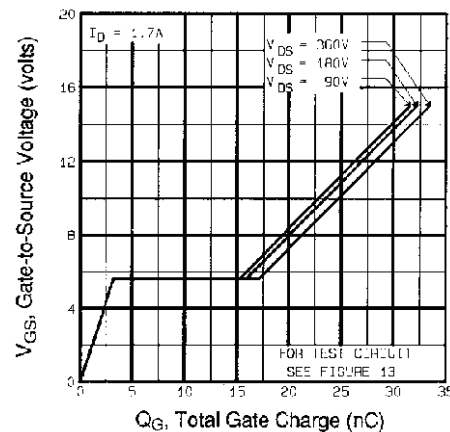


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

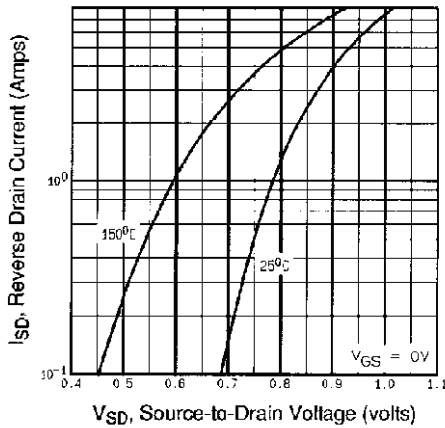


Fig. 7 - Typical Source-Drain Diode Forward Voltage

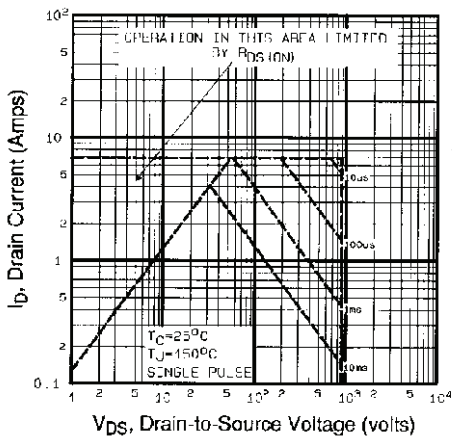


Fig. 8 - Maximum Safe Operating Area

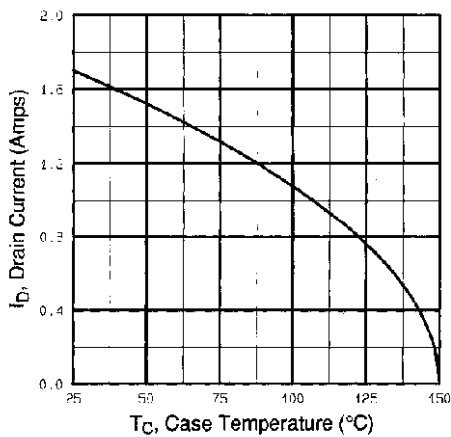


Fig. 9 - Maximum Drain Current vs. Case Temperature

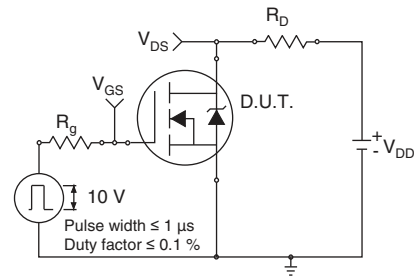


Fig. 10a - Switching Time Test Circuit

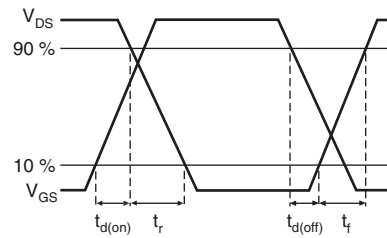


Fig. 11 - Switching Time Waveforms

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

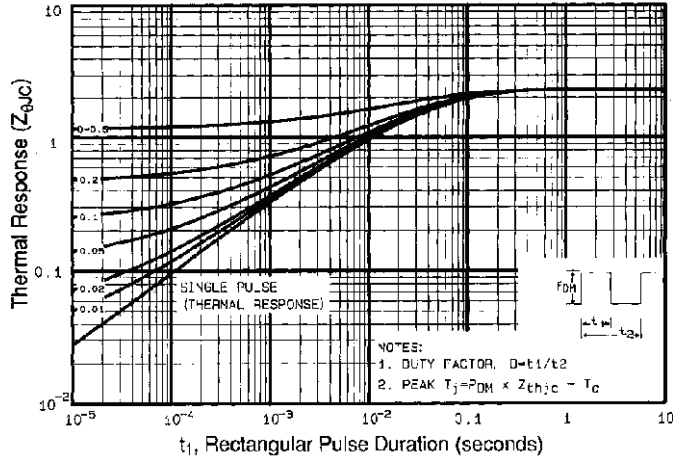


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

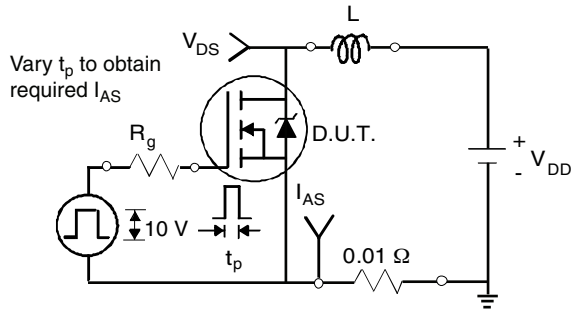


Fig. 12a - Unclamped Inductive Test Circuit

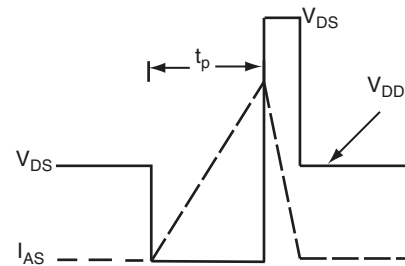


Fig. 12b - Unclamped Inductive Waveforms

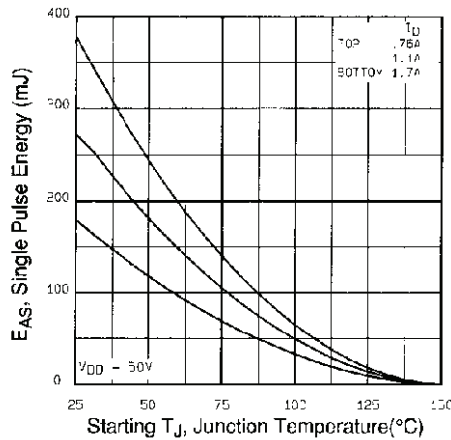


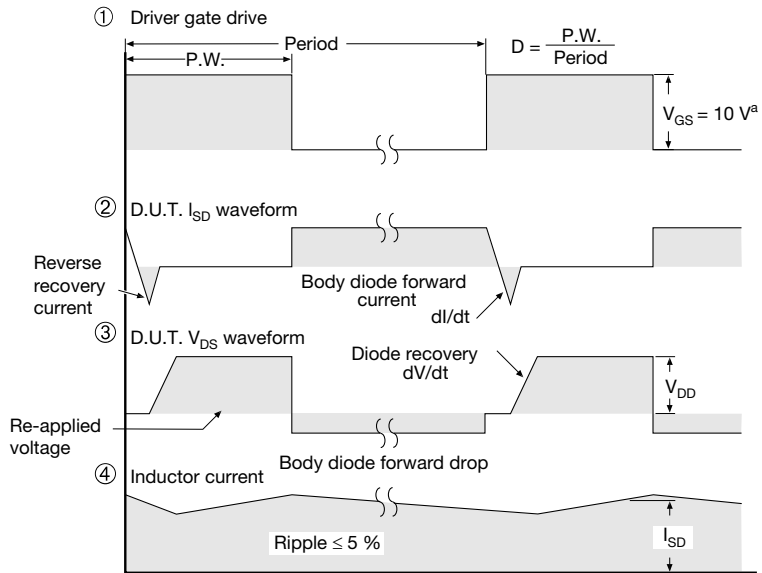
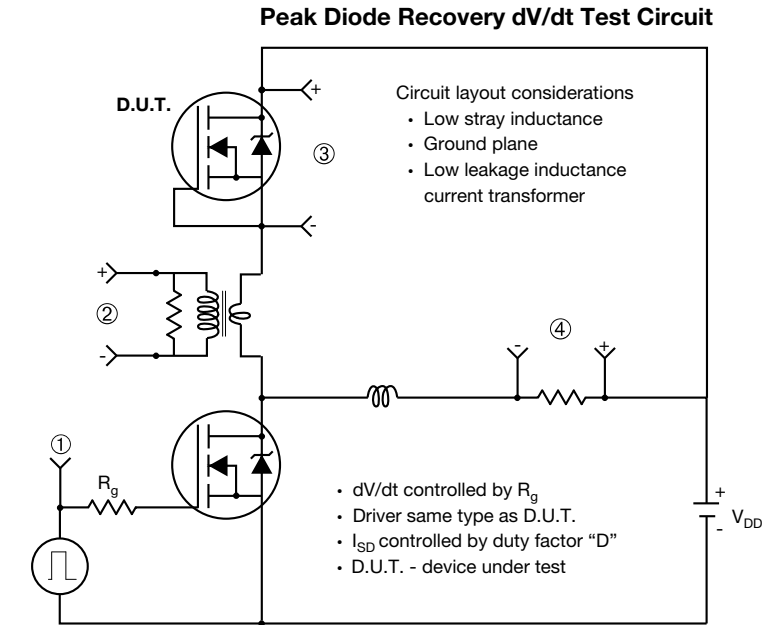
Fig. 12c - Maximum Avalanche Energy vs. Drain Current



Fig. 13a - Basic Gate Charge Waveform



Fig. 13b - Gate Charge Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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TO-263AB (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	0.00	0.25	0.000	0.010
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065
D	8.38	9.65	0.330	0.380

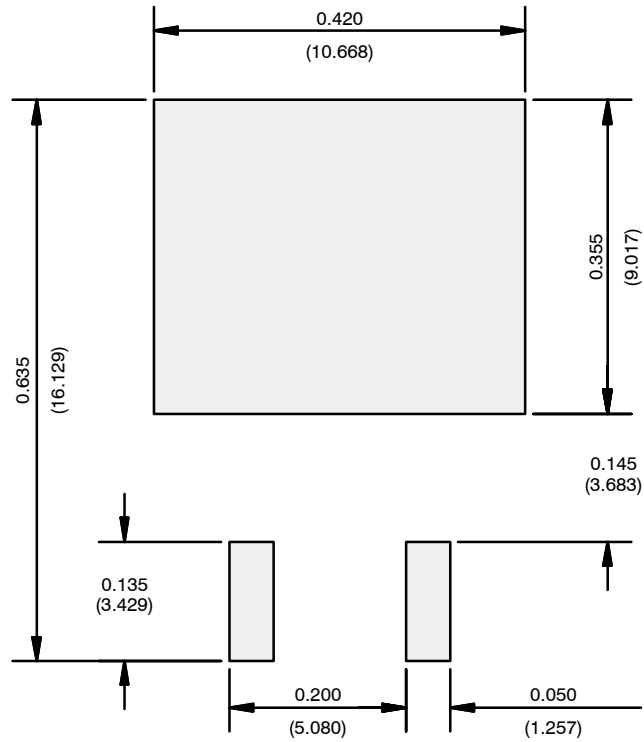
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	-	1.65	-	0.066
L2	-	1.78	-	0.070
L3	0.25 BSC		0.010 BSC	
L4	4.78	5.28	0.188	0.208

ECN: S-82110-Rev. A, 15-Sep-08
DWG: 5970

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions are shown in millimeters (inches).
3. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body at datum A.
4. Thermal PAD contour optional within dimension E, L1, D1 and E1.
5. Dimension b1 and c1 apply to base metal only.
6. Datum A and B to be determined at datum plane H.
7. Outline conforms to JEDEC outline to TO-263AB.

RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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