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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

FAIRCHILD SEMICONDUCTOR®

November 2013

FDT1600N10ALZ

N-Channel PowerTrench® MOSFET

100 V, 5.6 A, 160 mΩ

Features

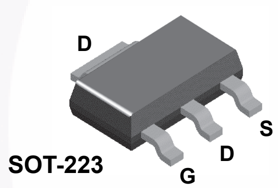
- $R_{DS(on)}$ = 121 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 2.8 A
- $R_{DS(on)}$ = 156 mΩ (Typ.) @ V_{GS} = 5 V, I_D = 1.8 A
- Low Gate Charge (Typ. 2.9 nC)
- Low C_{rss} (Typ. 2.04 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

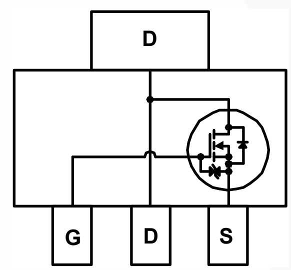
Description

This N-Channel MOSFET is produced using Fairchld Semiconductor's advanced PowerTrench® process that has been tailored to minimize the on-state resistance and maintain superior switching performance.

Application

- Consumer Appliances
- LED TV and Monitor
- Synchronous Rectification
- Uninterruptible Power Supply
- Micro Solar Inverter





MOSFET Maximum Ratings T_C = 25 °C unless otherwise noted.

Symbol	Parameter		FDT1600N10ALZ	Unit
V_{DSS}	Drain to Source Voltage		100	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	- Continuous (T_C = 25 °C)	5.6	A
		- Continuous (T_C = 100 °C)	3.5	
I_{DM}	Drain Current	- Pulsed (Note 2)	11.2	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)		9.2	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 4)		6.0	V/ns
P_D	Power Dissipation	(T_C = 25 °C)	10.42	W
		- Derate Above 25 °C	0.083	°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max. (Note 1)	12	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 1a)	60	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDT1600N10ALZ	16010ALZ	SOT-223	Tape and Reel	13"	12 mm	4000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit

Off Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 µA, V_{GS} = 0 V	100	-	-	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, referenced to 25 °C	-	0.1	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0V	-	-	1	µA
		V_{DS} = 80 V, V_{GS} = 0V, T_C = 125 °C	-	-	500	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	-	-	±10	µA

On Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 µA	1.4	-	2.8	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 2.8 A	-	121	160	mΩ
		V_{GS} = 5 V, I_D = 1.8 A	-	156	375	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 5.6 A	-	26.1	-	S

Dynamic Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	-	169	225	pF
C_{oss}	Output Capacitance		-	43	55	pF
C_{rss}	Reverse Transfer Capacitance		-	2.04	-	pF
$C_{oss(er)}$	Energy Related Output Capacitance	V_{DS} = 50 V, V_{GS} = 0 V	-	85	-	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{GS} = 10 V; V_{DD} = 50 V, I_D = 5.6 A	-	2.9	3.77	nC
$Q_{g(tot)}$	Total Gate Charge at 5V	V_{GS} = 5 V	-	1.6	2.08	nC
Q_{gs}	Gate to Source Gate Charge		-	0.7	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	0.64	-	nC
$V_{plateau}$	Gate Plateau Volatge	(Note 5)	-	3.81	-	V
Q_{sync}	Total Gate Charge Sync.	V_{DS} = 0 V, I_D = 2.8 A	-	2.45	-	nC
Q_{oss}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V	-	5.2	-	nC
ESR	Equivalent Series Resistance(G-S)	f = 1 MHz	-	2.1	-	Ω

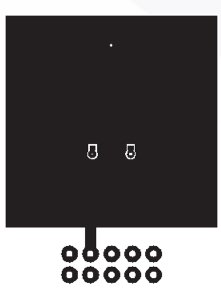
Switching Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 5.6 A, V_{GS} = 10 V, R_G = 4.7 Ω	-	7.4	24.8	ns
t_r	Rise Time		-	2.5	15	ns
$t_{d(off)}$	Turn-Off Delay Time		-	13.5	37	ns
t_f	Turn-Off Fall Time	(Note 5)	-	2.4	14.8	ns

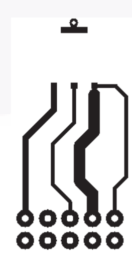
Drain-Source Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_S	Maximum Continous Drain to Source Diode Forward Current		-	-	5.6	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	11.2	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 5.6A	-	-	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 5.6A, V_{DD} = 50V, dI_F/dt = 100A/µs	-	34.1	-	ns
Q_{rr}	Reverse Recovery Charge		-	32.7	-	nC

NOTES:
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 60 °C/W when mounted on a 1 in^2 pad of 2-oz copper.



b) 118 °C/W when mounted on a minimum pad of 2 oz copper.

2. Repetitive rating: pulse-width limited by maximum junction temperature.
3. Starting T_J = 25 °C, L = 3 mH, I_{AS} = 2.47 A.
4. I_{SD} ≤ 5.6 A, di/dt ≤ 200 A/µs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
5. Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

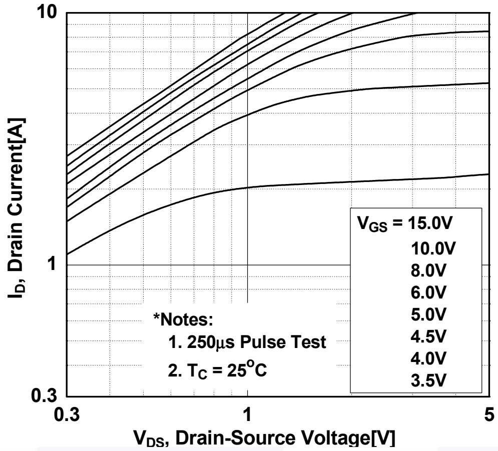


Figure 2. Transfer Characteristics

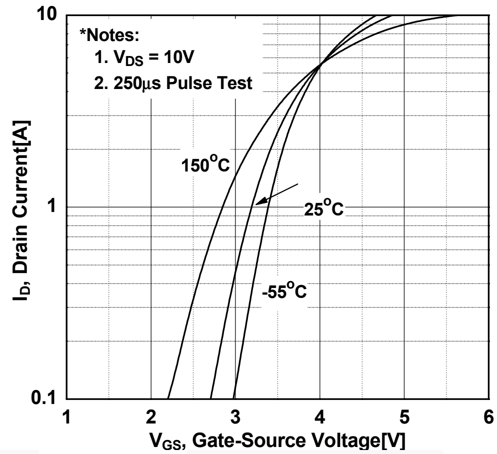


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

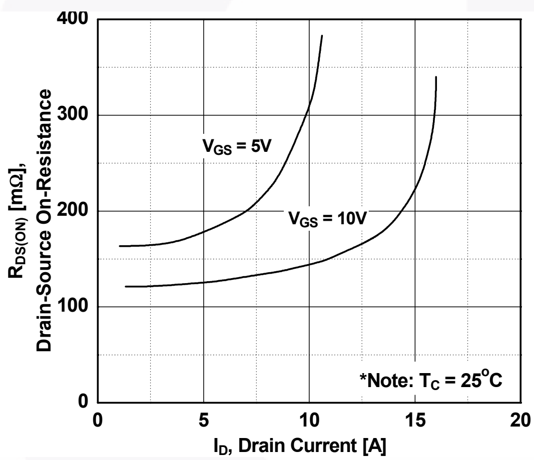


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

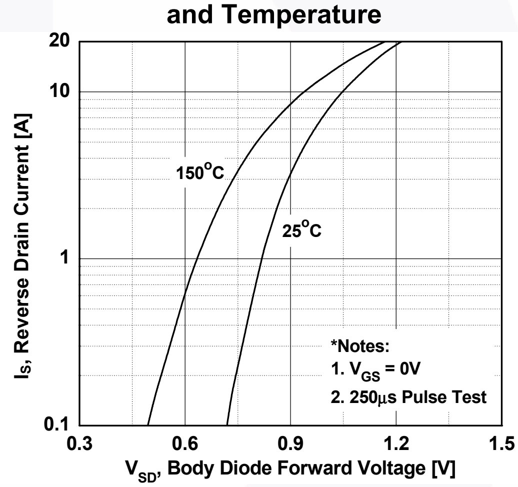


Figure 5. Capacitance Characteristics

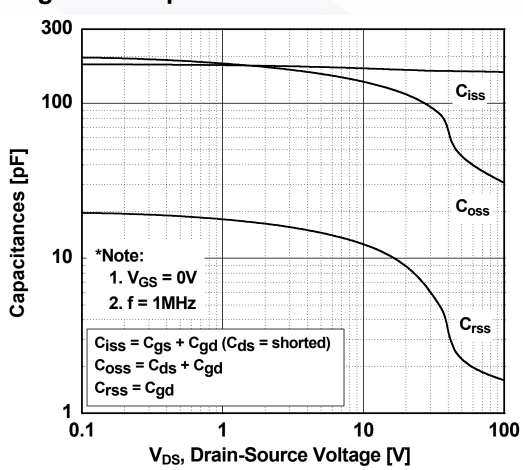
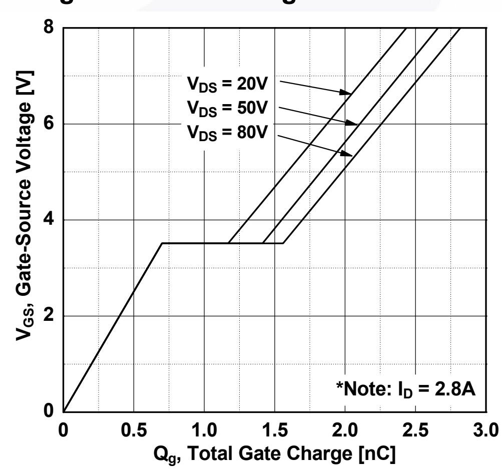


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

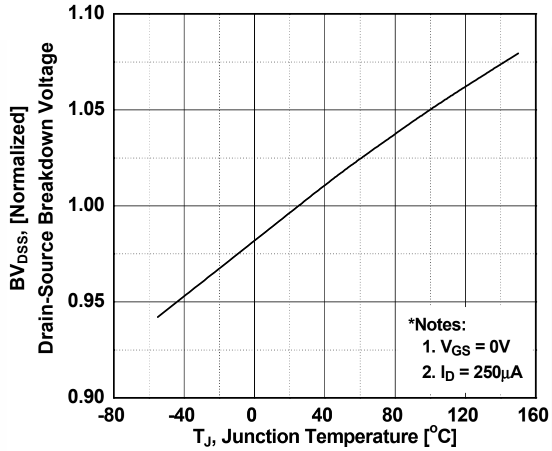


Figure 8. On-Resistance Variation vs. Temperature

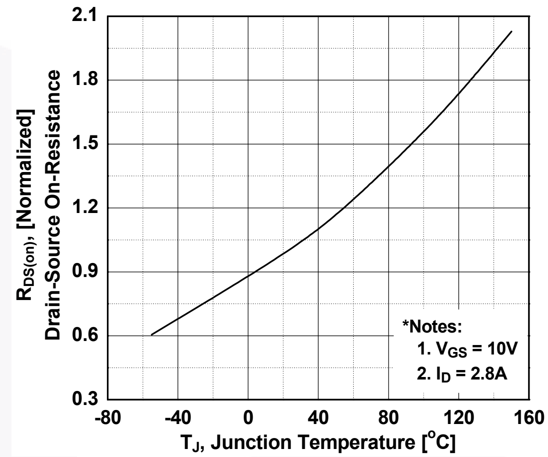


Figure 9. Maximum Safe Operating Area

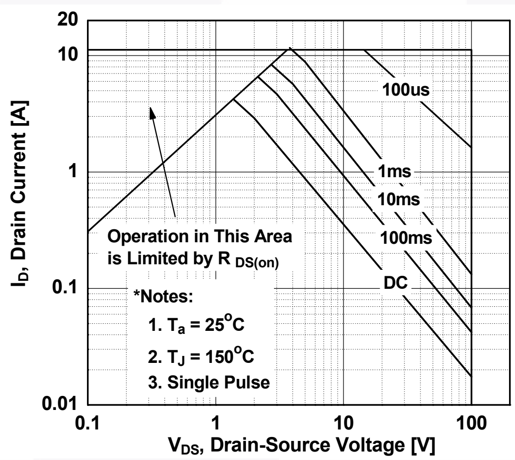


Figure 10. Maximum Drain Current vs. Case Temperature

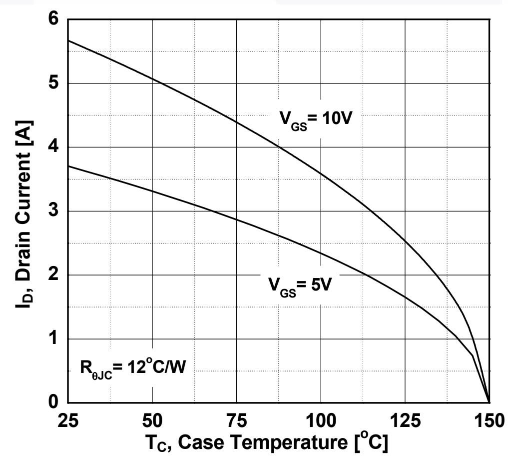


Figure 11. Eoss vs. Drain to Source Voltage

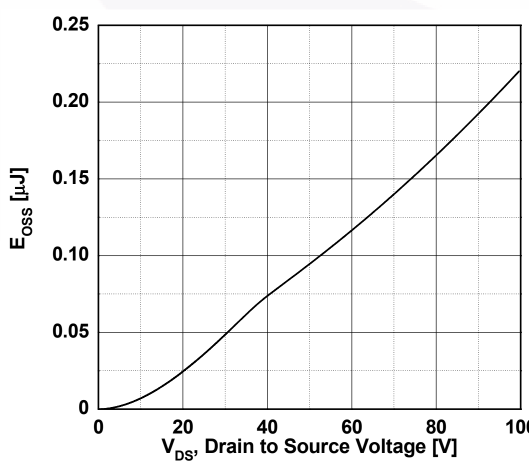
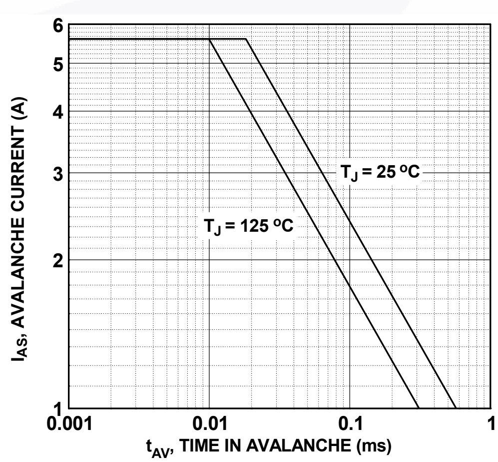
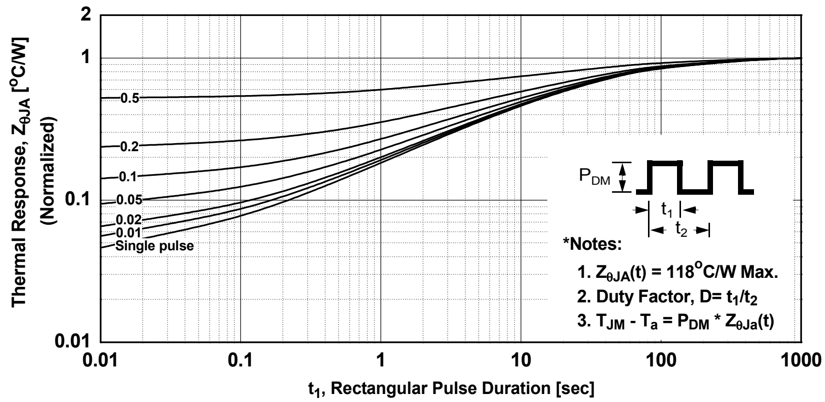


Figure 12. Unclamped Inductive Switching Capability



Typical Performance Characteristics (Continued)

Figure 13. Transient Thermal Response Curve



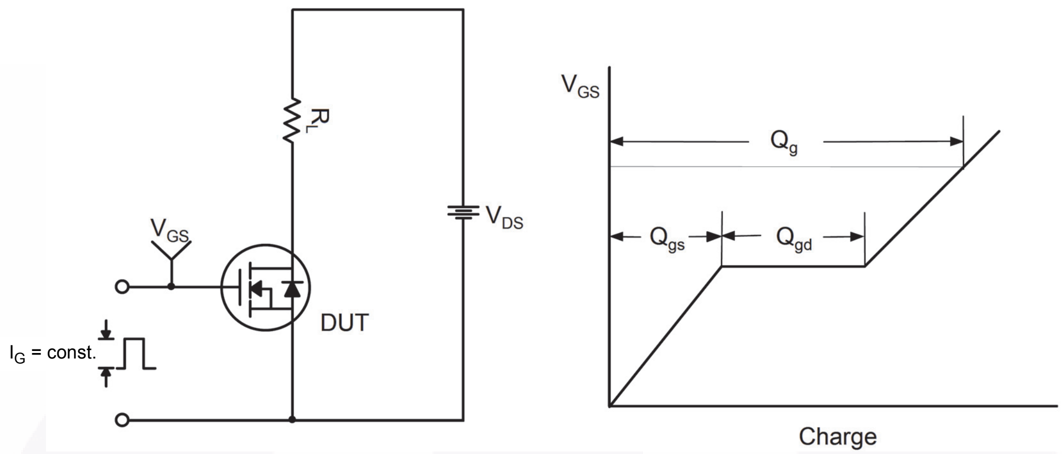


Figure 14. Gate Charge Test Circuit & Waveform

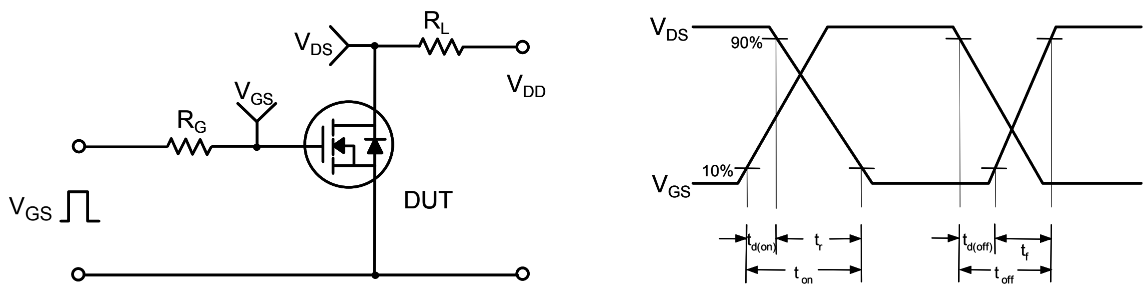


Figure 15. Resistive Switching Test Circuit & Waveforms

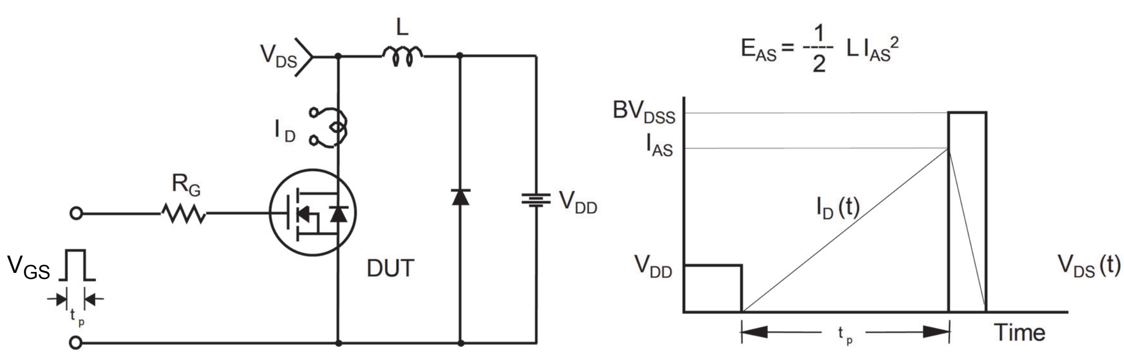


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

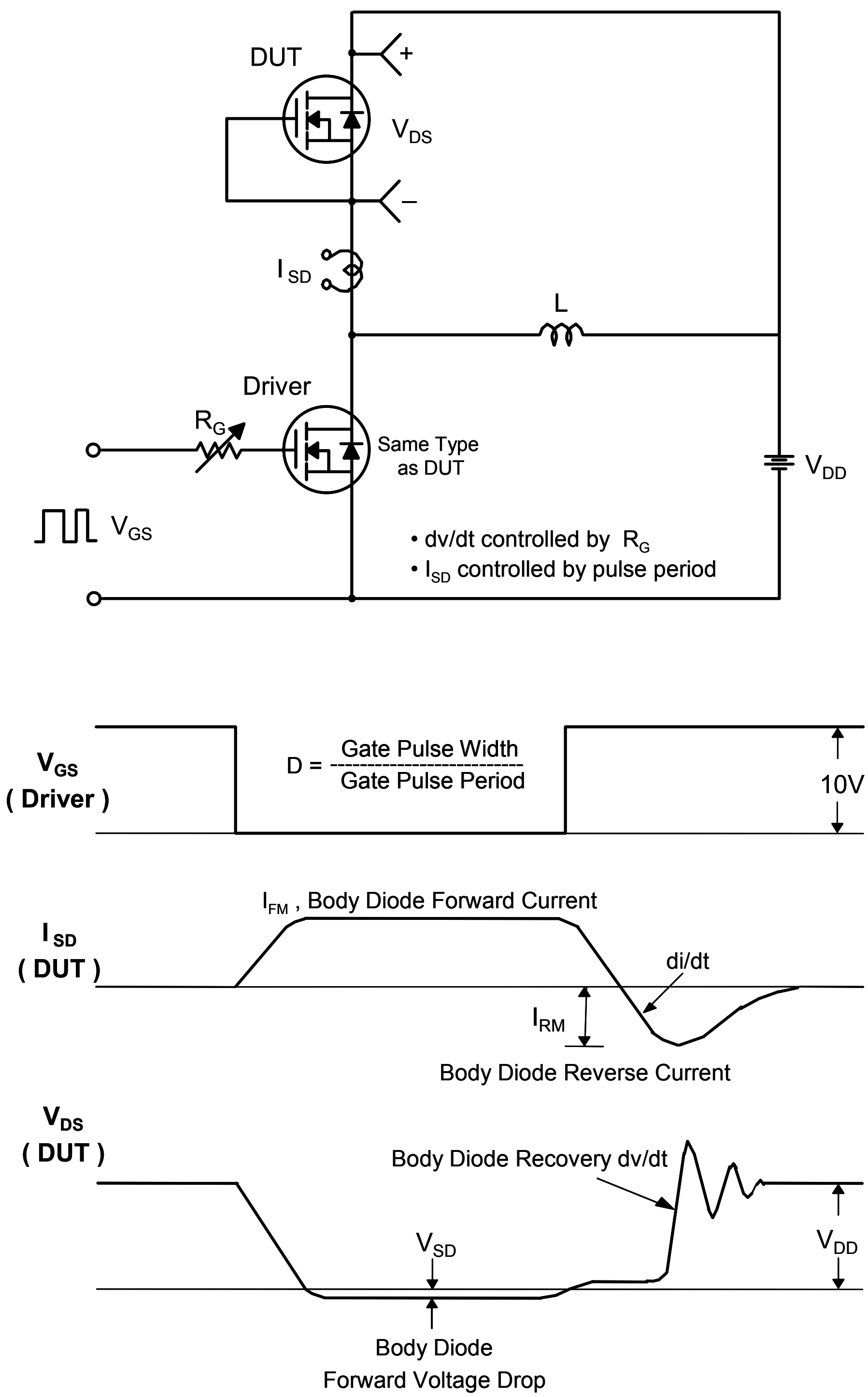


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

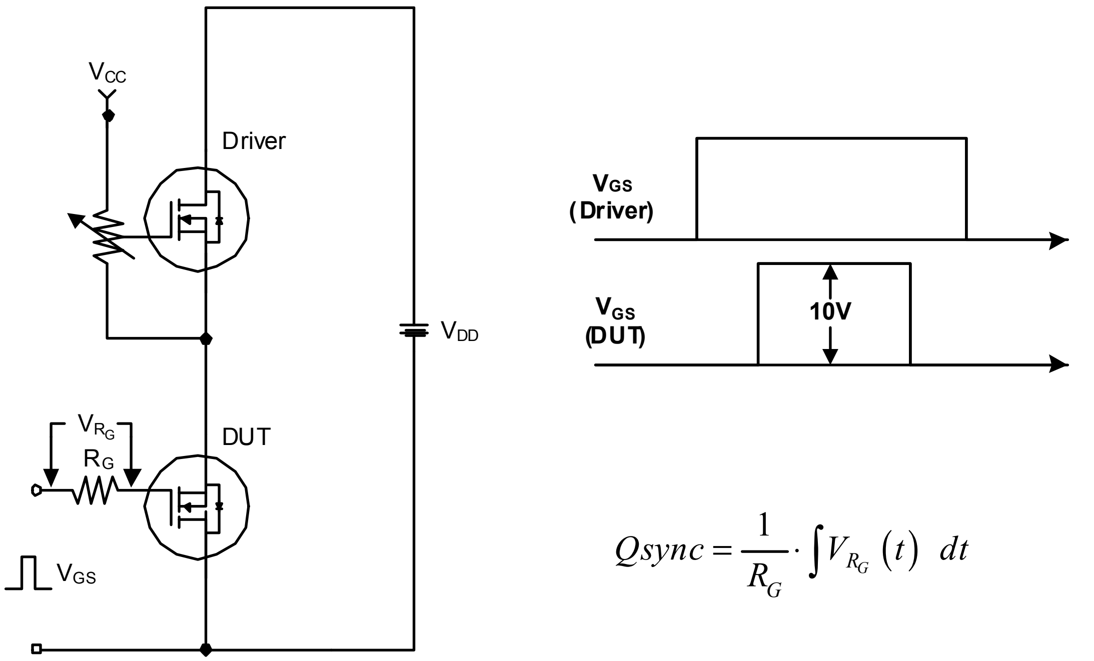


Figure 18. Total Gate Charge Qsync. Test Circuit & Waveforms

Mechanical Dimensions

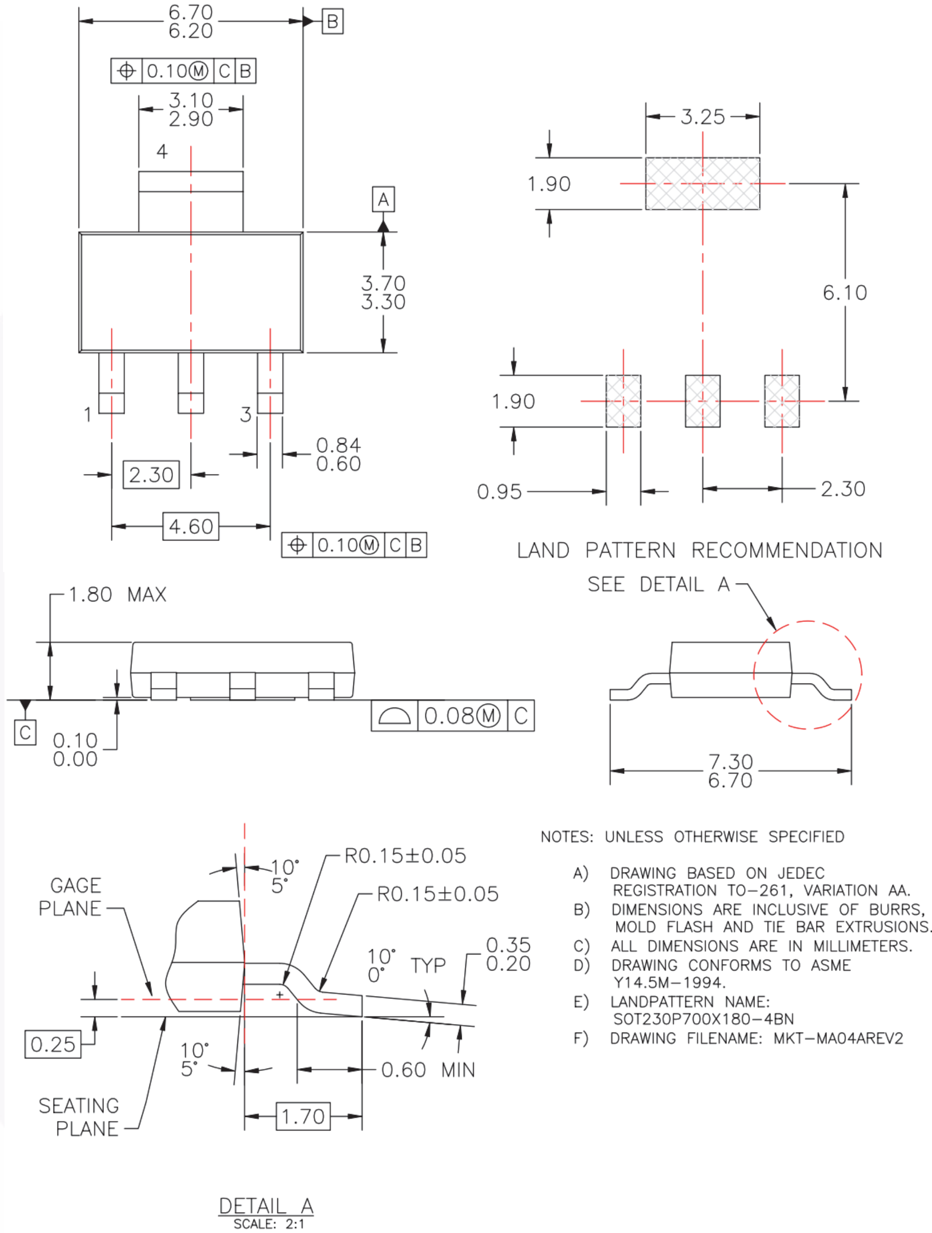


Figure 19. SOT-223, Molded, 4-Lead

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Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I66

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