

MOSFETs Silicon P-Channel MOS (U-MOSVI)

TPN4R712MD

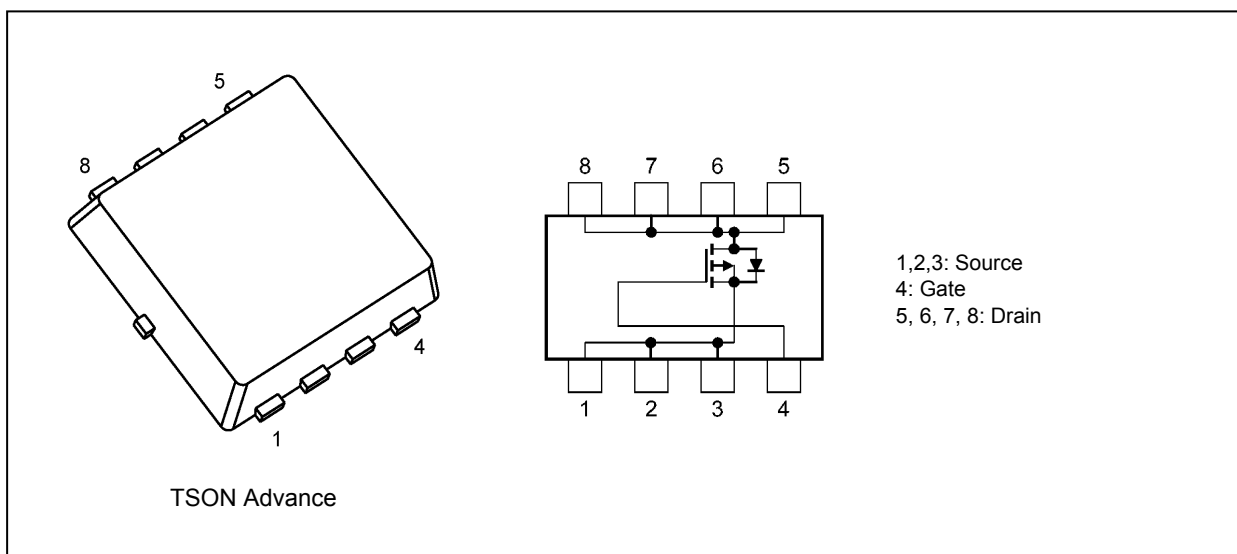
1. Applications

- Lithium-Ion Secondary Batteries
- Power Management Switches

2. Features

- (1) Low drain-source on-resistance: $R_{DS(ON)} = 3.8 \text{ m}\Omega$ (typ.) ($V_{GS} = -4.5 \text{ V}$)
- (2) Low leakage current: $I_{DSS} = -10 \text{ }\mu\text{A}$ (max) ($V_{DS} = -20 \text{ V}$)
- (3) Enhancement mode: $V_{th} = -0.5$ to -1.2 V ($V_{DS} = -10 \text{ V}$, $I_D = -1.0 \text{ mA}$)

3. Packaging and Internal Circuit



Start of commercial production

2014-12

4. Absolute Maximum Ratings (Note) ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	-20	V
Gate-source voltage	V_{GSS}	± 12	
Drain current (DC) ($T_c = 25\text{ }^\circ\text{C}$) (Note 1)	I_D	-36	A
Drain current (pulsed) ($t = 1\text{ ms}$) (Note 1)	I_{DP}	-180	
Power dissipation ($T_c = 25\text{ }^\circ\text{C}$)	P_D	42	W
Power dissipation ($t = 10\text{ s}$) (Note 2)		1.9	
Power dissipation ($t = 10\text{ s}$) (Note 3)		0.7	
Single-pulse avalanche energy (Note 4)	E_{AS}	320	mJ
Single-pulse avalanche current	I_{AS}	-36	A
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to 150	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

5. Thermal Characteristics

Characteristics	Symbol	Max	Unit
Channel-to-case thermal resistance ($T_c = 25\text{ }^\circ\text{C}$)	$R_{th(ch-c)}$	2.97	$^\circ\text{C/W}$
Channel-to-ambient thermal resistance ($t = 10\text{ s}$) (Note 2)	$R_{th(ch-a)}$	65.7	
Channel-to-ambient thermal resistance ($t = 10\text{ s}$) (Note 3)	$R_{th(ch-a)}$	178	

Note 1: Ensure that the channel temperature does not exceed $150\text{ }^\circ\text{C}$.

Note 2: Device mounted on a glass-epoxy board (a), Figure 5.1

Note 3: Device mounted on a glass-epoxy board (b), Figure 5.2

Note 4: $V_{DD} = -16\text{ V}$, $T_{ch} = 25\text{ }^\circ\text{C}$ (initial), $L = 190\text{ }\mu\text{H}$, $I_{AS} = -36\text{ A}$

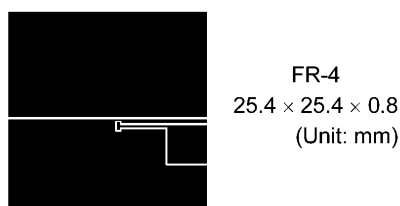


Fig. 5.1 Device Mounted on a Glass-Epoxy Board (a)

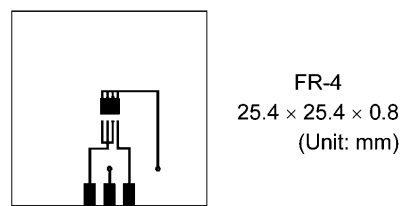


Fig. 5.2 Device Mounted on a Glass-Epoxy Board (b)

Note: This transistor is sensitive to electrostatic discharge and should be handled with care.

6. Electrical Characteristics

6.1. Static Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current	I_{GSS}	$V_{GS} = \pm 12\text{ V}, V_{DS} = 0\text{ V}$	—	—	± 0.1	μA
Drain cut-off current	I_{DSS}	$V_{DS} = -20\text{ V}, V_{GS} = 0\text{ V}$	—	—	-10	
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -10\text{ mA}, V_{GS} = 0\text{ V}$	-20	—	—	V
Drain-source breakdown voltage (Note 5)	$V_{(BR)DSX}$	$I_D = -10\text{ mA}, V_{GS} = 8.0\text{ V}$	-12	—	—	
Gate threshold voltage	V_{th}	$V_{DS} = -10\text{ V}, I_D = -1.0\text{ mA}$	-0.5	—	-1.2	
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS} = -2.5\text{ V}, I_D = -16\text{ A}$	—	6.0	8.1	$\text{m}\Omega$
		$V_{GS} = -4.5\text{ V}, I_D = -18\text{ A}$	—	3.8	4.7	

Note 5: If a reverse bias is applied between gate and source, this device enters $V_{(BR)DSX}$ mode. Note that the drain-source breakdown voltage is lowered in this mode.

6.2. Dynamic Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Input capacitance	C_{iss}	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	—	4300	—	pF
Reverse transfer capacitance	C_{rss}		—	640	—	
Output capacitance	C_{oss}		—	700	—	
Switching time (rise time)	t_r	See Fig. 6.2.1.	—	11	—	ns
Switching time (turn-on time)	t_{on}		—	18	—	
Switching time (fall time)	t_f		—	145	—	
Switching time (turn-off time)	t_{off}		—	443	—	

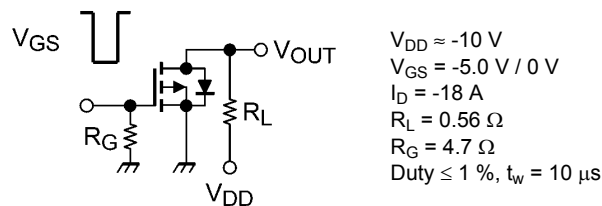


Fig. 6.2.1 Switching Time Test Circuit

6.3. Gate Charge Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Total gate charge (gate-source plus gate-drain)	Q_g	$V_{DD} \approx -16\text{ V}, V_{GS} = -5.0\text{ V}, I_D = -36\text{ A}$	—	65	—	nC
Gate-source charge 1	Q_{gs1}		—	7.5	—	
Gate-drain charge	Q_{gd}		—	20	—	

6.4. Source-Drain Characteristics ($T_a = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Reverse drain current (pulsed) (Note6)	I_{DRP}	—	—	—	-180	A
Diode forward voltage	V_{DSF}	$I_{DR} = -36\text{ A}, V_{GS} = 0\text{ V}$	—	—	1.2	V

Note6: Ensure that the channel temperature does not exceed $150\text{ }^\circ\text{C}$.

7. Marking

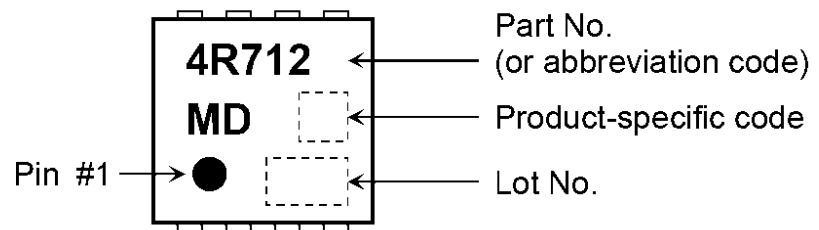


Fig. 7.1 Marking

8. Characteristics Curves (Note)

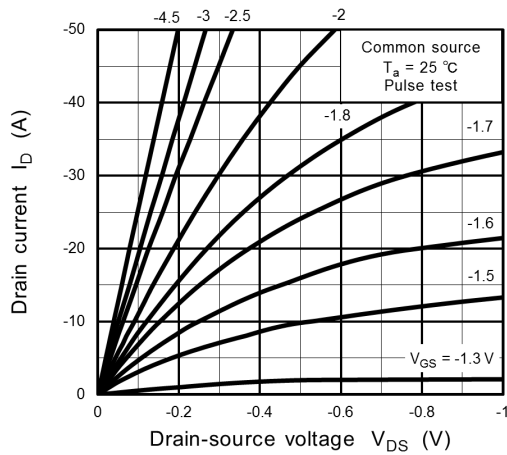


Fig. 8.1 $I_D - V_{DS}$

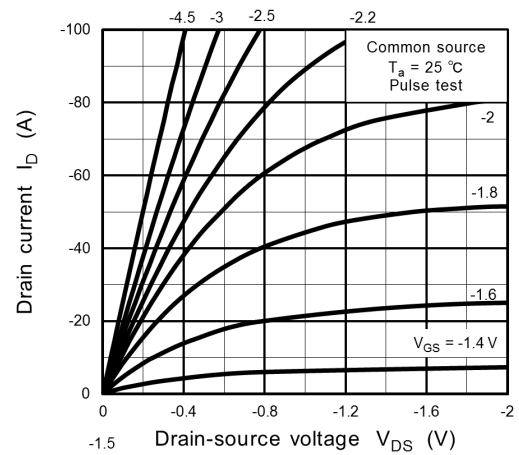


Fig. 8.2 $I_D - V_{DS}$

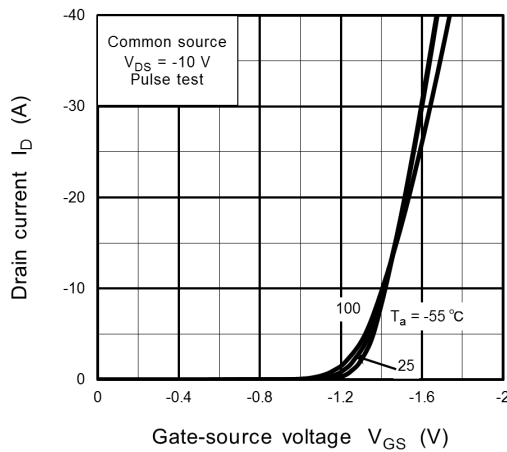


Fig. 8.3 $I_D - V_{GS}$

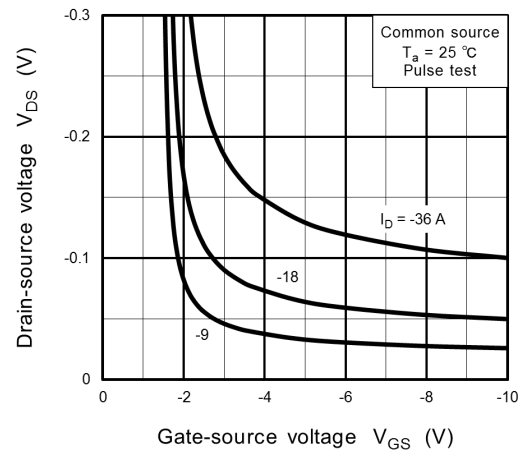


Fig. 8.4 $V_{DS} - V_{GS}$

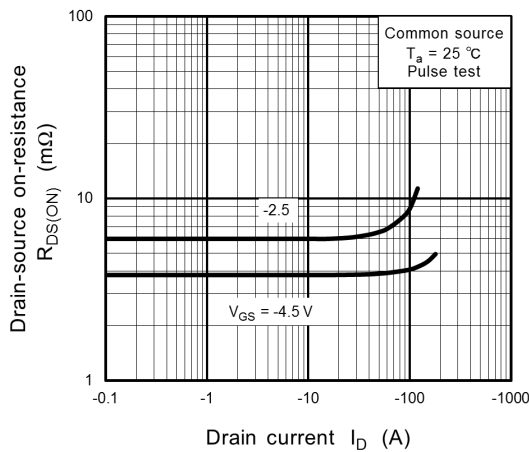


Fig. 8.5 $R_{DS(ON)} - I_D$

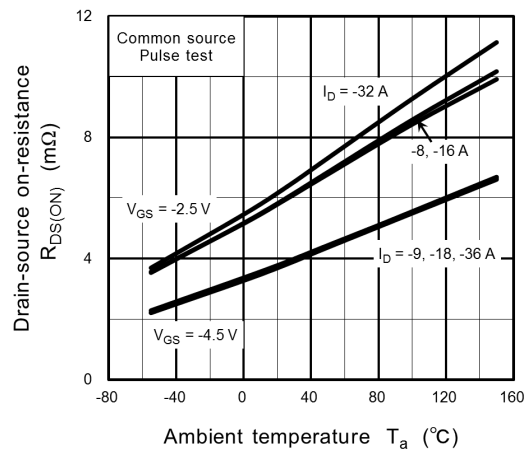


Fig. 8.6 $R_{DS(ON)} - T_a$

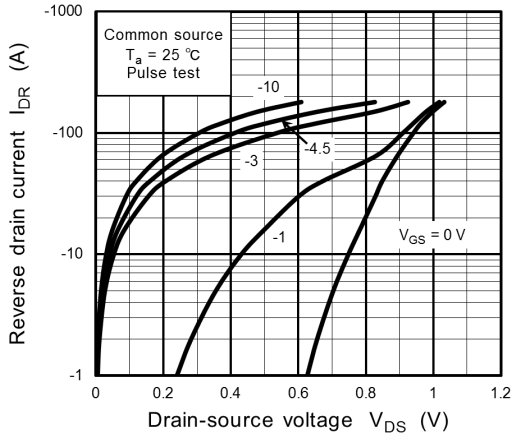


Fig. 8.7 $I_{DR} - V_{DS}$

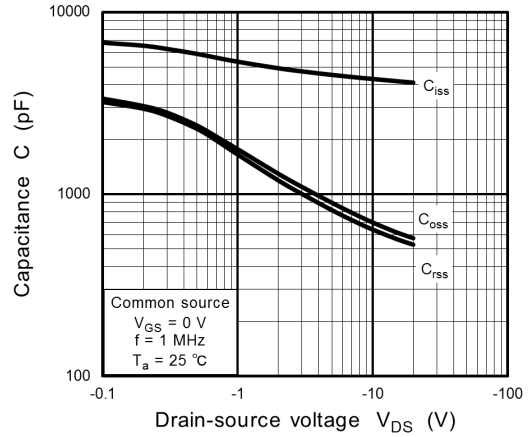


Fig. 8.8 Capacitance - V_{DS}

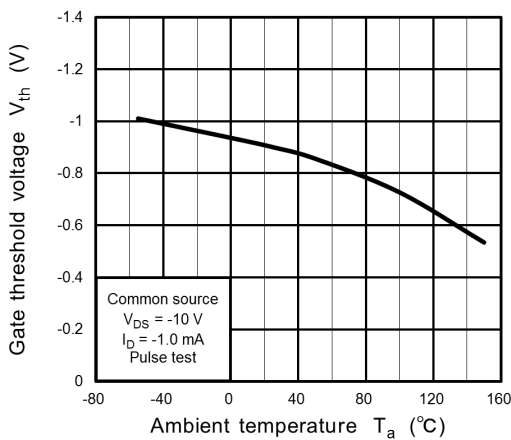


Fig. 8.9 $V_{th} - T_a$

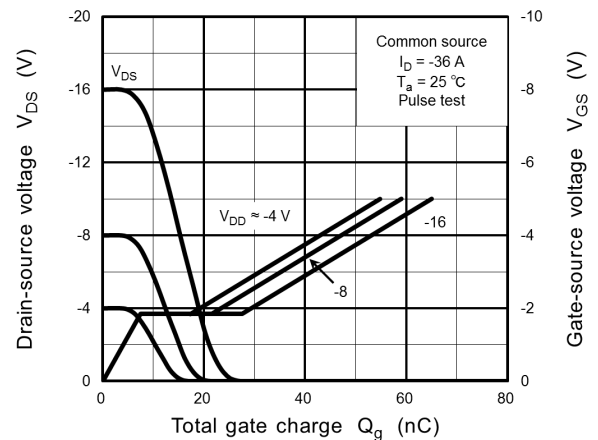
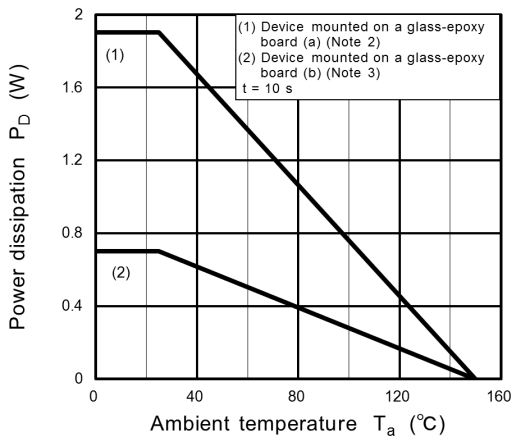
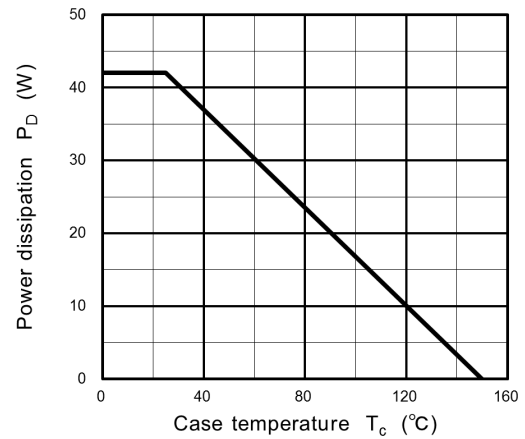


Fig. 8.10 Dynamic Input/Output Characteristics



**Fig. 8.11 $P_D - T_a$
(Guaranteed Maximum)**



**Fig. 8.12 $P_D - T_c$
(Guaranteed Maximum)**

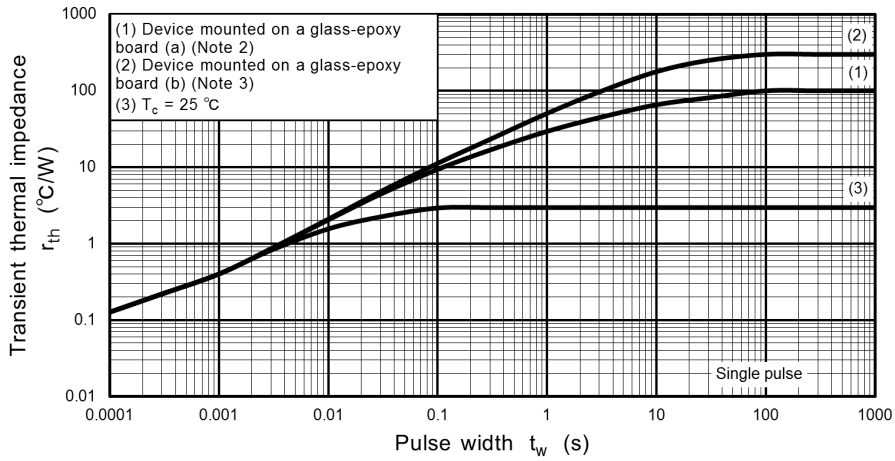


Fig. 8.13 $r_{th} - t_w$
(Guaranteed Maximum)

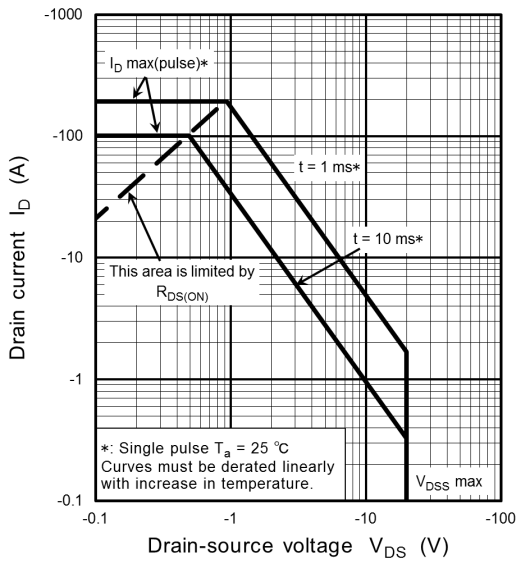


Fig. 8.14 Safe Operating Area
(Guaranteed Maximum)

Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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