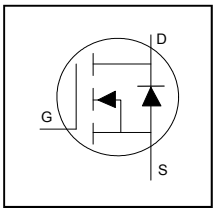
IRFS4321-7PPbF

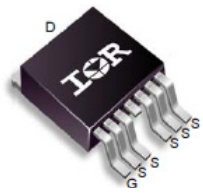
HEXFET® Power MOSFET

Application
- Motion Control Applications
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- Hard Switched and High Frequency Circuits



V_{DSS}	150V
$R_{DS(on)}$ typ.	11.7mΩ
max	14.7mΩ
I_D	86A

Benefits
- Low Rdson Reduces Losses
- Low Gate Charge Improves the Switching Performance
- Improved Diode Recovery Improves Switching & EMI Performance
- 30V Gate Voltage Rating Improves Robustness
- Fully Characterized Avalanche SOA



D^2Pak 7Pin

G	D	S
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFS4321-7PPbF	D^2Pak-7Pin	Tube	50	IRFS4321-7PPbF
		Tape and Reel Left	800	IRFS4321TRL7PP

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	86	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	61	
I_{DM}	Pulsed Drain Current ①	343	
P_D @T_C = 25°C	Maximum Power Dissipation	350	W
	Linear Derating Factor	2.3	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
$E_{AS\ (Thermally\ limited)}$	Single Pulse Avalanche Energy ②	120	mJ
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ④	——	0.43*	°C/W
$R_{\theta JA}$	Junction-to-Ambient	——	40	

* $R_{\theta JC}$ (end of life) for D2Pak and TO-262 = 0.65°C/W. This is the maximum measured value after 1000 temperature cycles from -55 to 150°C and is accounted for by the physical wear out of the die attach medium.

Notes ① through ④ are on page 2

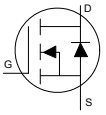
Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	150	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	150	—	mV/°C	Reference to 25°C, I_D = 1mA ①
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	11.7	14.7	mΩ	V_{GS} = 10V, I_D = 34A ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	V_{DS} = V_{GS}, I_D = 250µA
I_{DSS}	Drain-to-Source Leakage Current	—	—	20	µA	V_{DS} =150 V, V_{GS} = 0V
		—	—	1.0	mA	V_{DS} =150V,V_{GS} = 0V,T_J =125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
$R_{G(int)}$	Internal Gate Resistance	—	0.8	—	Ω	

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

gfs	Forward Transconductance	130	—	—	S	V_{DS} = 25V, I_D =50A
Q_g	Total Gate Charge	—	71	110	nC	I_D = 50A
Q_{gs}	Gate-to-Source Charge	—	24			V_{DS} = 75V
Q_{gd}	Gate-to-Drain (“Miller”) Charge	—	21			V_{GS} = 10V③
$t_{d(on)}$	Turn-On Delay Time	—	18	—	ns	V_{DD} = 98V
t_r	Rise Time	—	60	—		I_D = 50A
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		R_G= 2.5Ω
t_f	Fall Time	—	35	—		V_{GS} = 10V③
C_{iss}	Input Capacitance	—	4460	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	390	—		V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	—	82	—		f = 1.0MHz

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	86	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	343		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C,I_S = 50A,V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	—	89	130	ns	I_F = 50A,
Q_{rr}	Reverse Recovery Charge	—	300	450	nC	V_{DD} = 128V
I_{RRM}	Reverse Recovery Current	—	6.5	—	A	di/dt = 100A/µs ③

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{jmax}, starting T_J = 25°C, L = 0.096mH, R_G = 25Ω, I_{AS} = 50A, V_{GS} =10V. Part not recommended for use above this value.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ Rθ is measured at T_J approximately 90°C

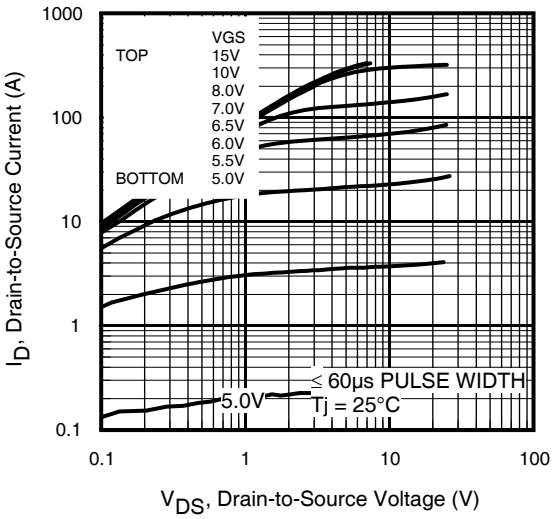


Fig 1. Typical Output Characteristics

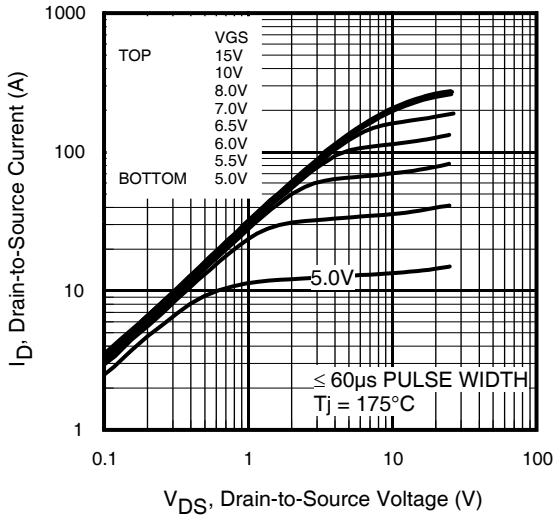


Fig 2. Typical Output Characteristics

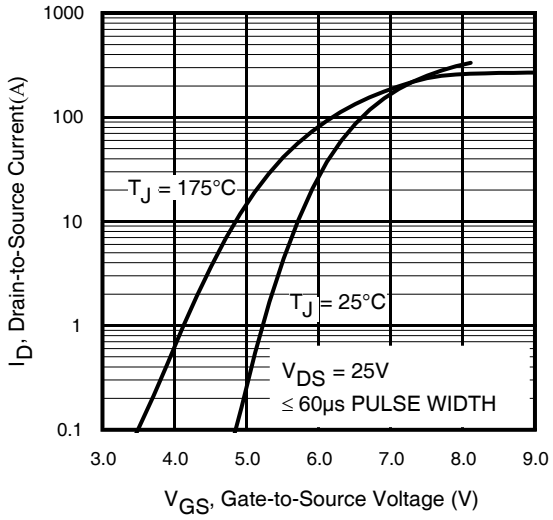


Fig 3. Typical Transfer Characteristics

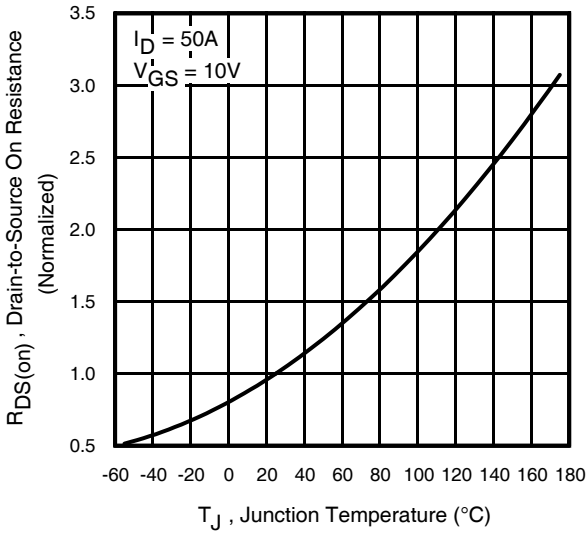


Fig 4. Normalized On-Resistance vs. Temperature

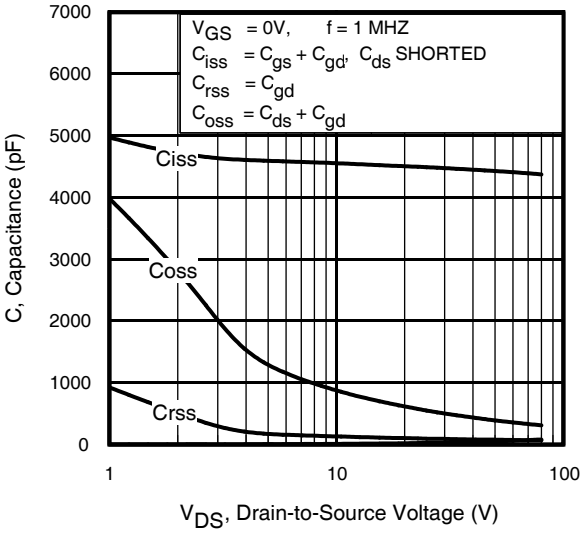


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

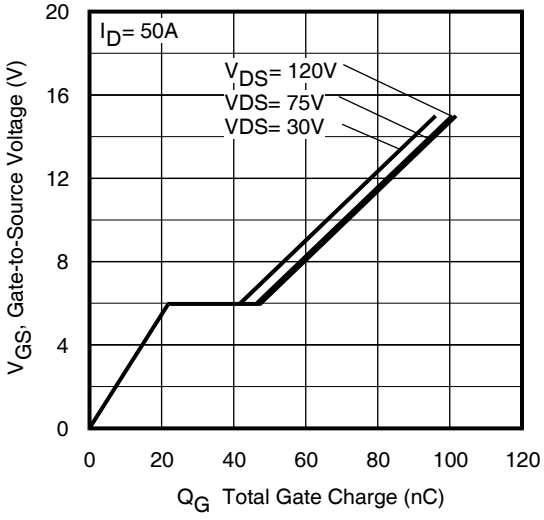


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

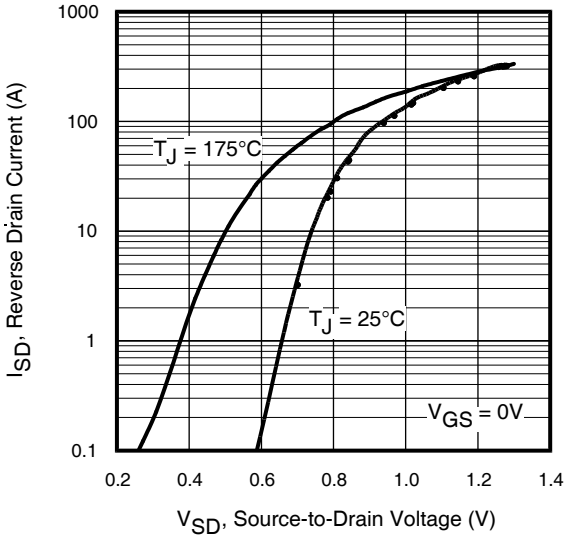


Fig 7. Typical Source-Drain Diode Forward Voltage

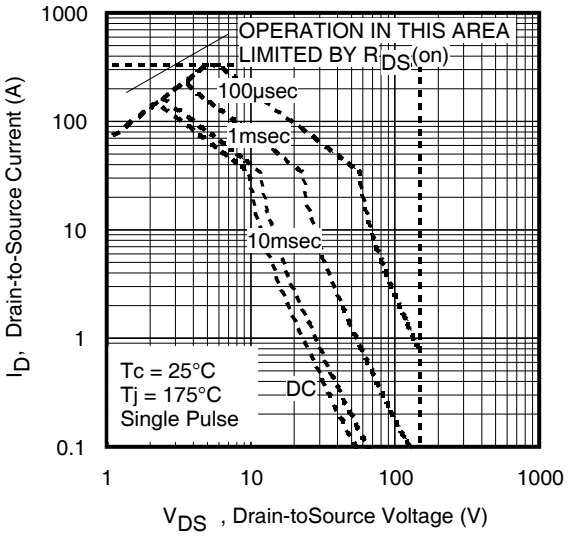


Fig 8. Maximum Safe Operating Area

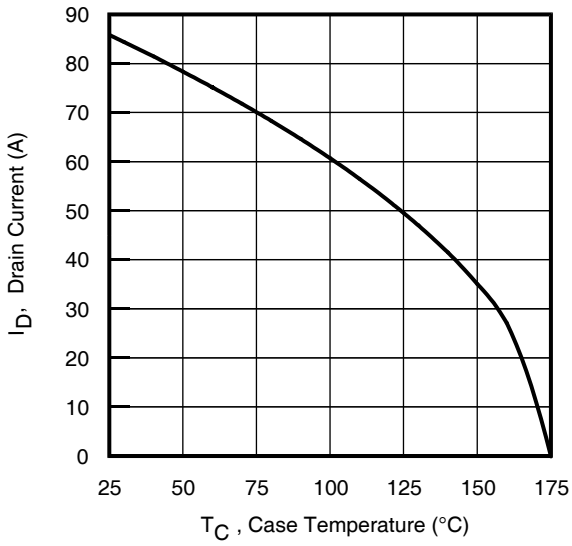


Fig 9. Maximum Drain Current vs. Case Temperature

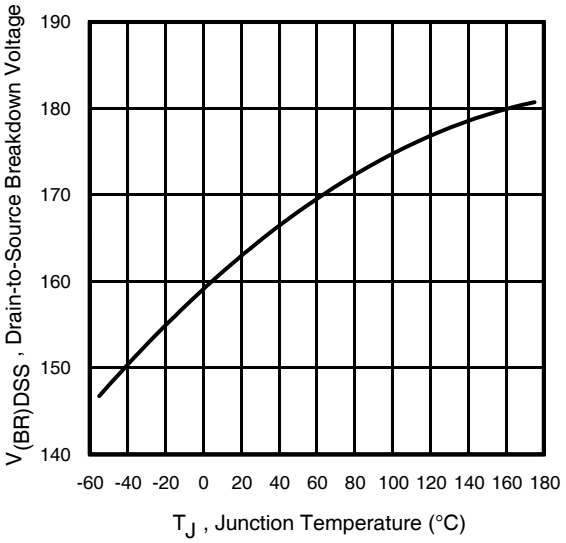


Fig 10. Drain-to–Source Breakdown Voltage

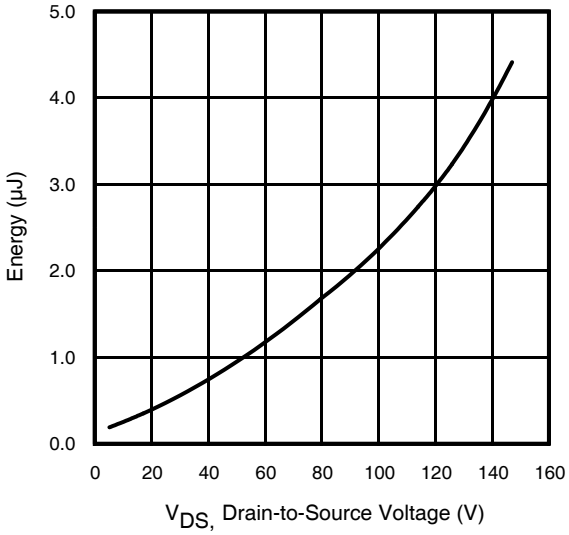


Fig 11. Typical C_{oss} Stored Energy

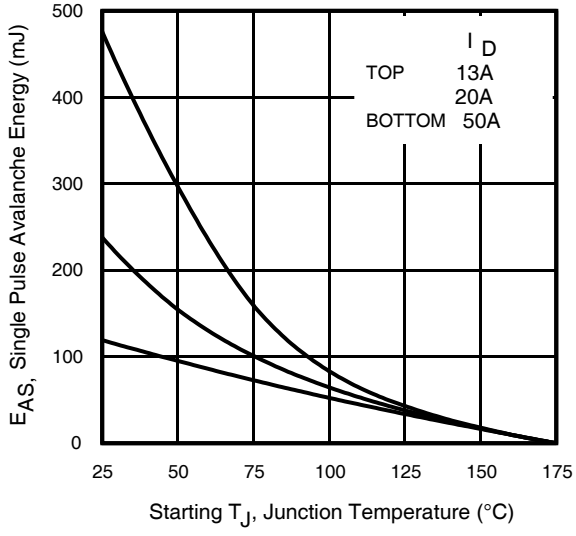


Fig 12. Maximum Avalanche Energy Vs. Drain Current

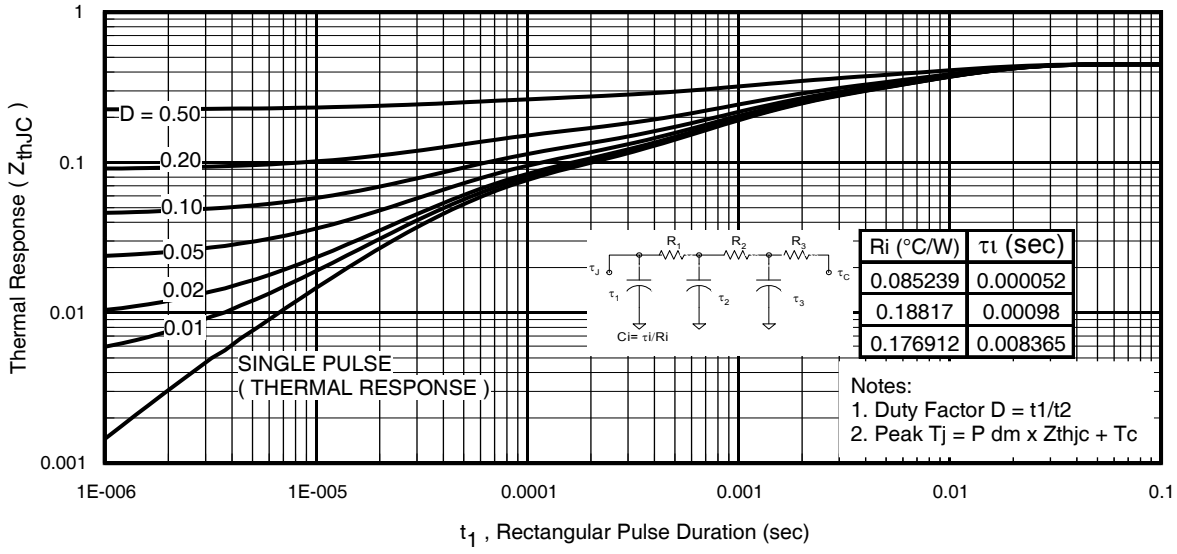


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

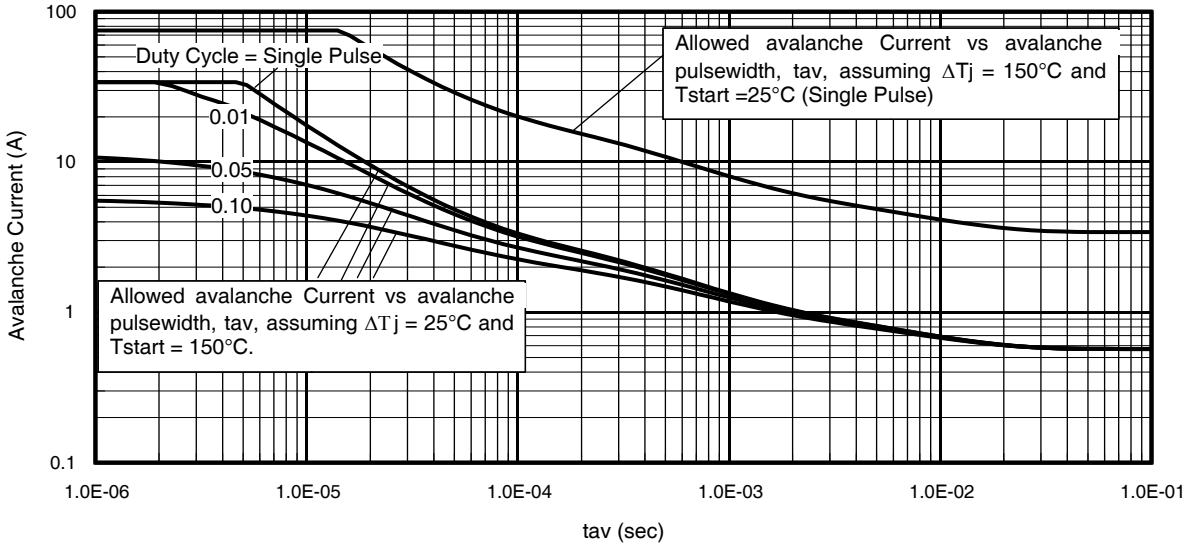
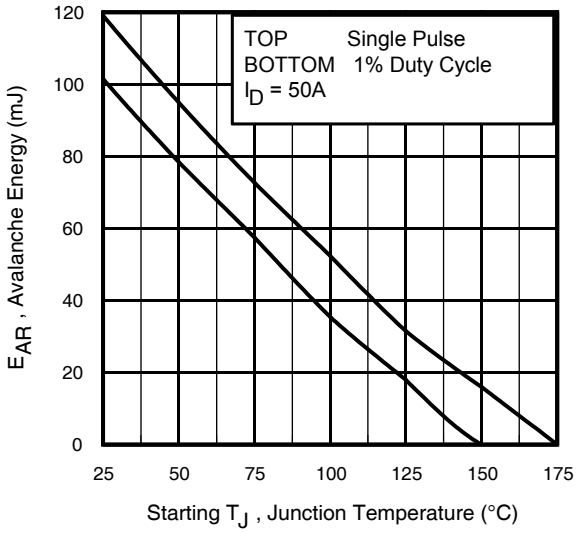


Fig 14. Typical Avalanche Current vs. Pulse width



Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).

   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = tav ·f
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)
   PD (ave) = 1/2 (1.3·BV·I_{av}) = ΔT/ Z_{thJC}
   I_{av} = 2ΔT/ [1.3·BV·Z_{th}]
   $E_{AS\ (AR)}$ = $P_{D\ (ave)}$·t_{av}

Fig 15. Maximum Avalanche Energy vs. Temperature

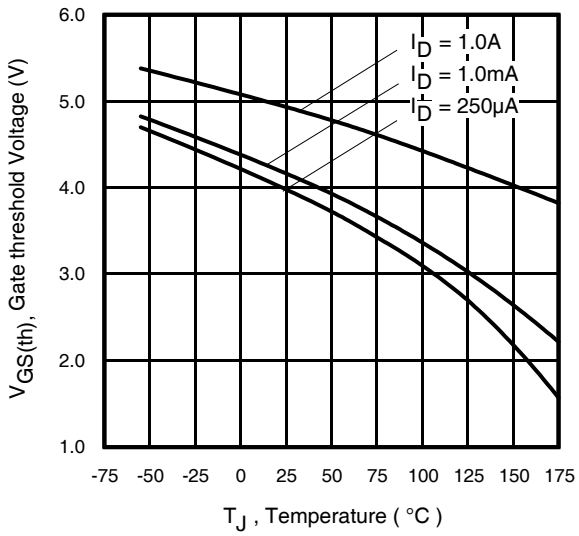


Fig 16. Threshold Voltage vs. Temperature

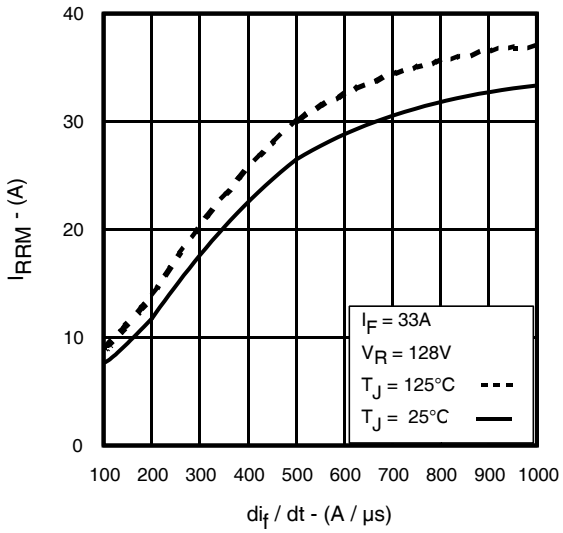


Fig 17. Typical Recovery Current vs. dif/dt

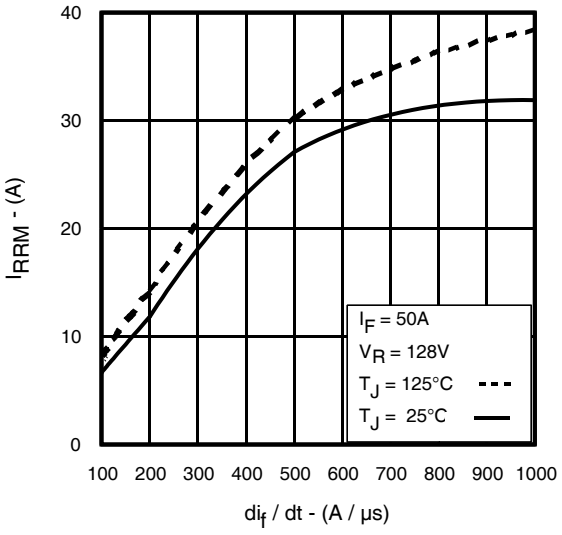


Fig 18. Typical Recovery Current vs. dif/dt

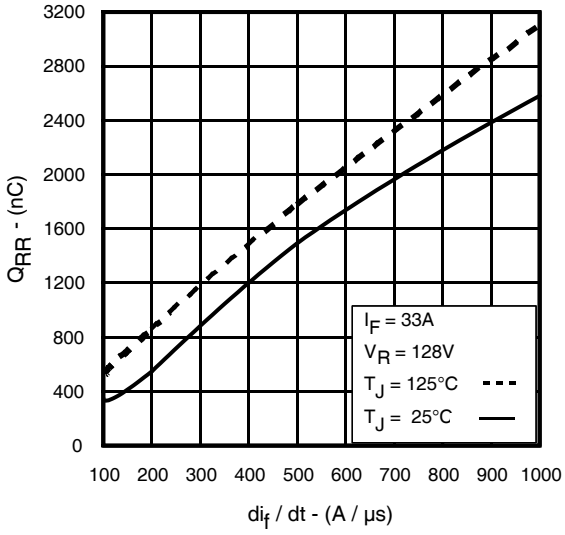


Fig 19. Typical Stored Charge vs. dif/dt

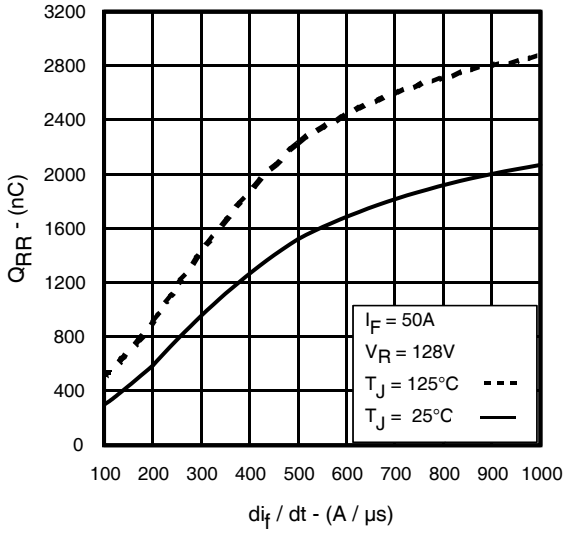


Fig 20. Typical Stored Charge vs. dif/dt

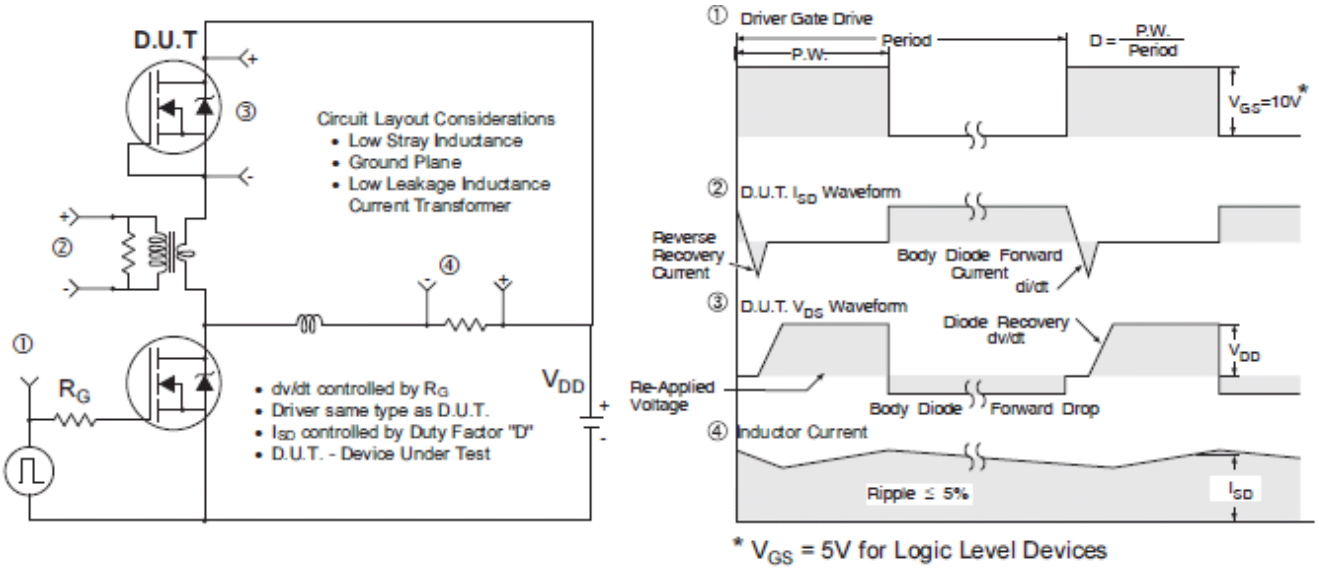


Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

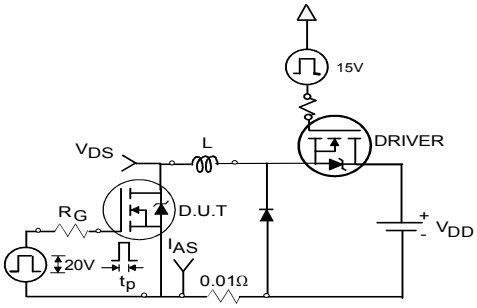


Fig 22a. Unclamped Inductive Test Circuit

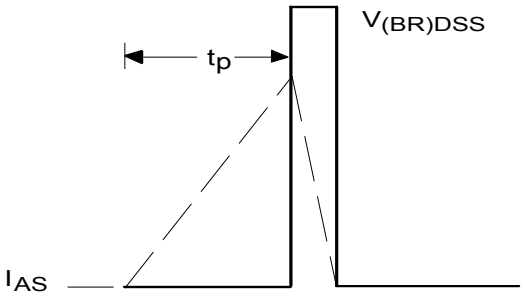


Fig 22b. Unclamped Inductive Waveforms

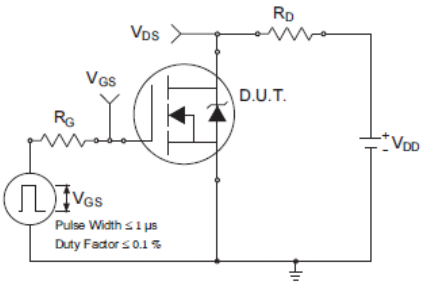


Fig 23a. Switching Time Test Circuit

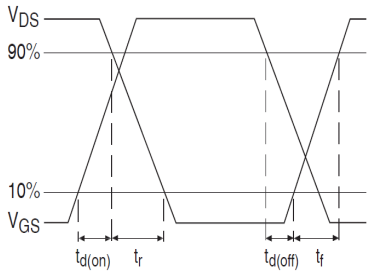


Fig 23b. Switching Time Waveforms

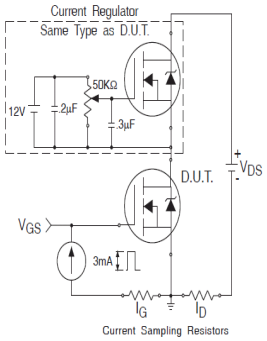


Fig 24a. Gate Charge Test Circuit

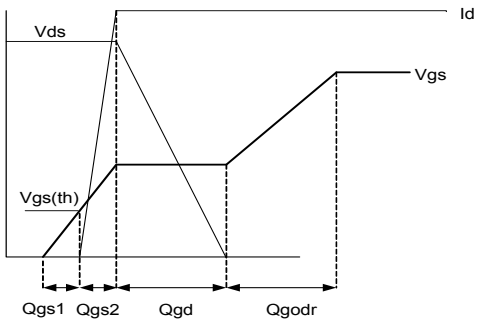
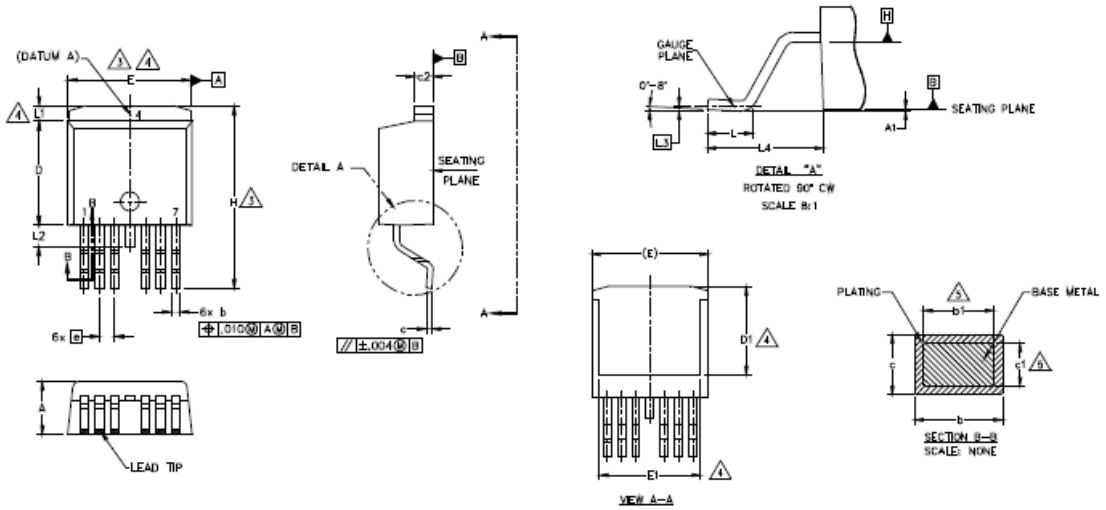


Fig 24b. Gate Charge Waveform

D²Pak-7Pin Package Outline (Dimensions are shown in millimeters (inches))



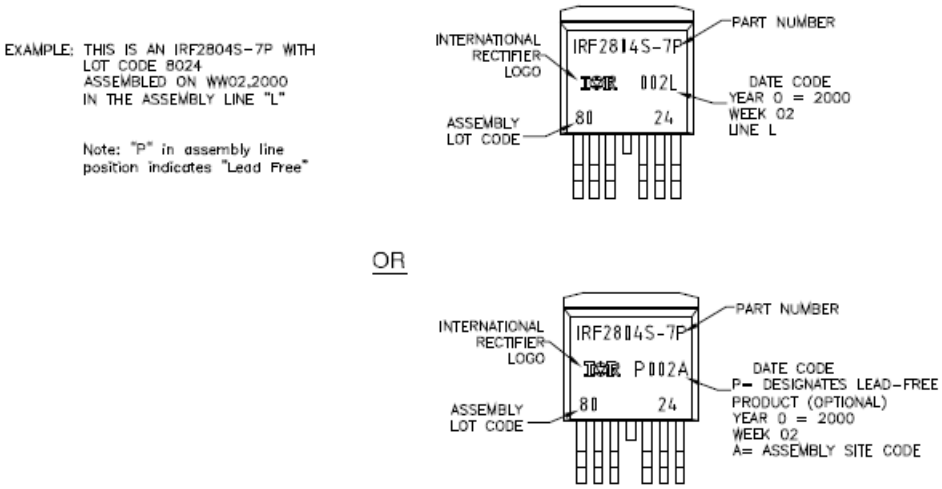
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	–	0.254	–	.010	
b	0.51	0.99	.020	.036	
b1	0.51	0.89	.020	.032	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	–	.270		4
E	9.65	10.67	.380	.420	3,4
E1	6.22	–	.245		4
e	1.27 BSC		.050 BSC		
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	
L1	–	1.68	–	.066	4
L2	–	1.78	–	.070	
L3	0.25 BSC		.010 BSC		
L4	4.78	5.28	.188	.208	

NOTES:

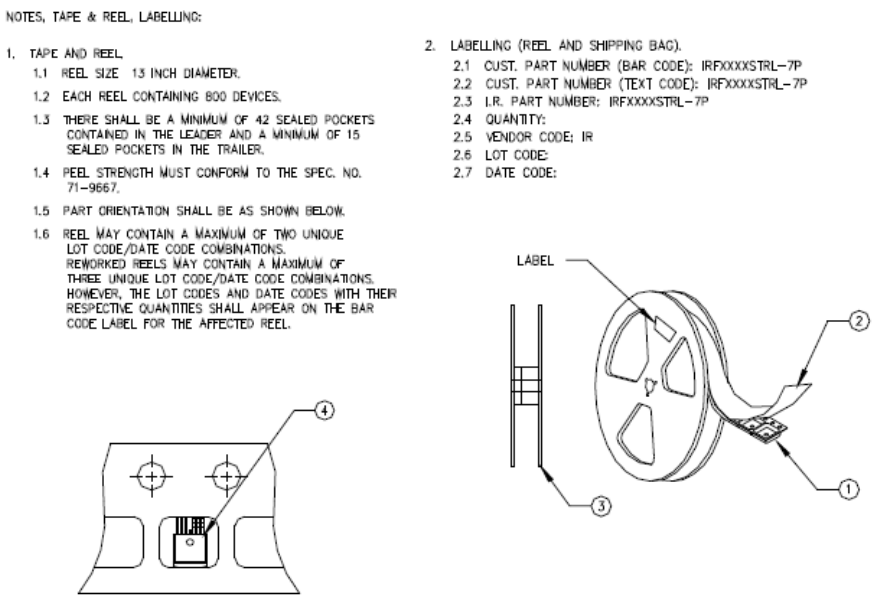
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M–1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

D²Pak-7Pin Part Marking Information



D2Pak-7Pin Tape and Reel



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification Level	Industrial (per JEDEC JESD47F) ††	
Moisture Sensitivity Level	D^2Pak-7Pin	MSL1
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site: http://www.irf.com/product-info/reliability/

†† Applicable version of JEDEC standard at the time of product release.

International
IOR Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA
To contact International Rectifier, please visit http://www.irf.com/whoto-call/

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