

# MUN2135, MMUN2135L, MUN5135, DTA123JE, DTA123JM3, NSBA123JF3

## Digital Transistors (BRT) R1 = 2.2 k $\Omega$ , R2 = 47 k $\Omega$

### PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### MAXIMUM RATINGS (T<sub>A</sub> = 25°C)

| Rating                         | Symbol               | Max | Unit |
|--------------------------------|----------------------|-----|------|
| Collector-Base Voltage         | V <sub>CBO</sub>     | 50  | Vdc  |
| Collector-Emitter Voltage      | V <sub>CEO</sub>     | 50  | Vdc  |
| Collector Current – Continuous | I <sub>C</sub>       | 100 | mAdc |
| Input Forward Voltage          | V <sub>IN(fwd)</sub> | 12  | Vdc  |
| Input Reverse Voltage          | V <sub>IN(rev)</sub> | 5   | Vdc  |

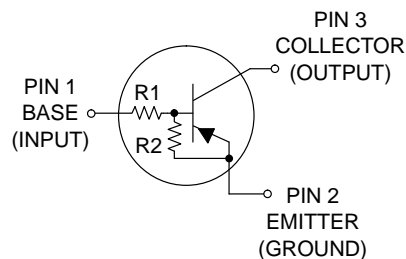
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



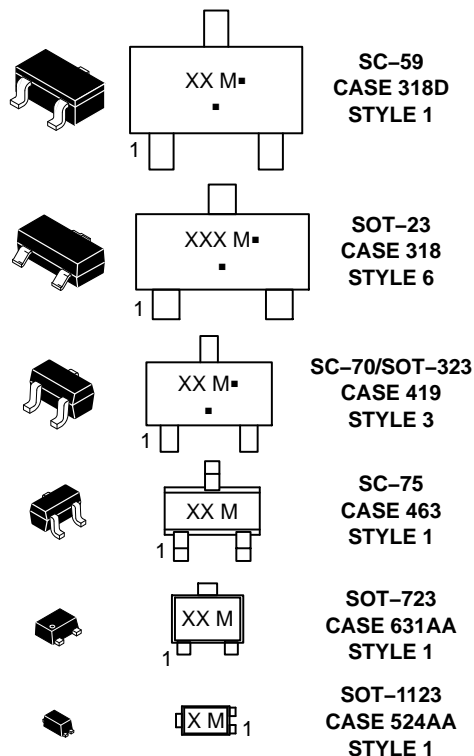
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#### PIN CONNECTIONS



#### MARKING DIAGRAMS



XXX = Specific Device Code  
M = Date Code\*  
■ = Pb-Free Package

(Note: Microdot may be in either location)

\*Date Code orientation may vary depending upon manufacturing location.

#### ORDERING INFORMATION

See detailed ordering, marking, and shipping information in the package dimensions section on page 2 of this data sheet.

# MUN2135, MMUN2135L, MUN5135, DTA123JE, DTA123JM3, NSBA123JF3

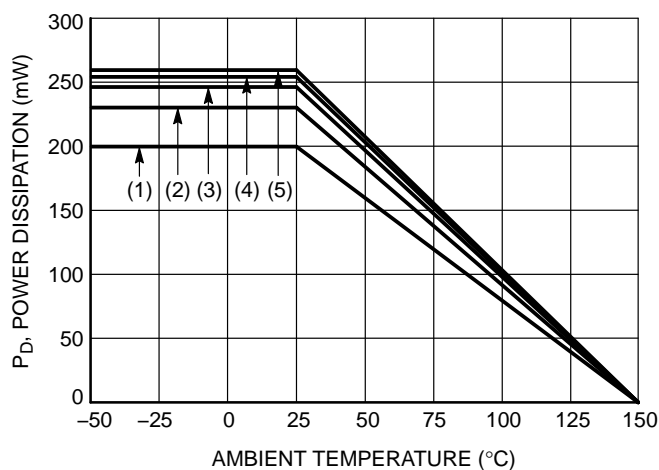
**Table 1. ORDERING INFORMATION**

| Device                            | Part Marking | Package                    | Shipping†          |
|-----------------------------------|--------------|----------------------------|--------------------|
| MUN2135T1G                        | 6R           | SC-59<br>(Pb-Free)         | 3000 / Tape & Reel |
| MMUN2135LT1G,<br>NSVMMUN2135LT1G* | ACA          | SOT-23<br>(Pb-Free)        | 3000 / Tape & Reel |
| MUN5135T1G                        | 6M           | SC-70/SOT-323<br>(Pb-Free) | 3000 / Tape & Reel |
| DTA123JET1G                       | 6M           | SC-75<br>(Pb-Free)         | 3000 / Tape & Reel |
| DTA123JM3T5G,<br>NSVDTA123JM3T5G* | 6M           | SOT-723<br>(Pb-Free)       | 8000 / Tape & Reel |
| NSBA123JF3T5G                     | J (90°)**    | SOT-1123<br>(Pb-Free)      | 8000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.

\*\* (XX°) = Degree rotation in the clockwise direction.



- (1) SC-75 and SC-70/SOT323; Minimum Pad
- (2) SC-59; Minimum Pad
- (3) SOT-23; Minimum Pad
- (4) SOT-1123; 100 mm<sup>2</sup>, 1 oz. copper trace
- (5) SOT-723; Minimum Pad

**Figure 1. Derating Curve**

# MUN2135, MMUN2135L, MUN5135, DTA123JE, DTA123JM3, NSBA123JF3

**Table 2. THERMAL CHARACTERISTICS**

| Characteristic  | Symbol  | Max                      | Unit                       |
|---|---|--------------------------|----------------------------|
| <b>THERMAL CHARACTERISTICS (SC-59) (MUN2135)</b>  |   |                          |                            |
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$<br>(Note 1)<br>(Note 2)<br>(Note 1)<br>(Note 2) | 230<br>338<br>1.8<br>2.7 | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance,<br>Junction to Ambient  | $R_{\theta JA}$<br>(Note 1)<br>(Note 2)               | 540<br>370               | $^\circ\text{C/W}$         |
| Thermal Resistance,<br>Junction to Lead   | $R_{\theta JL}$<br>(Note 1)<br>(Note 2)               | 264<br>287               | $^\circ\text{C/W}$         |
| Junction and Storage Temperature Range  | $T_J, T_{stg}$  | -55 to +150              | $^\circ\text{C}$           |
| <b>THERMAL CHARACTERISTICS (SOT-23) (MMUN2135L)</b>                                     |   |                          |                            |
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$<br>(Note 1)<br>(Note 2)<br>(Note 1)<br>(Note 2) | 246<br>400<br>2.0<br>3.2 | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance,<br>Junction to Ambient  | $R_{\theta JA}$<br>(Note 1)<br>(Note 2)               | 508<br>311               | $^\circ\text{C/W}$         |
| Thermal Resistance,<br>Junction to Lead   | $R_{\theta JL}$<br>(Note 1)<br>(Note 2)               | 174<br>208               | $^\circ\text{C/W}$         |
| Junction and Storage Temperature Range  | $T_J, T_{stg}$  | -55 to +150              | $^\circ\text{C}$           |
| <b>THERMAL CHARACTERISTICS (SC-70/SOT-323) (MUN5135)</b>                                |   |                          |                            |
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$<br>(Note 1)<br>(Note 2)<br>(Note 1)<br>(Note 2) | 202<br>310<br>1.6<br>2.5 | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance,<br>Junction to Ambient  | $R_{\theta JA}$<br>(Note 1)<br>(Note 2)               | 618<br>403               | $^\circ\text{C/W}$         |
| Thermal Resistance,<br>Junction to Lead   | $R_{\theta JL}$<br>(Note 1)<br>(Note 2)               | 280<br>332               | $^\circ\text{C/W}$         |
| Junction and Storage Temperature Range  | $T_J, T_{stg}$  | -55 to +150              | $^\circ\text{C}$           |
| <b>THERMAL CHARACTERISTICS (SC-75) (DTA123JE)</b>                                       |   |                          |                            |
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$<br>(Note 1)<br>(Note 2)<br>(Note 1)<br>(Note 2) | 200<br>300<br>1.6<br>2.4 | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance,<br>Junction to Ambient  | $R_{\theta JA}$<br>(Note 1)<br>(Note 2)               | 600<br>400               | $^\circ\text{C/W}$         |
| Junction and Storage Temperature Range  | $T_J, T_{stg}$  | -55 to +150              | $^\circ\text{C}$           |
| <b>THERMAL CHARACTERISTICS (SOT-723) (DTA123JM3)</b>                                    |   |                          |                            |
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$<br>(Note 1)<br>(Note 2)<br>(Note 1)<br>(Note 2) | 260<br>600<br>2.0<br>4.8 | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance,<br>Junction to Ambient  | $R_{\theta JA}$<br>(Note 1)<br>(Note 2)               | 480<br>205               | $^\circ\text{C/W}$         |
| Junction and Storage Temperature Range  | $T_J, T_{stg}$  | -55 to +150              | $^\circ\text{C}$           |

1. FR-4 @ Minimum Pad.
2. FR-4 @ 1.0 x 1.0 Inch Pad.
3. FR-4 @ 100 mm<sup>2</sup>, 1 oz. copper traces, still air.
4. FR-4 @ 500 mm<sup>2</sup>, 1 oz. copper traces, still air.

**Table 2. THERMAL CHARACTERISTICS**

| Characteristic  | Symbol  | Max                      | Unit                       |
|---|---|--------------------------|----------------------------|
| <b>THERMAL CHARACTERISTICS (SOT-1123) (NSBA123JF3)</b>                                  |   |                          |                            |
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$<br>(Note 3)<br>(Note 4)<br>(Note 3)<br>(Note 4) | 254<br>297<br>2.0<br>2.4 | mW<br>mW/ $^\circ\text{C}$ |
| Thermal Resistance,<br>Junction to Ambient  | $R_{\theta JA}$<br>(Note 3)<br>(Note 4)               | 493<br>421               | $^\circ\text{C/W}$         |
| Thermal Resistance, Junction to Lead  | $R_{\theta JL}$<br>(Note 3)                           | 193                      | $^\circ\text{C/W}$         |
| Junction and Storage Temperature Range  | $T_J, T_{stg}$  | -55 to +150              | $^\circ\text{C}$           |

- FR-4 @ Minimum Pad.
- FR-4 @ 1.0 x 1.0 Inch Pad.
- FR-4 @ 100 mm<sup>2</sup>, 1 oz. copper traces, still air.
- FR-4 @ 500 mm<sup>2</sup>, 1 oz. copper traces, still air.

**Table 3. ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

| Characteristic  | Symbol        | Min   | Typ   | Max   | Unit       |
|---|---------------|-------|-------|-------|------------|
| <b>OFF CHARACTERISTICS</b>  |               |       |       |       |            |
| Collector-Base Cutoff Current<br>( $V_{CB} = 50\text{ V}, I_E = 0$ )                              | $I_{CBO}$     | –     | –     | 100   | nAdc       |
| Collector-Emitter Cutoff Current<br>( $V_{CE} = 50\text{ V}, I_B = 0$ )                           | $I_{CEO}$     | –     | –     | 500   | nAdc       |
| Emitter-Base Cutoff Current<br>( $V_{EB} = 6.0\text{ V}, I_C = 0$ )                               | $I_{EBO}$     | –     | –     | 0.2   | mAdc       |
| Collector-Base Breakdown Voltage<br>( $I_C = 10\text{ }\mu\text{A}, I_E = 0$ )                    | $V_{(BR)CBO}$ | 50    | –     | –     | Vdc        |
| Collector-Emitter Breakdown Voltage (Note 5)<br>( $I_C = 2.0\text{ mA}, I_B = 0$ )                | $V_{(BR)CEO}$ | 50    | –     | –     | Vdc        |
| <b>ON CHARACTERISTICS</b>   |               |       |       |       |            |
| DC Current Gain (Note 5)<br>( $I_C = 5.0\text{ mA}, V_{CE} = 10\text{ V}$ )                       | $h_{FE}$      | 80    | 140   | –     |            |
| Collector – Emitter Saturation Voltage (Note 5)<br>( $I_C = 10\text{ mA}, I_B = 0.3\text{ mA}$ )  | $V_{CE(sat)}$ | –     | –     | 0.25  | Vdc        |
| Input Voltage (off)<br>( $V_{CE} = 5.0\text{ V}, I_C = 100\text{ }\mu\text{A}$ )                  | $V_{i(off)}$  | –     | 0.6   | 0.5   | Vdc        |
| Input Voltage (on)<br>( $V_{CE} = 0.3\text{ V}, I_C = 5.0\text{ mA}$ )                            | $V_{i(on)}$   | 1.1   | 0.8   | –     | Vdc        |
| Output Voltage (on)<br>( $V_{CC} = 5.0\text{ V}, V_B = 2.5\text{ V}, R_L = 1.0\text{ k}\Omega$ )  | $V_{OL}$      | –     | –     | 0.2   | Vdc        |
| Output Voltage (off)<br>( $V_{CC} = 5.0\text{ V}, V_B = 0.5\text{ V}, R_L = 1.0\text{ k}\Omega$ ) | $V_{OH}$      | 4.9   | –     | –     | Vdc        |
| Input Resistor  | $R_1$         | 1.5   | 2.2   | 2.9   | k $\Omega$ |
| Resistor Ratio  | $R_1/R_2$     | 0.038 | 0.047 | 0.056 |            |

- Pulsed Condition: Pulse Width = 300 msec, Duty Cycle  $\leq 2\%$ .

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**TYPICAL CHARACTERISTICS**  
MUN2135, MMUN2135L, MUN5135, DTA123JE, DTA123JM3

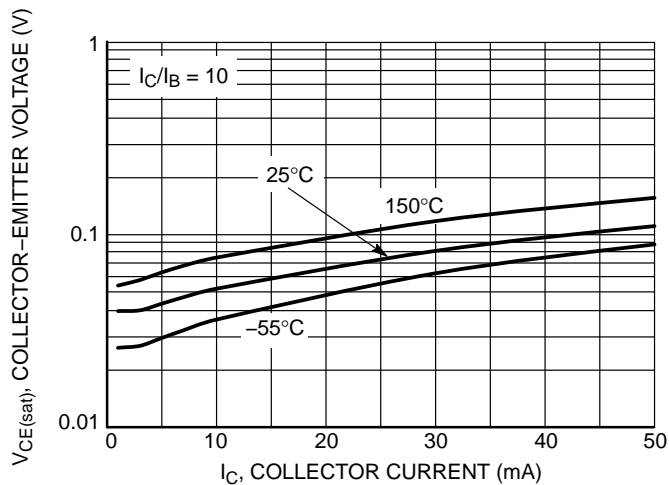


Figure 2.  $V_{CE(sat)}$  vs.  $I_C$

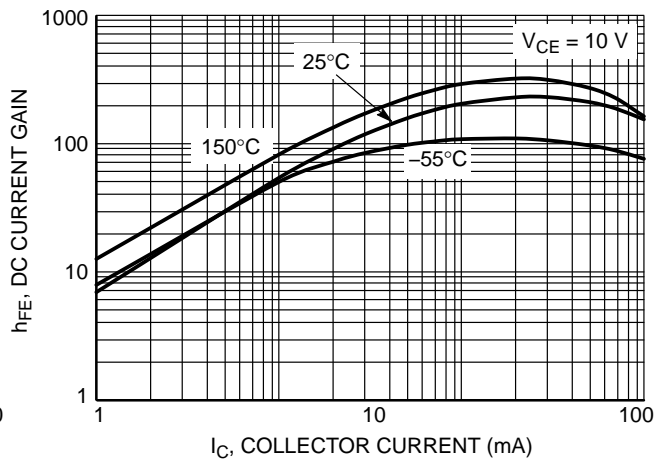


Figure 3. DC Current Gain

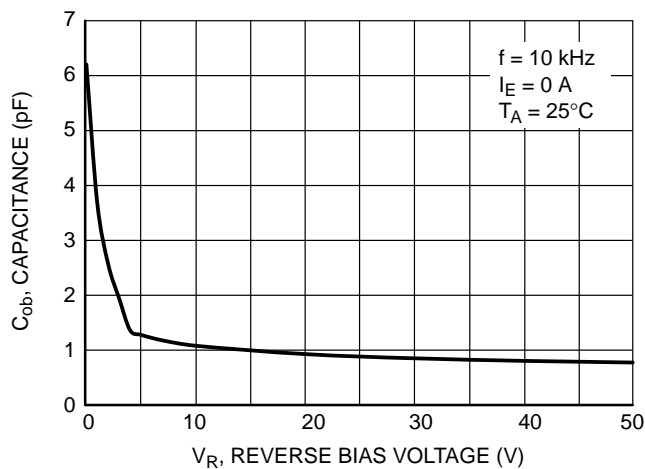


Figure 4. Output Capacitance

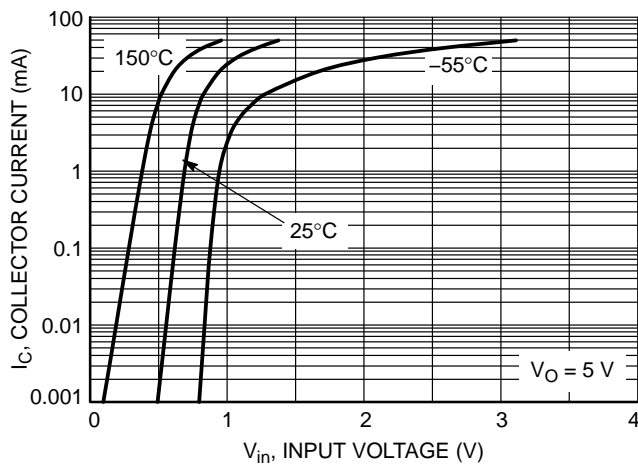


Figure 5. Output Current vs. Input Voltage

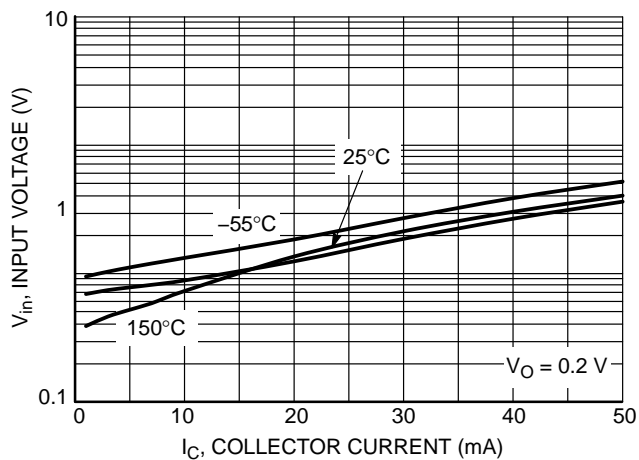


Figure 6. Input Voltage vs. Output Current

TYPICAL CHARACTERISTICS  
NSBA123JF3

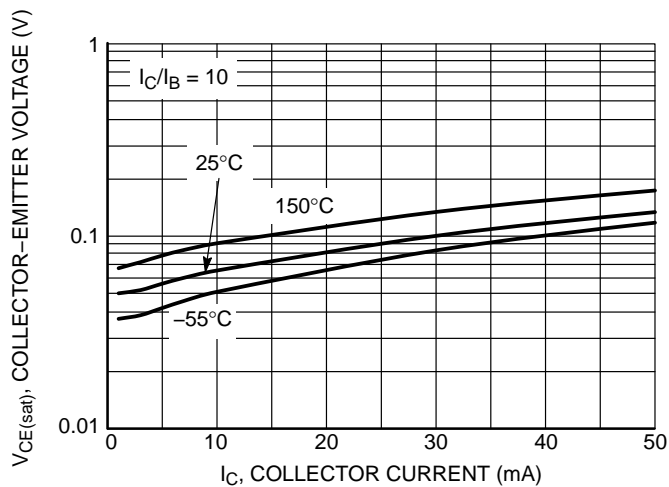


Figure 7.  $V_{CE(sat)}$  vs.  $I_C$

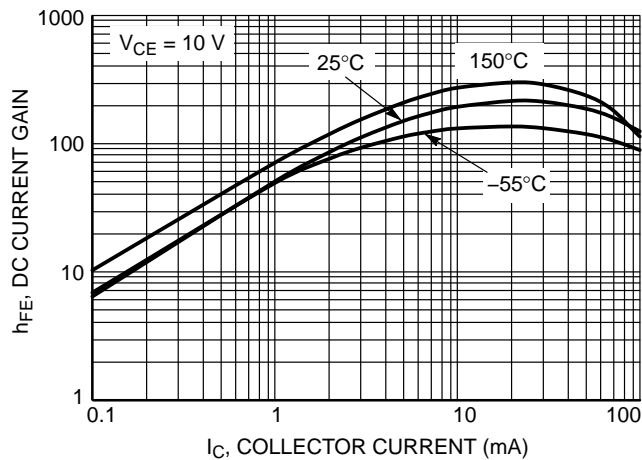


Figure 8. DC Current Gain

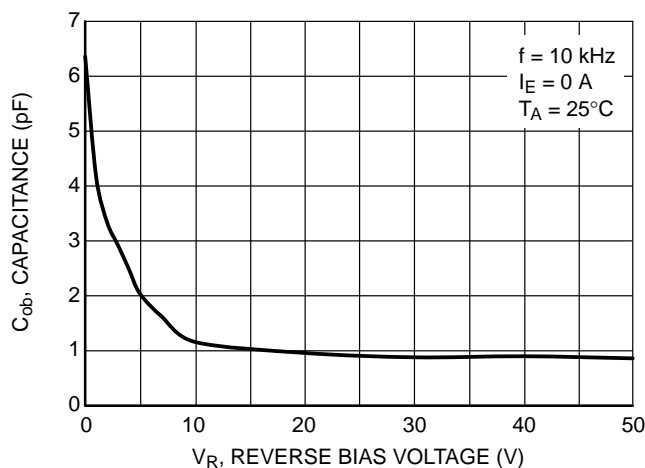


Figure 9. Output Capacitance

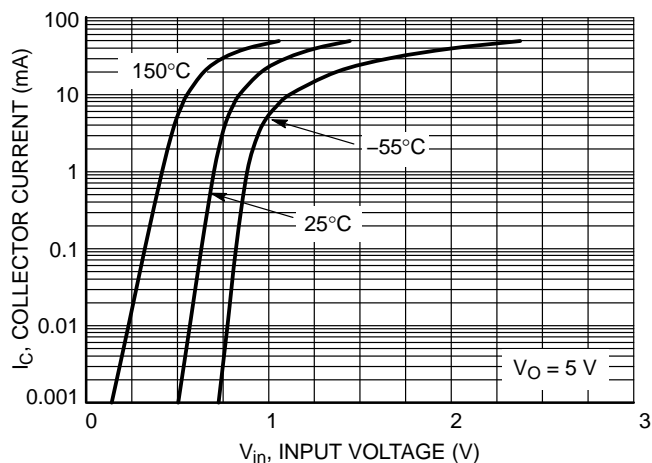


Figure 10. Output Current vs. Input Voltage

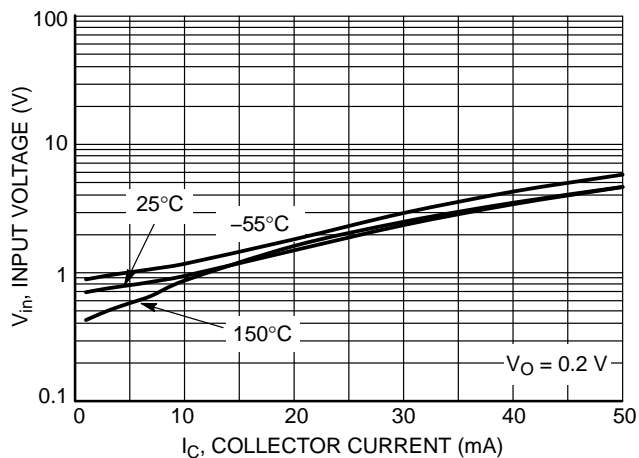


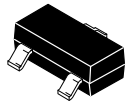
Figure 11. Input Voltage vs. Output Current

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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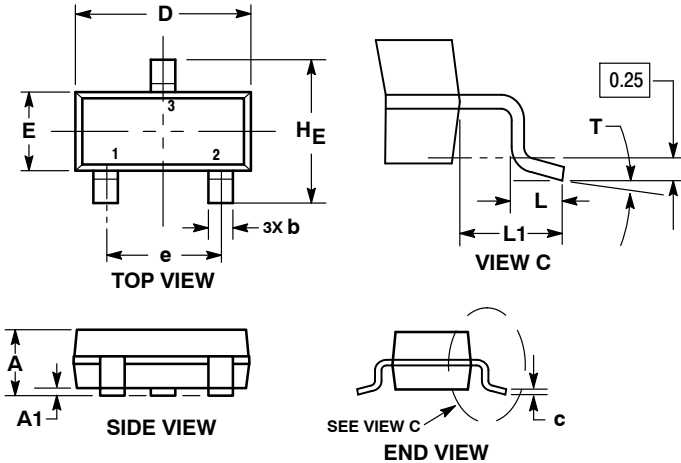
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### SOT-23 (TO-236) CASE 318-08 ISSUE AS

DATE 30 JAN 2018

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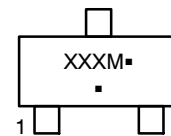


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM | MILLIMETERS |      |      | INCHES |       |       |
|-----|-------------|------|------|--------|-------|-------|
|     | MIN         | NOM  | MAX  | MIN    | NOM   | MAX   |
| A   | 0.89        | 1.00 | 1.11 | 0.035  | 0.039 | 0.044 |
| A1  | 0.01        | 0.06 | 0.10 | 0.000  | 0.002 | 0.004 |
| b   | 0.37        | 0.44 | 0.50 | 0.015  | 0.017 | 0.020 |
| c   | 0.08        | 0.14 | 0.20 | 0.003  | 0.006 | 0.008 |
| D   | 2.80        | 2.90 | 3.04 | 0.110  | 0.114 | 0.120 |
| E   | 1.20        | 1.30 | 1.40 | 0.047  | 0.051 | 0.055 |
| e   | 1.78        | 1.90 | 2.04 | 0.070  | 0.075 | 0.080 |
| L   | 0.30        | 0.43 | 0.55 | 0.012  | 0.017 | 0.022 |
| L1  | 0.35        | 0.54 | 0.69 | 0.014  | 0.021 | 0.027 |
| HE  | 2.10        | 2.40 | 2.64 | 0.083  | 0.094 | 0.104 |
| T   | 0°          | ---  | 10°  | 0°     | ---   | 10°   |

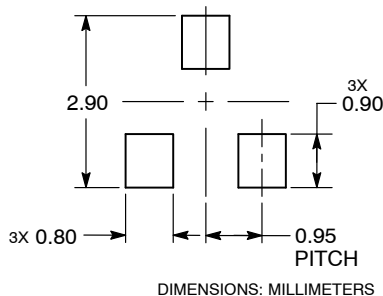
#### GENERIC MARKING DIAGRAM\*



XXX = Specific Device Code  
M = Date Code  
■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

#### RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

STYLE 1 THRU 5:  
CANCELLED

STYLE 6:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

STYLE 7:  
PIN 1. EMITTER  
2. BASE  
3. COLLECTOR

STYLE 8:  
PIN 1. ANODE  
2. NO CONNECTION  
3. CATHODE

STYLE 9:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 10:  
PIN 1. DRAIN  
2. SOURCE  
3. GATE

STYLE 11:  
PIN 1. ANODE  
2. CATHODE  
3. CATHODE-ANODE

STYLE 12:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE

STYLE 13:  
PIN 1. SOURCE  
2. DRAIN  
3. GATE

STYLE 14:  
PIN 1. CATHODE  
2. GATE  
3. ANODE

STYLE 15:  
PIN 1. GATE  
2. CATHODE  
3. ANODE

STYLE 16:  
PIN 1. ANODE  
2. CATHODE  
3. CATHODE

STYLE 17:  
PIN 1. NO CONNECTION  
2. ANODE  
3. CATHODE

STYLE 18:  
PIN 1. NO CONNECTION  
2. CATHODE  
3. ANODE

STYLE 19:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE-ANODE

STYLE 20:  
PIN 1. CATHODE  
2. ANODE  
3. GATE

STYLE 21:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

STYLE 22:  
PIN 1. RETURN  
2. OUTPUT  
3. INPUT

STYLE 23:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 24:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE


STYLE 25:  
PIN 1. ANODE  
2. CATHODE  
3. GATE

STYLE 26:  
PIN 1. CATHODE  
2. ANODE  
3. NO CONNECTION

STYLE 27:  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE

STYLE 28:  
PIN 1. ANODE  
2. ANODE  
3. ANODE

|                  |                 |  |
|------------------|-----------------|--|
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| DESCRIPTION:     | SOT-23 (TO-236) | PAGE 1 OF 1  |

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

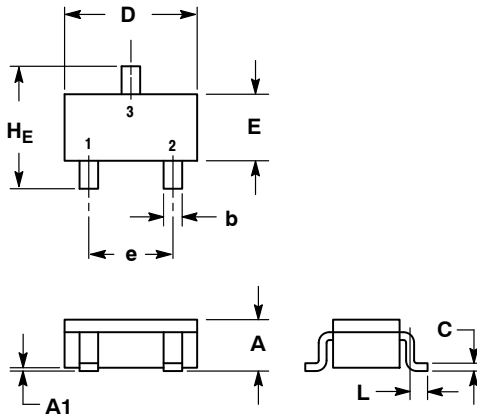
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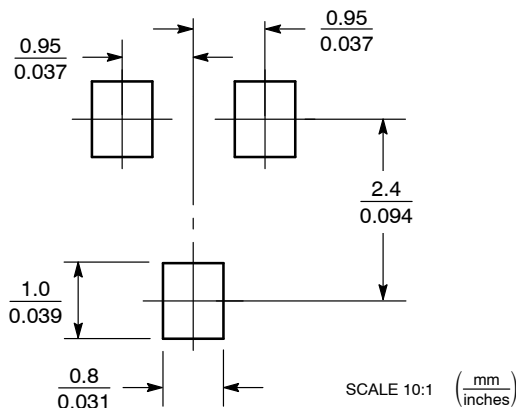
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SC-59  
CASE 318D-04  
ISSUE H

DATE 28 JUN 2012



### SOLDERING FOOTPRINT\*

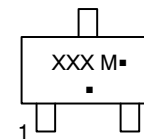


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.

| DIM | MILLIMETERS |      |      | INCHES |       |       |
|-----|-------------|------|------|--------|-------|-------|
|     | MIN         | NOM  | MAX  | MIN    | NOM   | MAX   |
| A   | 1.00        | 1.15 | 1.30 | 0.039  | 0.045 | 0.051 |
| A1  | 0.01        | 0.06 | 0.10 | 0.001  | 0.002 | 0.004 |
| b   | 0.35        | 0.43 | 0.50 | 0.014  | 0.017 | 0.020 |
| c   | 0.09        | 0.14 | 0.18 | 0.003  | 0.005 | 0.007 |
| D   | 2.70        | 2.90 | 3.10 | 0.106  | 0.114 | 0.122 |
| E   | 1.30        | 1.50 | 1.70 | 0.051  | 0.059 | 0.067 |
| e   | 1.70        | 1.90 | 2.10 | 0.067  | 0.075 | 0.083 |
| L   | 0.20        | 0.40 | 0.60 | 0.008  | 0.016 | 0.024 |
| H_E | 2.50        | 2.80 | 3.00 | 0.099  | 0.110 | 0.118 |

### GENERIC MARKING DIAGRAM



XXX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package\*

(\*Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

STYLE 1:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

STYLE 2:  
PIN 1. ANODE  
2. N.C.  
3. CATHODE

STYLE 3:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 4:  
PIN 1. CATHODE  
2. N.C.  
3. ANODE

STYLE 5:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE

STYLE 6:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE/CATHODE

DOCUMENT NUMBER: 98ASB42664B

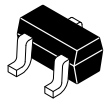
DESCRIPTION: SC-59

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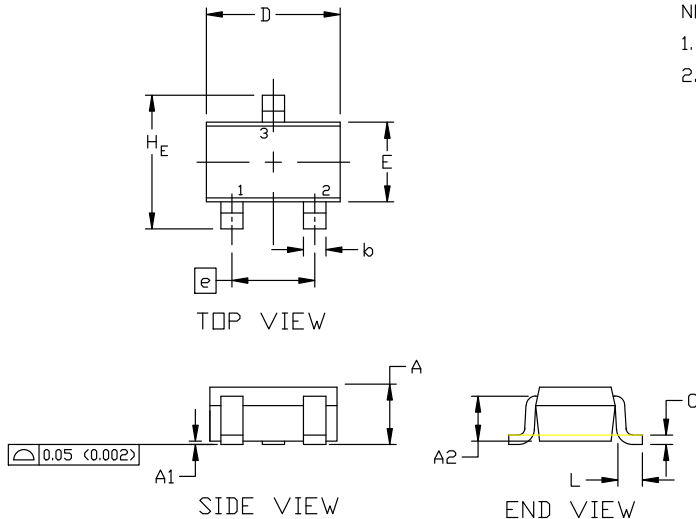
SCALE 4:1

### SC-70 (SOT-323)

#### CASE 419

#### ISSUE R

DATE 11 OCT 2022

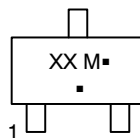


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

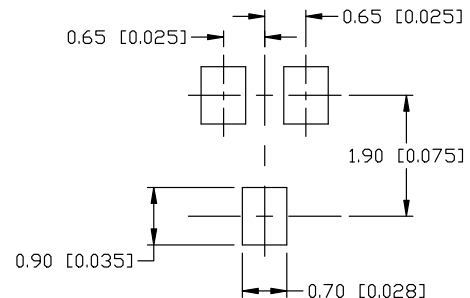
| DIM            | MILLIMETERS |      |      | INCHES    |       |       |
|----------------|-------------|------|------|-----------|-------|-------|
|                | MIN.        | NOM. | MAX. | MIN.      | NOM.  | MAX.  |
| A              | 0.80        | 0.90 | 1.00 | 0.032     | 0.035 | 0.040 |
| A1             | 0.00        | 0.05 | 0.10 | 0.000     | 0.002 | 0.004 |
| A2             | 0.70 REF    |      |      | 0.028 BSC |       |       |
| b              | 0.30        | 0.35 | 0.40 | 0.012     | 0.014 | 0.016 |
| c              | 0.10        | 0.18 | 0.25 | 0.004     | 0.007 | 0.010 |
| D              | 1.80        | 2.00 | 2.20 | 0.071     | 0.080 | 0.087 |
| E              | 1.15        | 1.24 | 1.35 | 0.045     | 0.049 | 0.053 |
| e              | 1.20        | 1.30 | 1.40 | 0.047     | 0.051 | 0.055 |
| e1             | 0.65 BSC    |      |      | 0.026 BSC |       |       |
| L              | 0.20        | 0.38 | 0.56 | 0.008     | 0.015 | 0.022 |
| H <sub>E</sub> | 2.00        | 2.10 | 2.40 | 0.079     | 0.083 | 0.095 |

#### GENERIC MARKING DIAGRAM



XX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### SOLDERING FOOTPRINT

STYLE 1:  
CANCELLED

STYLE 2:  
PIN 1. ANODE  
2. N.C.  
3. CATHODE

STYLE 3:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

STYLE 4:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE

STYLE 5:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 6:  
PIN 1. EMITTER  
2. BASE  
3. COLLECTOR

STYLE 7:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

STYLE 8:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

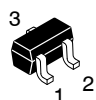
STYLE 9:  
PIN 1. ANODE  
2. CATHODE  
3. CATHODE-ANODE

STYLE 10:  
PIN 1. CATHODE  
2. ANODE  
3. ANODE-CATHODE

STYLE 11:  
PIN 1. CATHODE  
2. CATHODE  
3. CATHODE

|                  |                 |   |
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| DESCRIPTION:     | SC-70 (SOT-323) | PAGE 1 OF 1   |

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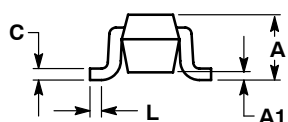
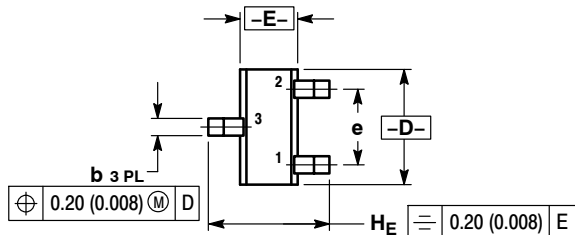
SCALE 4:1

### SC-75/SOT-416

#### CASE 463-01

#### ISSUE G

DATE 07 AUG 2015



STYLE 1:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

STYLE 2:  
PIN 1. ANODE  
2. N/C  
3. CATHODE

STYLE 3:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

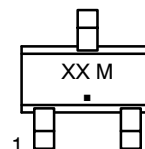
STYLE 4:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE

STYLE 5:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.

| DIM            | MILLIMETERS |      |      | INCHES   |       |       |
|----------------|-------------|------|------|----------|-------|-------|
|                | MIN         | NOM  | MAX  | MIN      | NOM   | MAX   |
| A              | 0.70        | 0.80 | 0.90 | 0.027    | 0.031 | 0.035 |
| A1             | 0.00        | 0.05 | 0.10 | 0.000    | 0.002 | 0.004 |
| b              | 0.15        | 0.20 | 0.30 | 0.006    | 0.008 | 0.012 |
| C              | 0.10        | 0.15 | 0.25 | 0.004    | 0.006 | 0.010 |
| D              | 1.55        | 1.60 | 1.65 | 0.061    | 0.063 | 0.065 |
| E              | 0.70        | 0.80 | 0.90 | 0.027    | 0.031 | 0.035 |
| e              | 1.00 BSC    |      |      | 0.04 BSC |       |       |
| L              | 0.10        | 0.15 | 0.20 | 0.004    | 0.006 | 0.008 |
| H <sub>E</sub> | 1.50        | 1.60 | 1.70 | 0.060    | 0.063 | 0.067 |

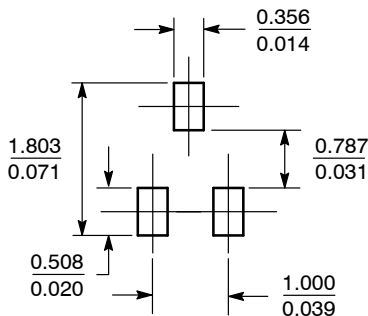
### GENERIC MARKING DIAGRAM\*



XX = Specific Device Code  
M = Date Code  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

### SOLDERING FOOTPRINT\*



SCALE 10:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

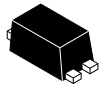
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|------------------|---------------|--|
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| DESCRIPTION:     | SC-75/SOT-416 | PAGE 1 OF 1  |

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

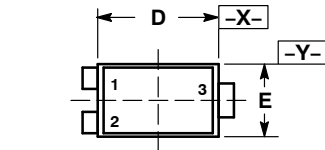
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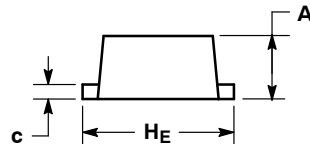
SCALE 8:1

**SOT-1123**  
**CASE 524AA**  
**ISSUE C**

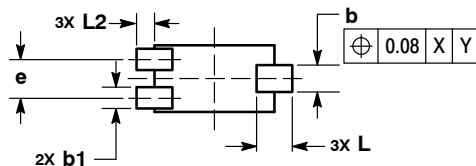
DATE 29 NOV 2011



**TOP VIEW**

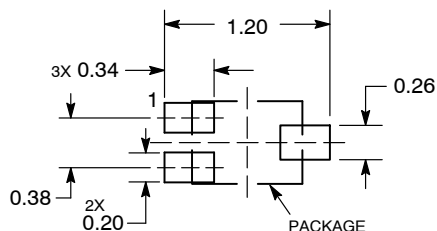


**SIDE VIEW**



**BOTTOM VIEW**

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

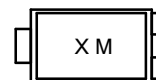
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

| DIM            | MILLIMETERS |      |
|----------------|-------------|------|
|                | MIN         | MAX  |
| A              | 0.34        | 0.40 |
| b              | 0.15        | 0.28 |
| b1             | 0.10        | 0.20 |
| c              | 0.07        | 0.17 |
| D              | 0.75        | 0.85 |
| E              | 0.55        | 0.65 |
| e              | 0.35        | 0.40 |
| H <sub>E</sub> | 0.95        | 1.05 |
| L              | 0.185       | REF  |
| L2             | 0.05        | 0.15 |

### GENERIC MARKING DIAGRAM\*



X = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "▪", may or may not be present.

#### STYLE 1:

PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

#### STYLE 2:

PIN 1. ANODE  
2. N/C  
3. CATHODE

#### STYLE 3:

PIN 1. ANODE  
2. ANODE  
3. CATHODE

#### STYLE 4:

PIN 1. CATHODE  
2. CATHODE  
3. ANODE

#### STYLE 5:

PIN 1. GATE  
2. SOURCE  
3. DRAIN

|                         |  |   |
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| <b>DESCRIPTION:</b>     | <b>SOT-1123, 3-LEAD, 1.0X0.6X0.37, 0.35P</b> | <b>PAGE 1 OF 1</b>  |

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

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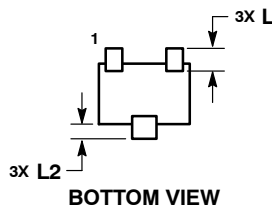
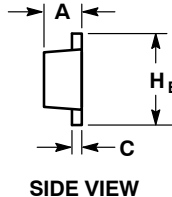
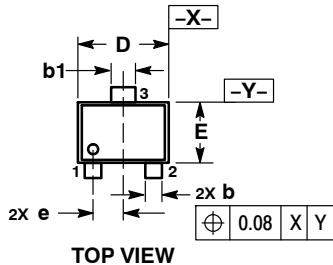
ON



SCALE 4:1

## SOT-723 CASE 631AA-01 ISSUE D

DATE 10 AUG 2009



STYLE 1:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR

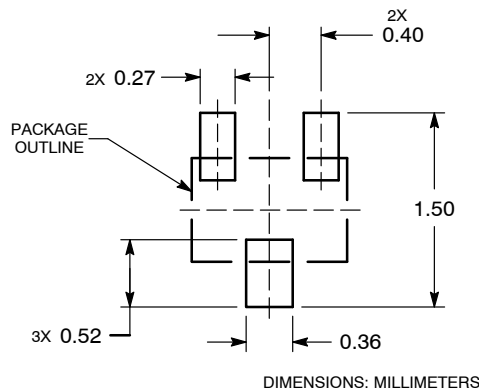
STYLE 2:  
PIN 1. ANODE  
2. N/C  
3. CATHODE

STYLE 3:  
PIN 1. ANODE  
2. ANODE  
3. CATHODE

STYLE 4:  
PIN 1. CATHODE  
2. CATHODE  
3. ANODE

STYLE 5:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN

### RECOMMENDED SOLDERING FOOTPRINT\*



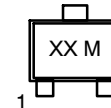
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

| MILLIMETERS |          |      |      |
|-------------|----------|------|------|
| DIM         | MIN      | NOM  | MAX  |
| A           | 0.45     | 0.50 | 0.55 |
| b           | 0.15     | 0.21 | 0.27 |
| b1          | 0.25     | 0.31 | 0.37 |
| C           | 0.07     | 0.12 | 0.17 |
| D           | 1.15     | 1.20 | 1.25 |
| E           | 0.75     | 0.80 | 0.85 |
| e           | 0.40 BSC |      |      |
| H E         | 1.15     | 1.20 | 1.25 |
| L           | 0.29 REF |      |      |
| L2          | 0.15     | 0.20 | 0.25 |

### GENERIC MARKING DIAGRAM\*



XX = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G", may or not be present.

DOCUMENT NUMBER: 98AON12989D

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DESCRIPTION: SOT-723

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