International
IOR Rectifier

IRF6715MPbF
IRF6715MTRPbF

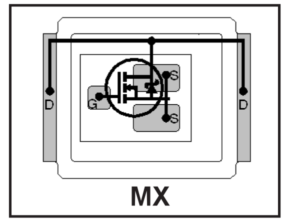
DirectFET™ Power MOSFET ②

- RoHs Compliant and Halogen Free①
- Low Profile (<0.6 mm)
- Dual Sided Cooling Compatible ①
- Ultra Low Package Inductance
- Optimized for High Frequency Switching ①
- Ideal for CPU Core DC-DC Converters
- Optimized for Sync. FET socket of Sync. Buck Converter①
- Low Conduction and Switching Losses
- Compatible with existing Surface Mount Techniques ①
- 100% Rg tested

Typical values (unless otherwise specified)

V_{DSS}	V_{GS}	$R_{DS(on)}$	$R_{DS(on)}$
25V max	±20V max	1.3mΩ@ 10V	2.1mΩ@ 4.5V

$Q_{g\ tot}$	Q_{gd}	Q_{gs2}	Q_{rr}	Q_{oss}	$V_{gs(th)}$
40nC	12.0nC	5.3nC	37nC	26nC	1.9V



DirectFET™ ISOMETRIC

Applicable DirectFET Outline and Substrate Outline (see p.7,8 for details)①

SQ	SX	ST		MQ	**MX**	MT	MP			

Description

The IRF6715MPbF combines the latest HEXFET® Power MOSFET Silicon technology with the advanced DirectFET™ packaging to achieve the lowest on-state resistance in a package that has the footprint of a SO-8 and only 0.6 mm profile. The DirectFET package is compatible with existing layout geometries used in power applications, PCB assembly equipment and vapor phase, infra-red or convection soldering techniques, when application note AN-1035 is followed regarding the manufacturing methods and processes. The DirectFET package allows dual sided cooling to maximize thermal transfer in power systems, improving previous best thermal resistance by 80%.

The IRF6715MPbF balances both low resistance and low charge along with ultra low package inductance to reduce both conduction and switching losses. The reduced total losses make this product ideal for high efficiency DC-DC converters that power the latest generation of processors operating at higher frequencies. The IRF6715MPbF has been optimized for parameters that are critical in synchronous buck including Rds(on), gate charge and Cdv/dt-induced turn on immunity. The IRF6715MPbF offers particularly low Rds(on) and high Cdv/dt immunity for synchronous FET applications.

Absolute Maximum Ratings

	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	25	V
V_{GS}	Gate-to-Source Voltage	±20	
I_D @ $T_A = 25°C$	Continuous Drain Current, V_{GS} @ 10V ③	34	A
I_D @ $T_A = 70°C$	Continuous Drain Current, V_{GS} @ 10V ③	27	
I_D @ $T_C = 25°C$	Continuous Drain Current, V_{GS} @ 10V ④	180	
I_{DM}	Pulsed Drain Current ⑤	270	
E_{AS}	Single Pulse Avalanche Energy ⑥	200	mJ
I_{AR}	Avalanche Current ⑤	27	A

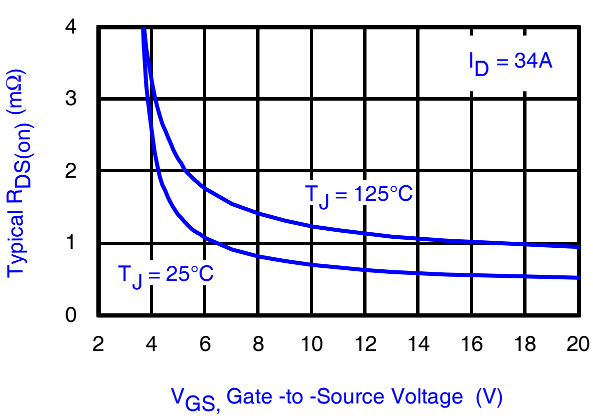


Fig 1. Typical On-Resistance Vs. Gate Voltage

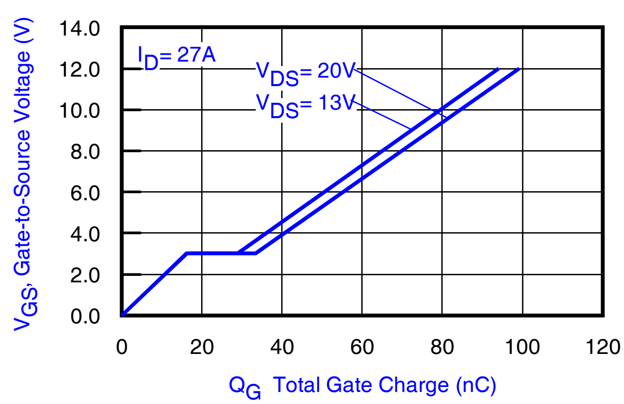


Fig 2. Typical Total Gate Charge vs Gate-to-Source Voltage

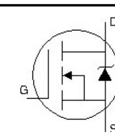
Notes:

① Click on this section to link to the appropriate technical paper.
② Click on this section to link to the DirectFET Website.
③ Surface mounted on 1 in. square Cu board, steady state.
④ T_C measured with thermocouple mounted to top (Drain) of part.
⑤ Repetitive rating; pulse width limited by max. junction temperature.
⑥ Starting $T_J = 25°C$, $L = 0.56mH$, $R_G = 25\Omega$, $I_{AS} = 27A$.

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	25	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	17	—	mV/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	1.3	1.6	mΩ	V_{GS} = 10V, I_D = 34A ⑦
		—	2.1	2.7		V_{GS} = 4.5V, I_D = 27A ⑦
$V_{GS(th)}$	Gate Threshold Voltage	1.4	1.9	2.4	V	V_{DS} = V_{GS}, I_D = 100µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-6.2	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	µA	V_{DS} = 20V, V_{GS} = 0V
		—	—	150		V_{DS} = 20V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
gfs	Forward Transconductance	135	—	—	S	V_{DS} = 13V, I_D = 27A
Q_g	Total Gate Charge	—	40	59	nC	V_{DS} = 13V V_{GS} = 4.5V I_D = 27A See Fig. 15
Q_{gs1}	Pre-Vth Gate-to-Source Charge	—	12	—		
Q_{gs2}	Post-Vth Gate-to-Source Charge	—	5.3	—		
Q_{gd}	Gate-to-Drain Charge	—	12	—		
Q_{godr}	Gate Charge Overdrive	—	11	—		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	—	17	—		
Q_{oss}	Output Charge	—	26	—	nC	V_{DS} = 16V, V_{GS} = 0V
R_G	Gate Resistance	—	1.1	2.0	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	20	—	ns	V_{DD} = 13V, V_{GS} = 4.5V ⑦ I_D = 27A R_G = 1.8Ω See Fig. 17
t_r	Rise Time	—	31	—		
$t_{d(off)}$	Turn-Off Delay Time	—	16	—		
t_f	Fall Time	—	12	—		
C_{iss}	Input Capacitance	—	5340	—	pF	V_{GS} = 0V V_{DS} = 13V f = 1.0MHz
C_{oss}	Output Capacitance	—	1280	—		
C_{rss}	Reverse Transfer Capacitance	—	600	—		

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	98	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ⑤	—	—	270		
V_{SD}	Diode Forward Voltage	—	—	1.0	V	T_J = 25°C, I_S = 27A, V_{GS} = 0V ⑦
t_{rr}	Reverse Recovery Time	—	28	42	ns	T_J = 25°C, I_F = 27A di/dt = 200A/µs ⑦
Q_{rr}	Reverse Recovery Charge	—	37	56	nC	

Notes:

⑦ Pulse width ≤ 400µs; duty cycle ≤ 2%

Absolute Maximum Ratings

	Parameter	Max.	Units
P_D @T_A = 25°C	Power Dissipation ③	2.8	W
P_D @T_A = 70°C	Power Dissipation ③	1.8	
P_D @T_C = 25°C	Power Dissipation ④	78	
T_P	Peak Soldering Temperature	270	°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-40 to + 150	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient ③⑩	——	45	°C/W
$R_{\theta JA}$	Junction-to-Ambient ⑧⑩	12.5	——	
$R_{\theta JA}$	Junction-to-Ambient ⑨⑩	20	——	
$R_{\theta JC}$	Junction-to-Case ④⑩	——	1.6	
$R_{\theta J\text{-}PCB}$	Junction-to-PCB Mounted	1.0	——	
	Linear Derating Factor ③	0.022		W/°C

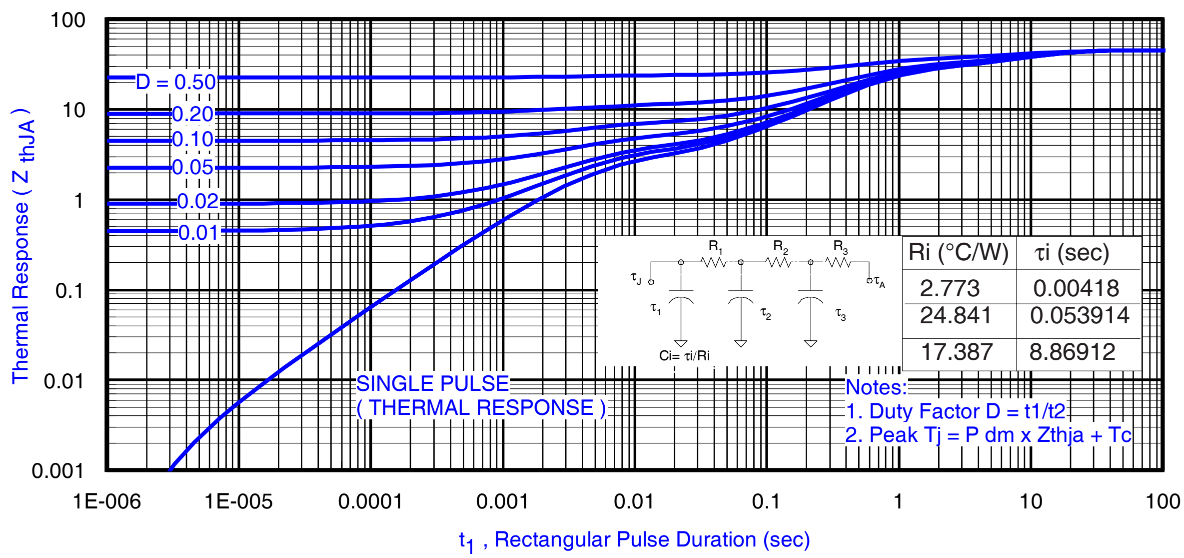


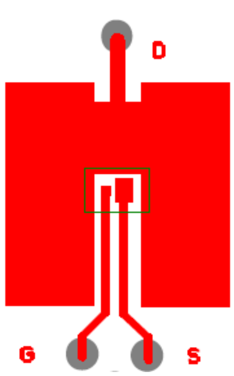
Fig 3. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient ③

Notes:

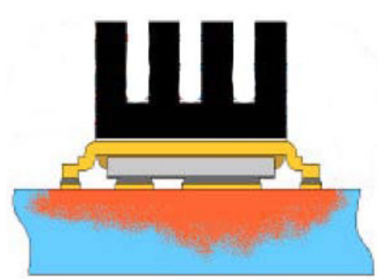
⑧ Used double sided cooling , mounting pad with large heatsink.

⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink.

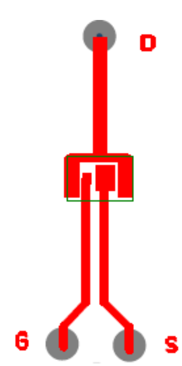
⑩ R_θ is measured at T_J of approximately 90°C .



③ Surface mounted on 1 in. square Cu (still air).



⑨ Mounted to a PCB with small clip heatsink (still air)



⑨ Mounted on minimum footprint full size board with metalized back and with small clip heatsink (still air)

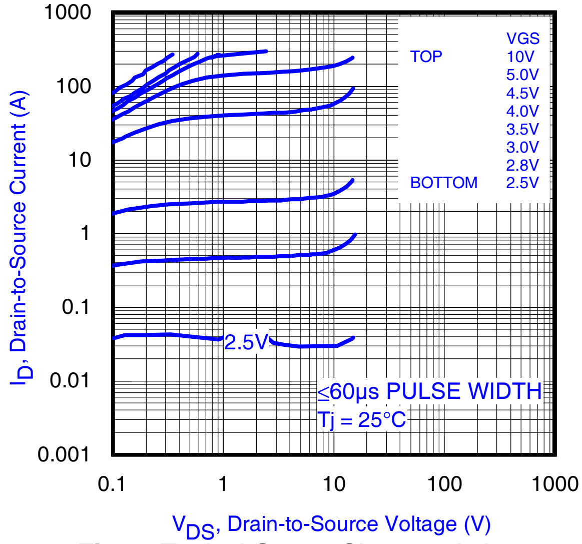


Fig 4. Typical Output Characteristics

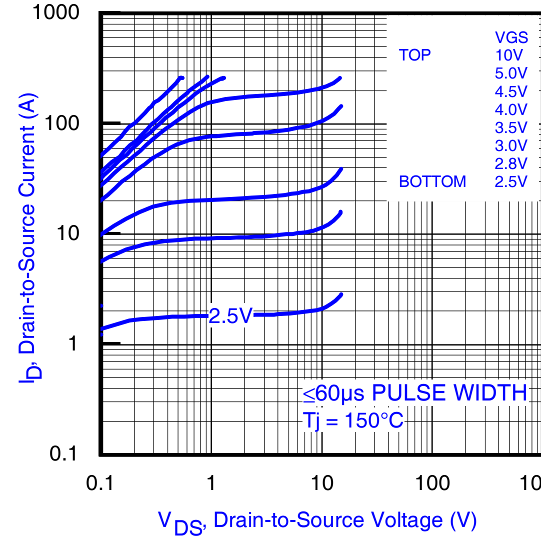


Fig 5. Typical Output Characteristics

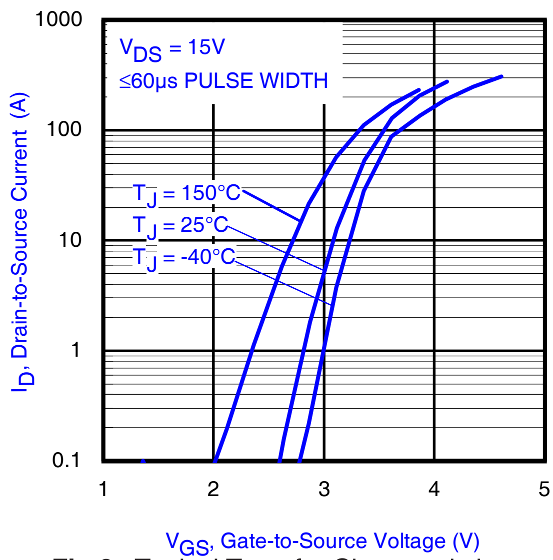


Fig 6. Typical Transfer Characteristics

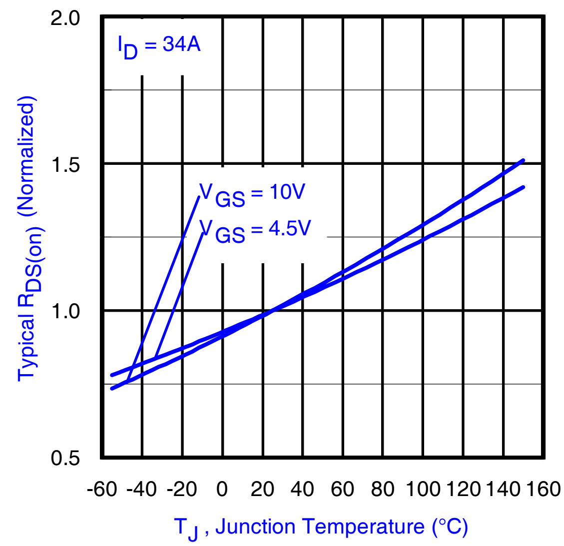


Fig 7. Normalized On-Resistance vs. Temperature

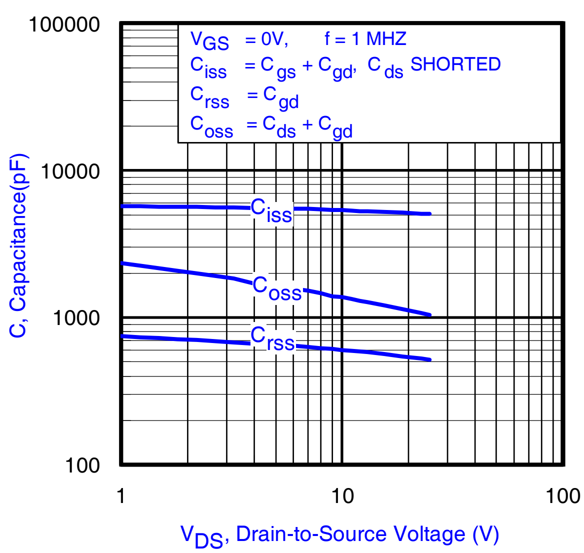


Fig 8. Typical Capacitance vs.Drain-to-Source Voltage

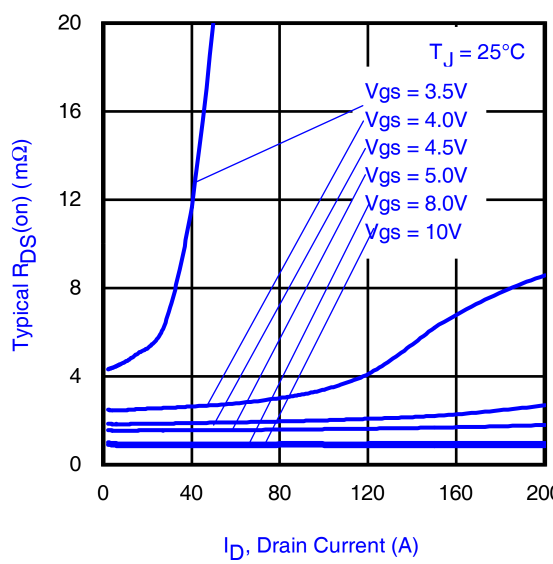


Fig 9. Typical On-Resistance Vs. Drain Current and Gate Voltage

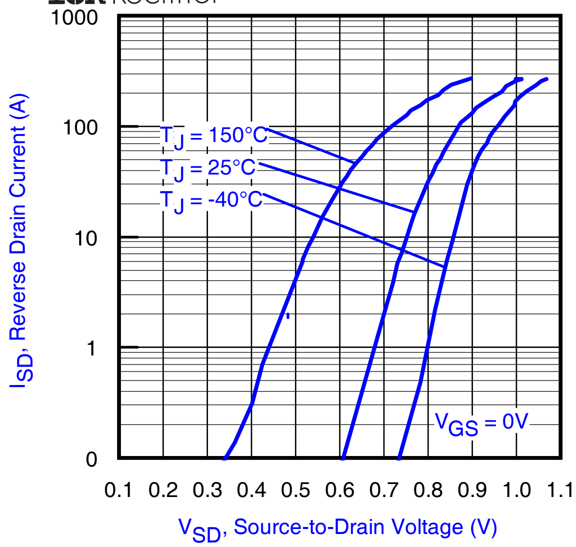


Fig 10. Typical Source-Drain Diode Forward Voltage

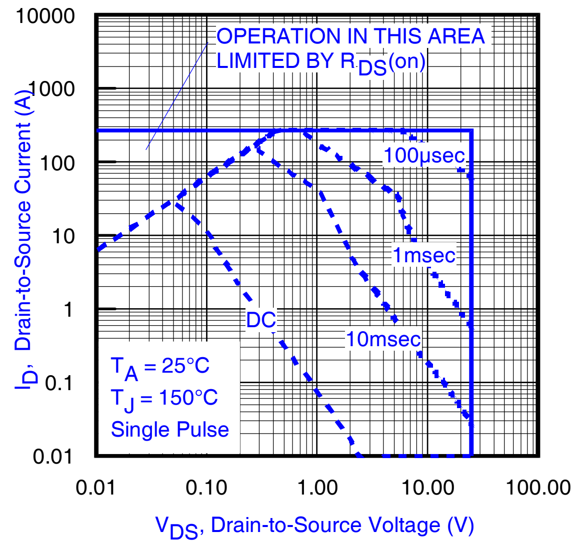


Fig11. Maximum Safe Operating Area

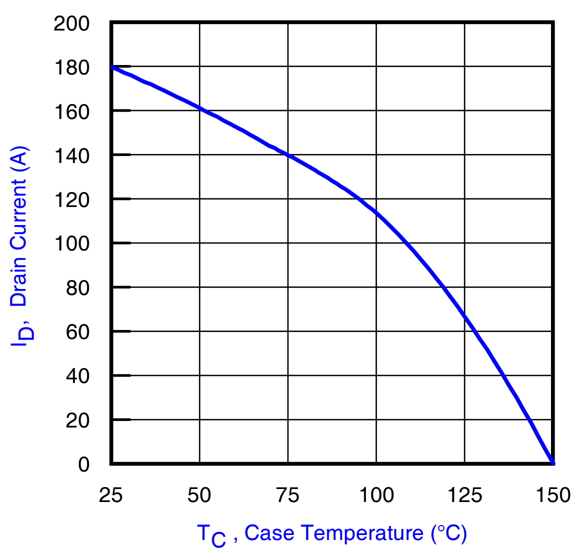


Fig 12. Maximum Drain Current vs. Case Temperature

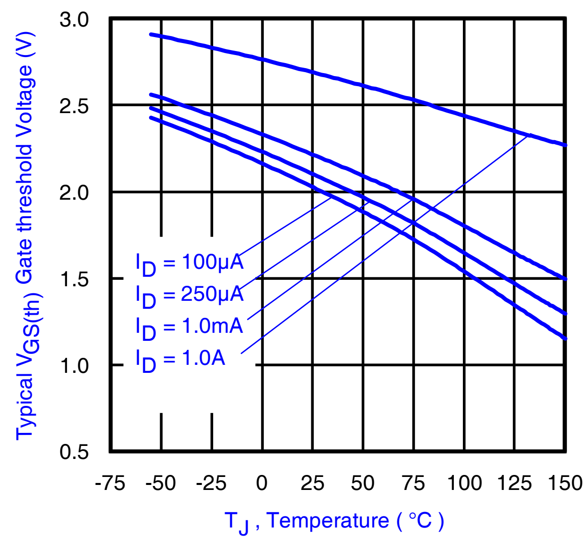


Fig 13. Typical Threshold Voltage vs. Junction Temperature

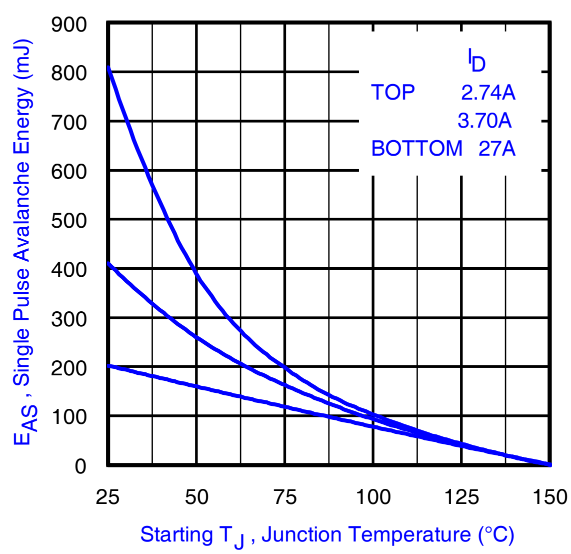


Fig 14. Maximum Avalanche Energy vs. Drain Current

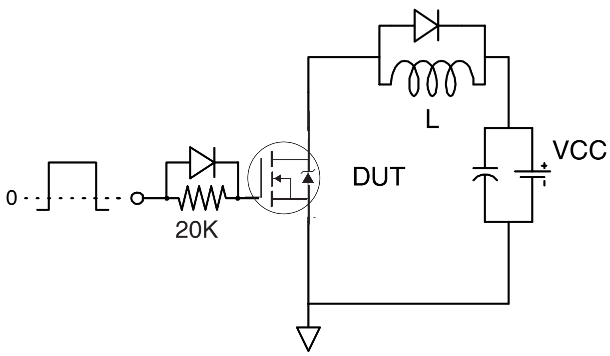


Fig 15a. Gate Charge Test Circuit

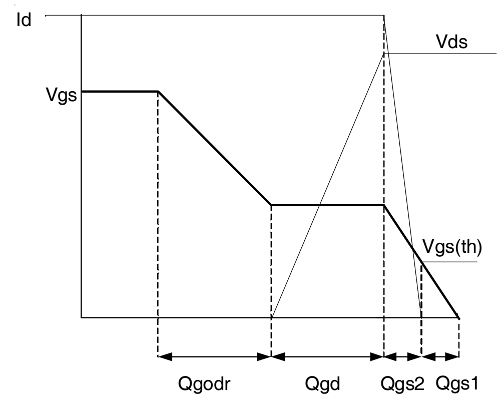


Fig 15b. Gate Charge Waveform

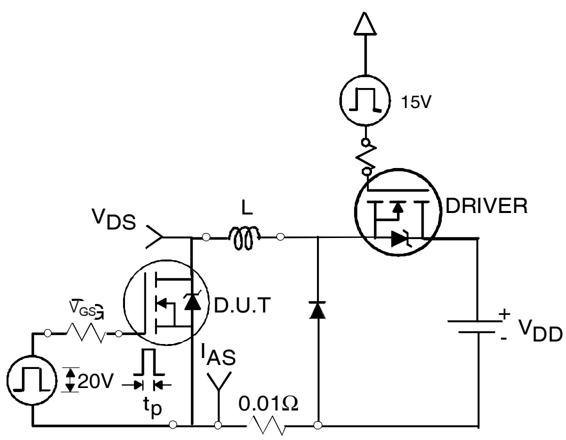


Fig 16a. Unclamped Inductive Test Circuit

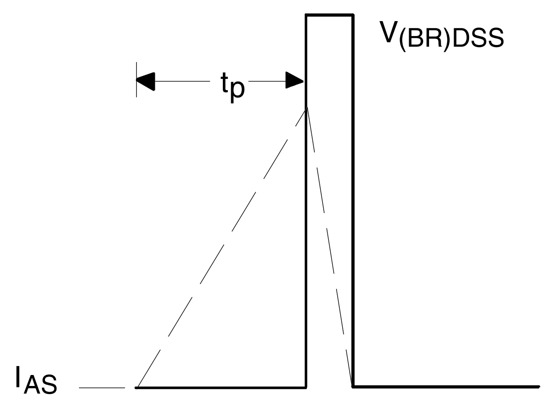


Fig 16b. Unclamped Inductive Waveforms

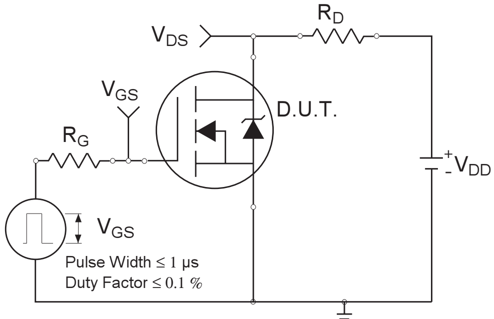


Fig 17a. Switching Time Test Circuit

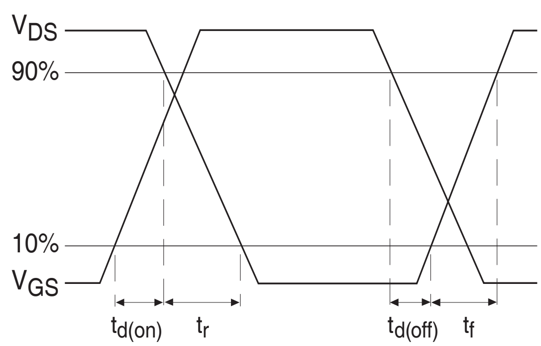
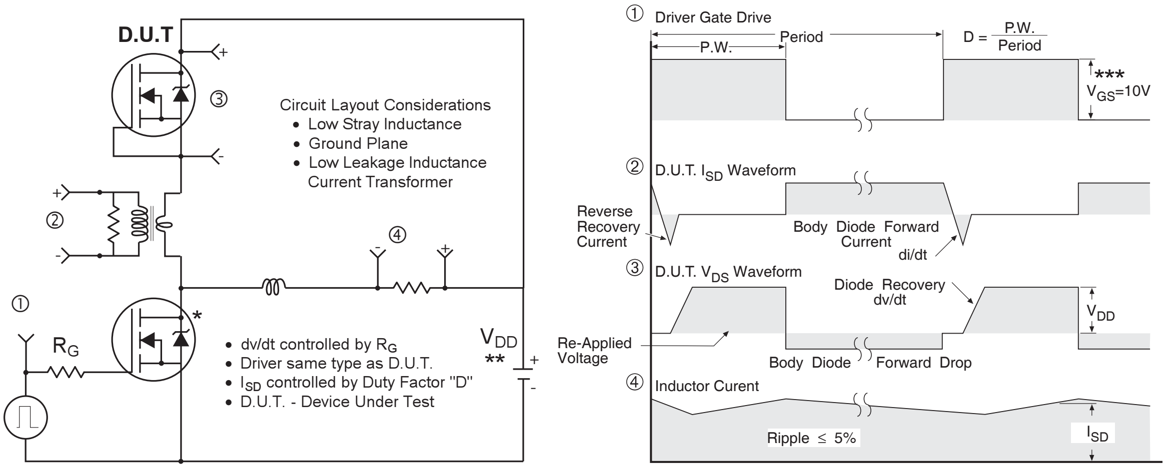


Fig 17b. Switching Time Waveforms



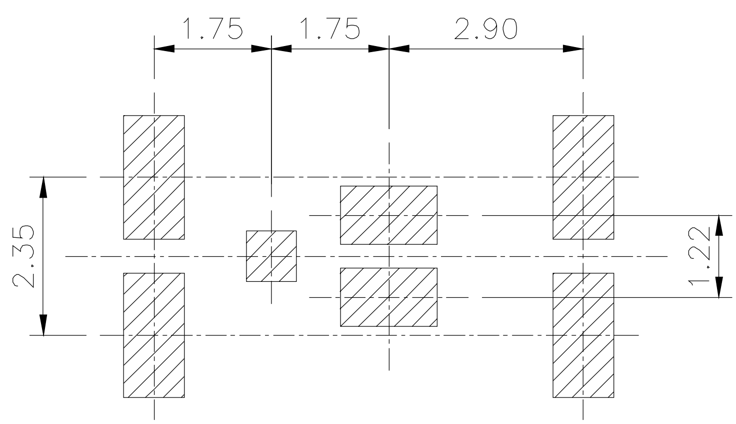
* Use P-Channel Driver for P-Channel Measurements
** Reverse Polarity for P-Channel

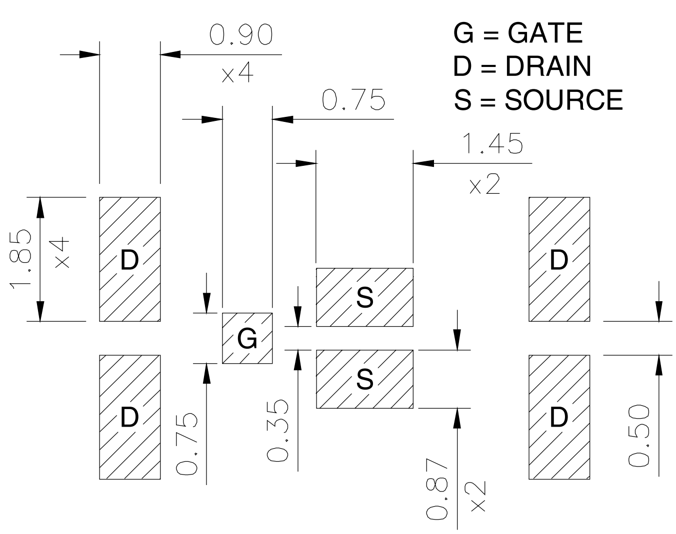
*** V_{GS} = 5V for Logic Level Devices

Fig 18. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs

DirectFET™ Board Footprint, MX Outline (Medium Size Can, X-Designation).

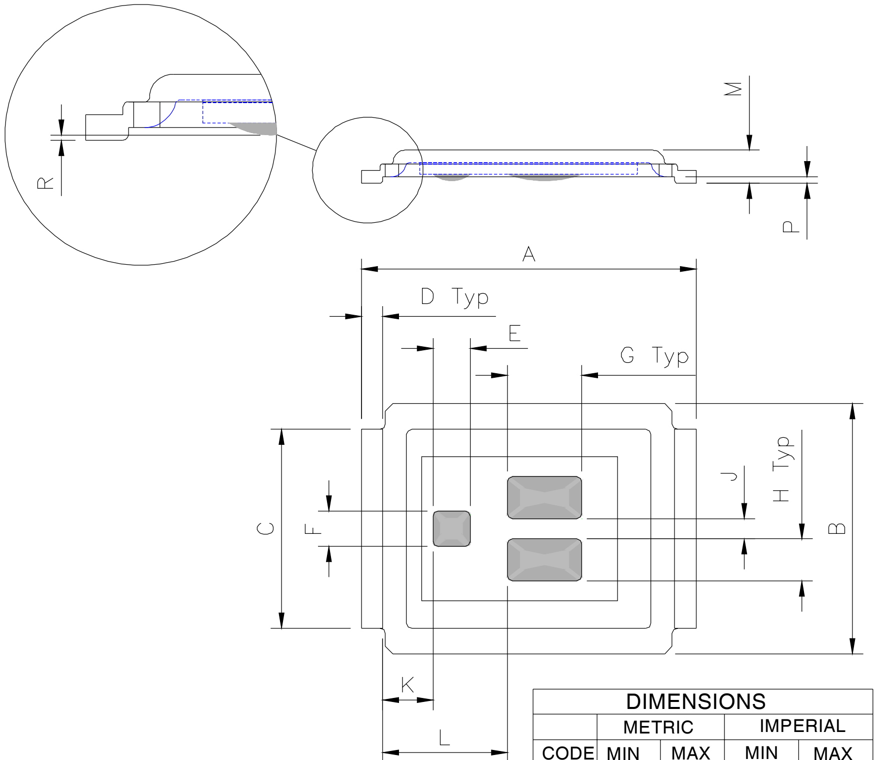
Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET.
This includes all recommendations for stencil and substrate designs.





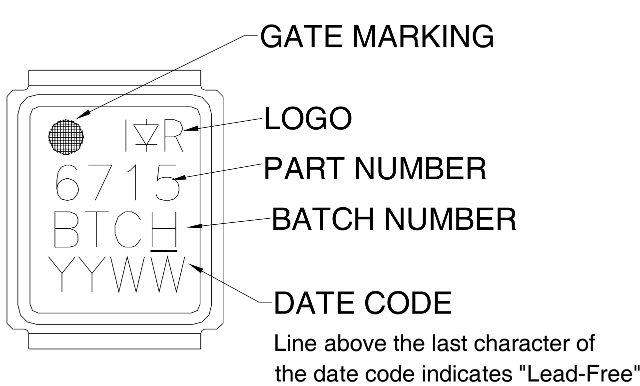
DirectFET™ Outline Dimension, MX Outline (Medium Size Can, X-Designation).

Please see DirectFET application note AN-1035 for all details regarding the assembly of DirectFET. This includes all recommendations for stencil and substrate designs.

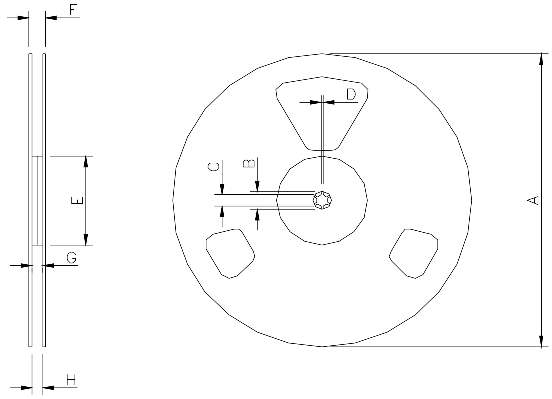


DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.201
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.68	0.72	0.027	0.028
F	0.68	0.72	0.027	0.028
G	1.38	1.42	0.054	0.056
H	0.80	0.84	0.032	0.033
J	0.38	0.42	0.015	0.017
K	0.88	1.01	0.035	0.039
L	2.28	2.41	0.090	0.095
M	0.616	0.676	0.0235	0.0274
R	0.020	0.080	0.0008	0.0031
P	0.08	0.17	0.003	0.007

DirectFET™ Part Marking



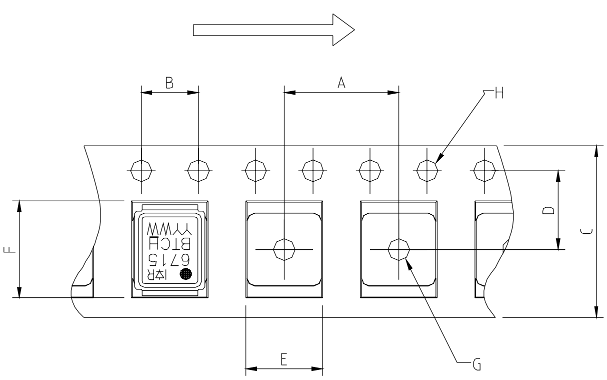
DirectFET™ Tape & Reel Dimension (Showing component orientation).



NOTE: Controlling dimensions in mm
Std reel quantity is 4800 parts. (ordered as IRF6715MTRPBF). For 1000 parts on 7" reel, order IRF6715MTR1PBF

REEL DIMENSIONS								
	STANDARD OPTION **(QTY 4800)**				TR1 OPTION **(QTY 1000)**			
	METRIC		IMPERIAL		METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	330.0	N.C	12.992	N.C	177.77	N.C	6.9	N.C
B	20.2	N.C	0.795	N.C	19.06	N.C	0.75	N.C
C	12.8	13.2	0.504	0.520	13.5	12.8	0.53	0.50
D	1.5	N.C	0.059	N.C	1.5	N.C	0.059	N.C
E	100.0	N.C	3.937	N.C	58.72	N.C	2.31	N.C
F	N.C	18.4	N.C	0.724	N.C	13.50	N.C	0.53
G	12.4	14.4	0.488	0.567	11.9	12.01	0.47	N.C
H	11.9	15.4	0.469	0.606	11.9	12.01	0.47	N.C

LOADED TAPE FEED DIRECTION



NOTE: CONTROLLING DIMENSIONS IN MM

DIMENSIONS				
	METRIC		IMPERIAL	
CODE	MIN	MAX	MIN	MAX
A	7.90	8.10	0.311	0.319
B	3.90	4.10	0.154	0.161
C	11.90	12.30	0.469	0.484
D	5.45	5.55	0.215	0.219
E	5.10	5.30	0.201	0.209
F	6.50	6.70	0.256	0.264
G	1.50	N.C	0.059	N.C
H	1.50	1.60	0.059	0.063

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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IMPORTANT NOTICE

WARNINGS