

# High Voltage Power MOSFET

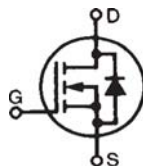
## I<sub>TX</sub>6N200P3HV

$$V_{DSS} = 2000V$$

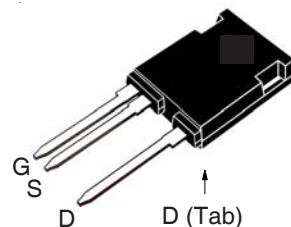
$$I_{D25} = 6A$$

$$R_{DS(on)} \leq 4.0\Omega$$

N-Channel Enhancement Mode



TO-247PLUS-HV



G = Gate      D = Drain  
S = Source    Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
$V_{DSS}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$	2000	V
$V_{DGR}$	$T_J = 25^\circ\text{C}$ to $150^\circ\text{C}$ , $R_{GS} = 1M\Omega$	2000	V
$V_{GSS}$	Continuous	$\pm 20$	V
$V_{GSM}$	Transient	$\pm 30$	V
$I_{D25}$	$T_C = 25^\circ\text{C}$	6	A
$I_{DM}$	$T_C = 25^\circ\text{C}$ , Pulse Width Limited by $T_{JM}$	18	A
$P_D$	$T_C = 25^\circ\text{C}$	960	W
$T_J$		- 55 ... +150	$^\circ\text{C}$
$T_{JM}$		150	$^\circ\text{C}$
$T_{stg}$		- 55 ... +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
$T_{SOLD}$	1.6 mm (0.062in.) from Case for 10s	260	$^\circ\text{C}$
$M_d$	Mounting Force	20..120 / 4.5..27	Nm/lb.in
<b>Weight</b>		6	g

### Features

- High Blocking Voltage
- High Voltage Package

### Advantages

- Easy to Mount
- Space Savings
- High Power Density

### Applications

- High Voltage Power Supplies
- Capacitor Discharge Applications
- Pulse Circuits
- Laser and X-Ray Generation Systems

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSS}$	$V_{GS} = 0V$ , $I_D = 250\mu\text{A}$	2000		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\mu\text{A}$	3.0		5.0 V
$I_{GSS}$	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$			$\pm 100$ nA
$I_{DSS}$	$V_{DS} = 0.8 \cdot V_{DSS}$ , $V_{GS} = 0V$ $T_J = 100^\circ\text{C}$		150	25 $\mu\text{A}$ $\mu\text{A}$
$R_{DS(on)}$	$V_{GS} = 10V$ , $I_D = 3A$ , Note 1			4.0 $\Omega$

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 30\text{V}$ , $I_D = 3\text{A}$ , Note 1	4.5	7.5	S
$C_{iss}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$		3700	pF
$C_{oss}$			236	pF
$C_{rss}$			104	pF
$R_{Gi}$	Gate Input Resistance		2.5	$\Omega$
$t_{d(on)}$	<b>Resistive Switching Times</b> $V_{GS} = 10\text{V}$ , $V_{DS} = 500\text{V}$ , $I_D = 0.5 \cdot I_{D25}$ $R_G = 2\Omega$ (External)		28	ns
$t_r$			22	ns
$t_{d(off)}$			80	ns
$t_f$			46	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$ , $V_{DS} = 0.5 \cdot V_{DSS}$ , $I_D = 0.5 \cdot I_{D25}$		143	nC
$Q_{gs}$			21	nC
$Q_{gd}$			70	nC
$R_{thJC}$				0.13 $^\circ\text{C/W}$
$R_{thCS}$		0.15		$^\circ\text{C/W}$

**Source-Drain Diode**

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max
$I_S$	$V_{GS} = 0\text{V}$ , Note 1			6 A
$I_{SM}$	Repetitive, pulse Width Limited by $T_{JM}$			24 A
$V_{SD}$	$I_F = I_S$ , $V_{GS} = 0\text{V}$ , Note 1			1.5 V
$t_{rr}$	$I_F = 3\text{A}$ , $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 100\text{V}$		520	ns
$Q_{RM}$			580	nC
$I_{RM}$			2.2	A

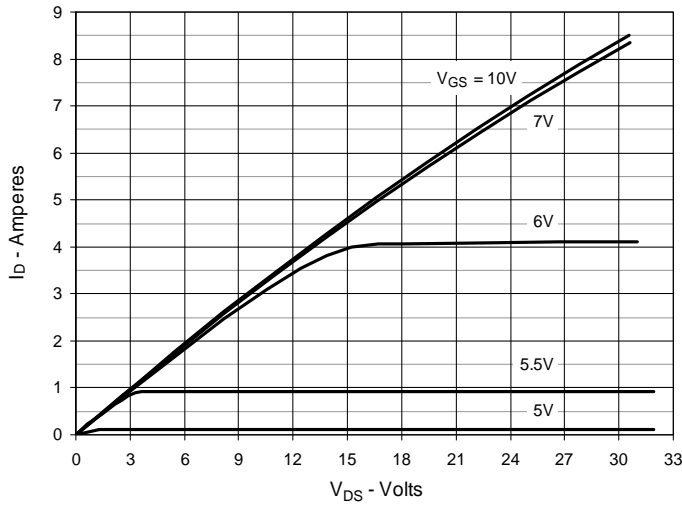
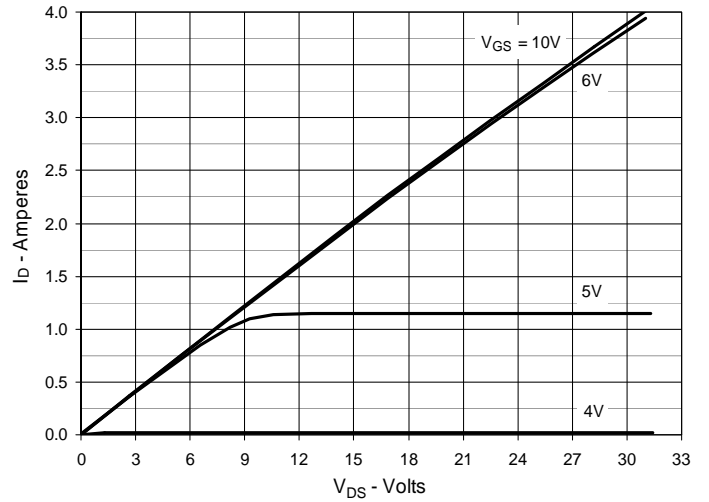
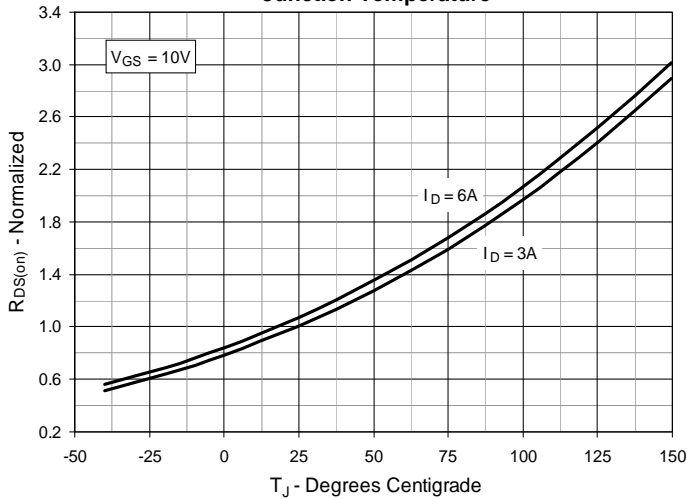
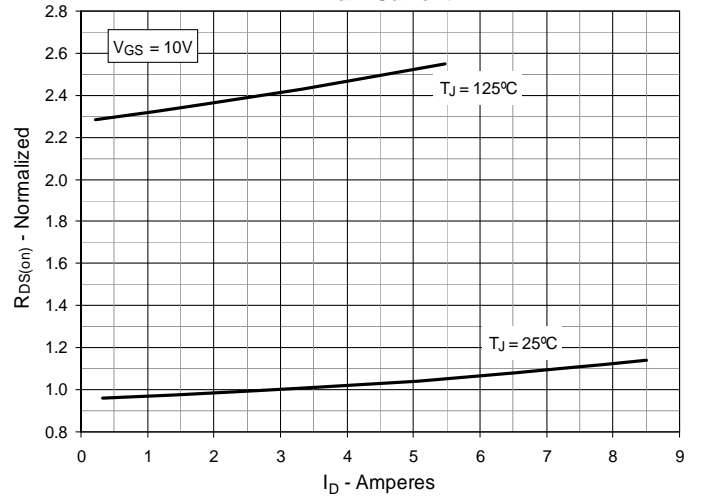
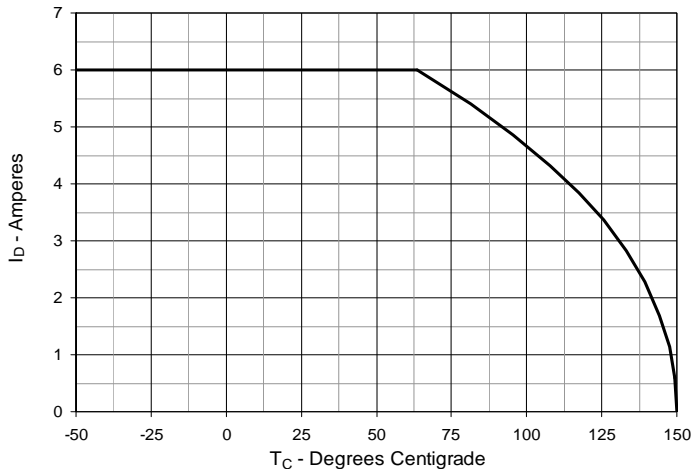
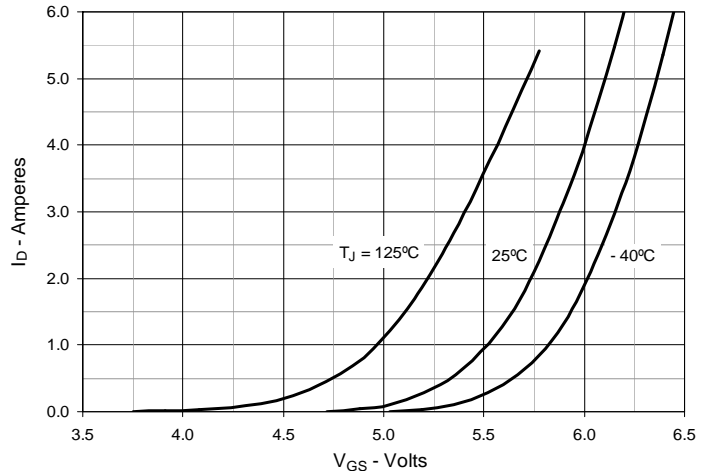
Note: 1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .

**ADVANCE TECHNICAL INFORMATION**

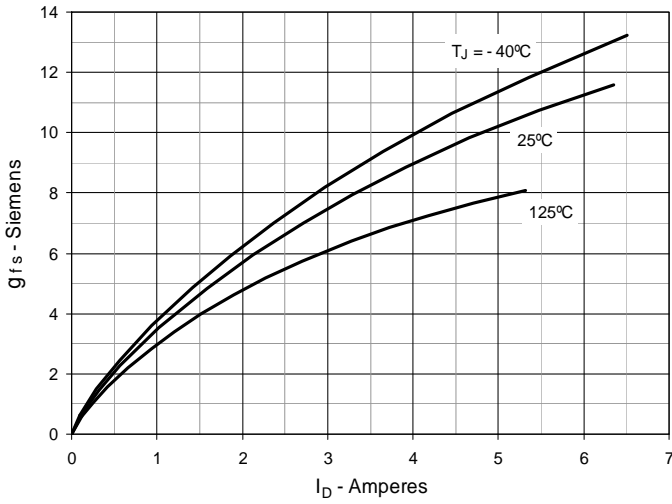
The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

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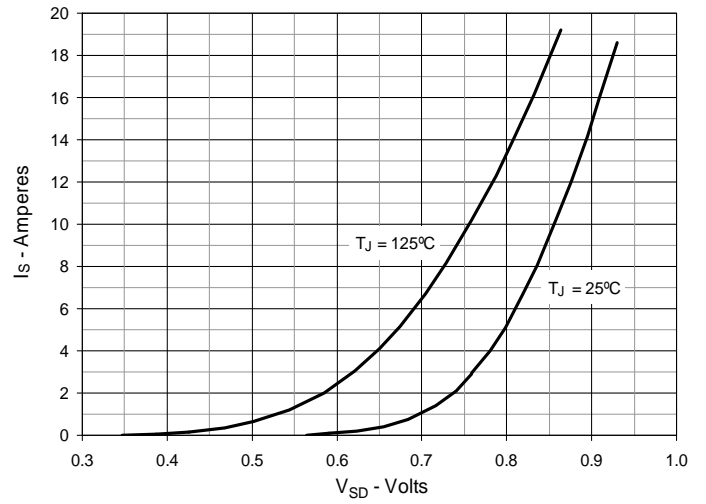
IXYS MOSFETs and IGBTs are covered	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
by one or more of the following U.S. patents:	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

**Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$** 

**Fig. 2. Output Characteristics @  $T_J = 125^\circ\text{C}$** 

**Fig. 3.  $R_{DS(on)}$  Normalized to  $I_D = 3\text{A}$  Value vs. Junction Temperature**

**Fig. 4.  $R_{DS(on)}$  Normalized to  $I_D = 3\text{A}$  Value vs. Drain Current**

**Fig. 5. Maximum Drain Current vs. Case Temperature**

**Fig. 6. Input Admittance**


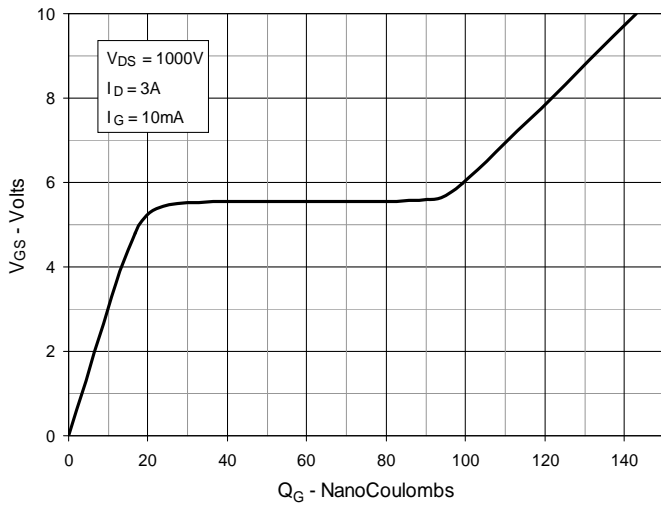
**Fig. 7. Transconductance**



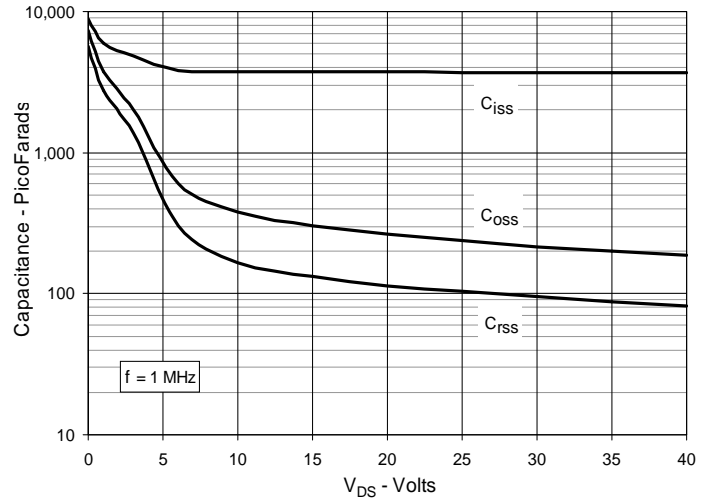
**Fig. 8. Forward Voltage Drop of Intrinsic Diode**



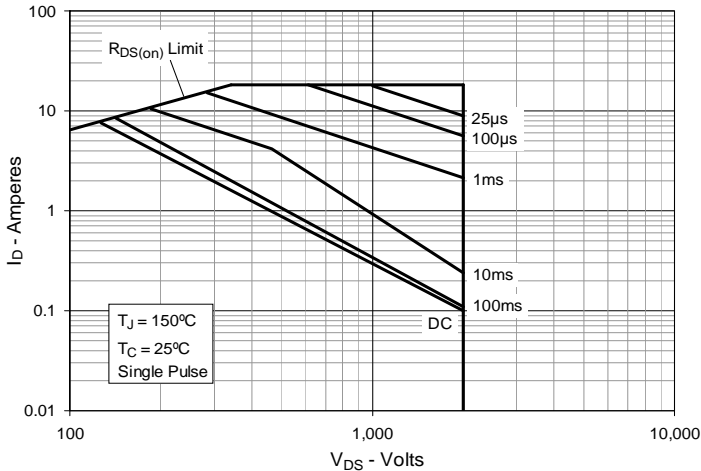
**Fig. 9. Gate Charge**



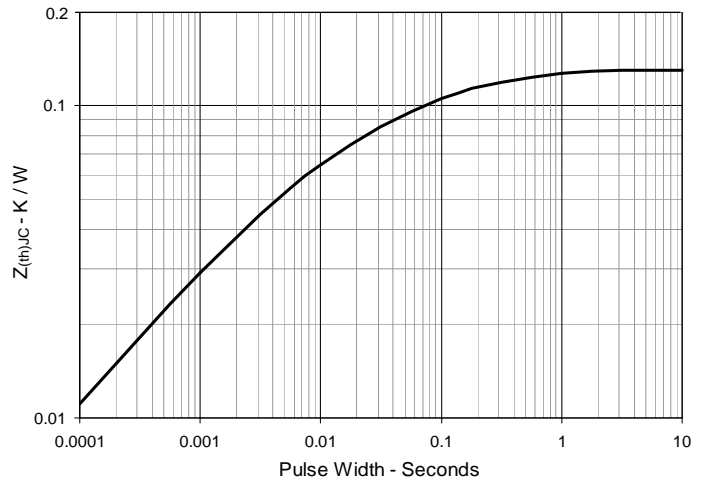
**Fig. 10. Capacitance**

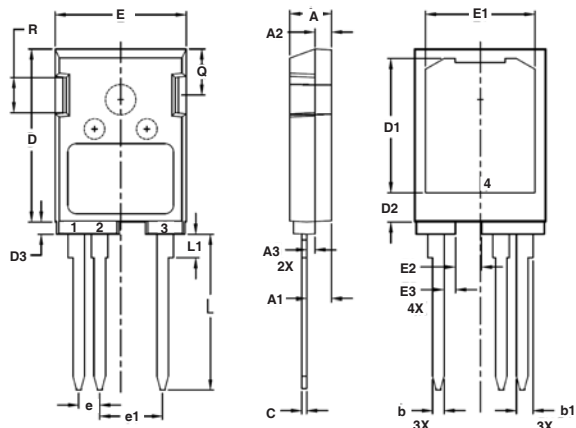


**Fig. 11. Forward-Bias Safe Operating Area**



**Fig. 12 Maximum Transient Thermal Impedance**



**TO-247PLUS HV OUTLINE**


**PINS:**  
**1 - Gate**  
**2 - Source**  
**3,4 - Drain**

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.114	.122	2.90	3.10
A2	.075	.083	1.90	2.10
A3	.035	.043	0.90	1.10
b	.053	.059	1.35	1.50
b1	.075	.083	1.90	2.10
c	.022	.030	0.55	0.75
D	.819	.843	20.80	21.40
D1	.638	.646	16.20	16.40
D2	.134	.146	3.40	3.70
D3	.055	.063	1.40	1.60
E	.622	.638	15.80	16.20
E1	.520	.528	13.20	13.40
E2	.118	.126	3.00	3.20
E3	.051	.059	1.30	1.50
e	.100 BSC		2.54 BSC	
e1	.300 BSC		7.62 BSC	
L	.732	.748	18.60	19.00
L1	.106	.118	2.70	3.00
Q	.216	.224	5.50	5.70
R	.165	.169	4.20	4.30



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