

NTS4173P

MOSFET – Power, Single, P-Channel, SC-70 -30 V, -1.3 A

Features

- -30 V BV_{DS} , Low $R_{DS(on)}$ in SC-70 Package
- Low Threshold Voltage
- Fast Switching Speed
- This is a Halide-Free Device
- This is a Pb-Free Device

Applications

- Load Switch
- Low Current Inverter and DC-DC Converters
- Power Switch for Printers, Communication Equipment

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DSS}	-30	V
Gate-to-Source Voltage		V_{GS}	± 12	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	-1.2	A
			$T_A = 85^\circ\text{C}$	
	$t \leq 5$ s	$T_A = 25^\circ\text{C}$	-1.3	
Power Dissipation (Note 1)	Steady State	$T_A = 25^\circ\text{C}$	0.29	W
	$t \leq 5$ s		0.35	
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	-5.0	A
Operating Junction and Storage Temperature		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)		I_S	-1.0	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	425	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – $t \leq 5$ s (Note 1)	$R_{\theta JA}$	360	

1. Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)

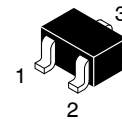
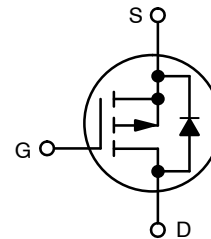


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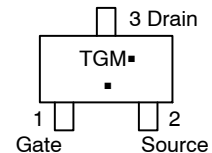
$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
-30 V	150 m Ω @ -10 V	-1.2 A
	200 m Ω @ -4.5 V	-1.0 A
	280 m Ω @ -2.5 V	-0.9 A

SC-70/SOT-323 (3 LEADS)



SC-70/SOT-323
CASE 419
STYLE 8

MARKING DIAGRAM/ PIN ASSIGNMENT



TG = Specific Device Code
M = Date Code*
▪ = Pb-Free Package
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTS4173PT1G	SC-70 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

* Date code orientation may vary depending upon manufacturing location

NTS4173P

MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -24 V, T _J = 25°C V _{GS} = 0 V, V _{DS} = -24 V, T _J = 85°C			-1.0 -5.0	μA
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±12 V			±0.1	μA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250 μA	-0.7	-1.15	-1.5	V
Drain-to-Source On-Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -1.2 A		90	150	mΩ
		V _{GS} = -4.5 V, I _D = -1.0 A		110	200	
		V _{GS} = -2.5 V, I _D = -0.9 A		165	280	
Forward Transconductance	g _{FS}	V _{DS} = -5 V, I _D = -1.2 A		3.6		S

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = -15 V		430		pF
Output Capacitance	C _{oss}			55		
Reverse Transfer Capacitance	C _{rss}			40		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -4.5 V, V _{DS} = -15 V, I _D = -1.2 A		4.8		nC
Threshold Gate Charge	Q _{G(TH)}			0.6		
Gate-to-Source Charge	Q _{GS}			1.1		
Gate-to-Drain Charge	Q _{GD}			1.5		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -10 V, V _{DS} = -15 V, I _D = -1.2 A		10.1		nC
Threshold Gate Charge	Q _{G(TH)}			0.6		
Gate-to-Source Charge	Q _{GS}			1.1		
Gate-to-Drain Charge	Q _{GD}			1.5		

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(on)}	V _{GS} = -4.5 V, V _{DS} = -15 V, I _D = -1.2 A, R _G = 3 Ω		7.7		ns
Rise Time	t _r			5.2		
Turn-Off Delay Time	t _{d(off)}			16.2		
Fall Time	t _f			6.7		
Turn-On Delay Time	t _{d(on)}	V _{GS} = -10 V, V _{DS} = -15 V, I _D = -1.2 A, R _G = 3 Ω		5.3		ns
Rise Time	t _r			6.7		
Turn-Off Delay Time	t _{d(off)}			19.9		
Fall Time	t _f			7.1		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V, I _S = -1.0 A		-0.8	-1.0	V
Reverse Recovery Time	t _{RR}	V _{DS} = 20 V, V _{GS} = 0 V, I _S = -1.0 A, dI _{SD} /dt = 100 A/μs		12		ns
Charge Time	t _a			10		
Discharge Time	t _b			2.0		
Reverse Recovery Charge	Q _{RR}			7.0		nC

- Surface-mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [2 oz] including traces)
- Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%
- Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

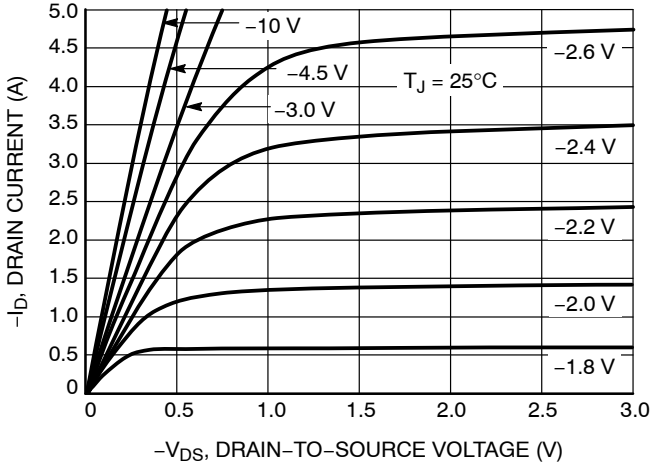


Figure 1. On-Region Characteristics

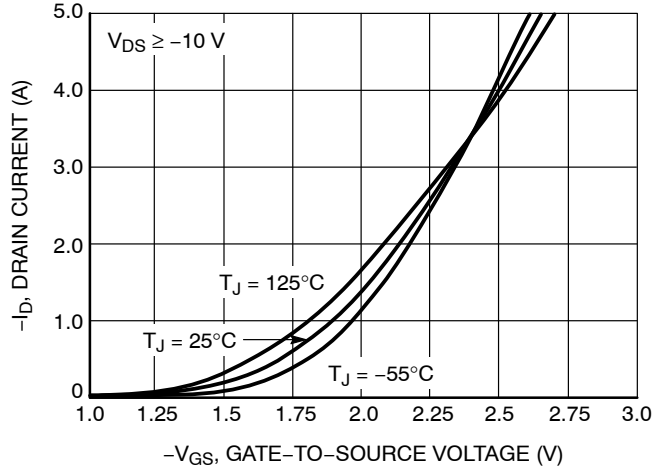


Figure 2. Transfer Characteristics

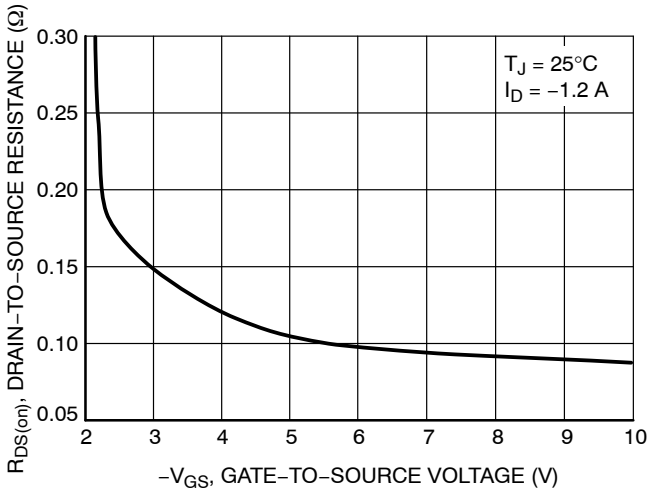


Figure 3. On-Resistance vs. Gate Voltage

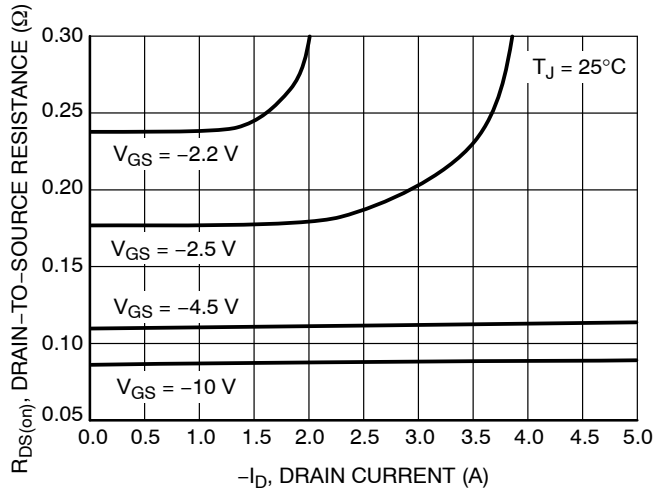


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

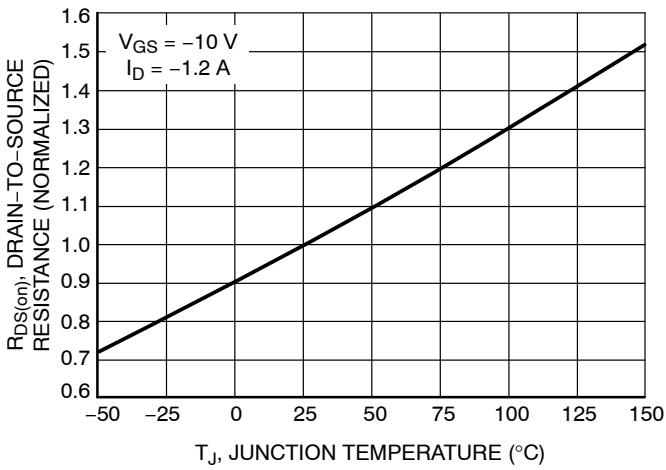


Figure 5. On-Resistance Variation with Temperature

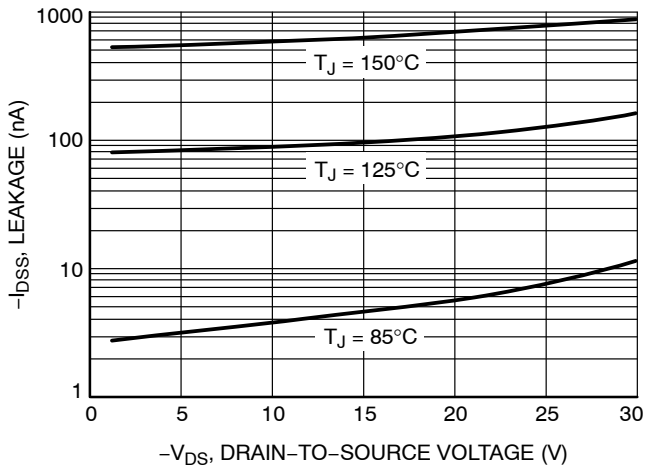


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

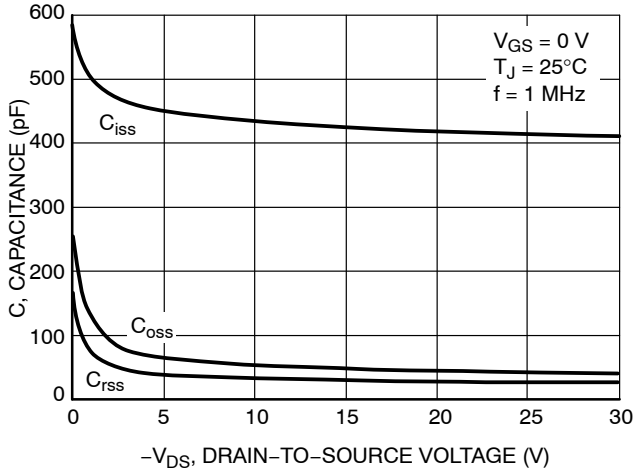


Figure 7. Capacitance Variation

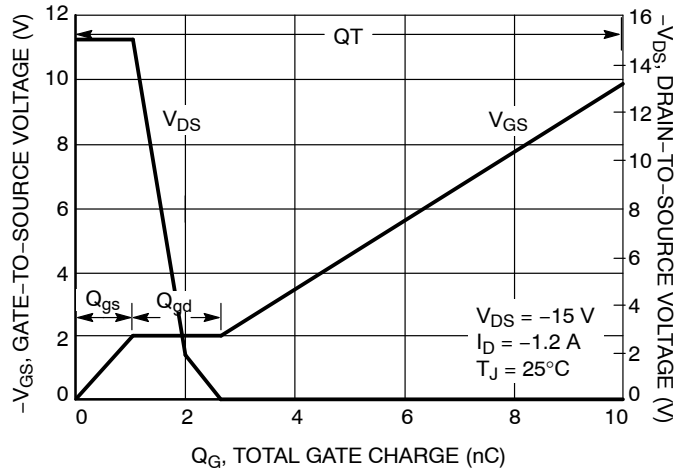


Figure 8. Gate-to-Source Voltage vs. Total Charge

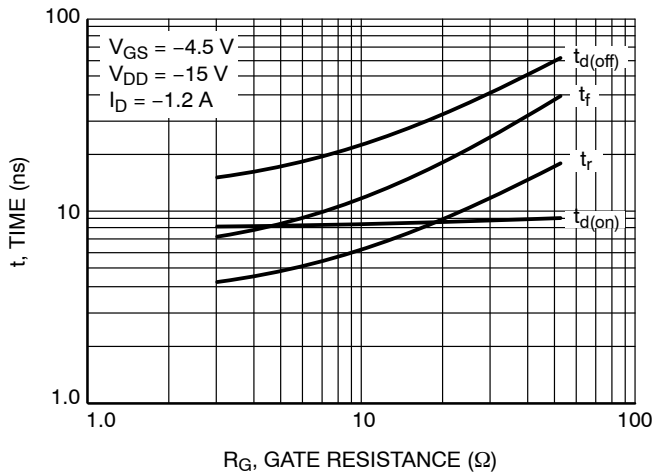


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

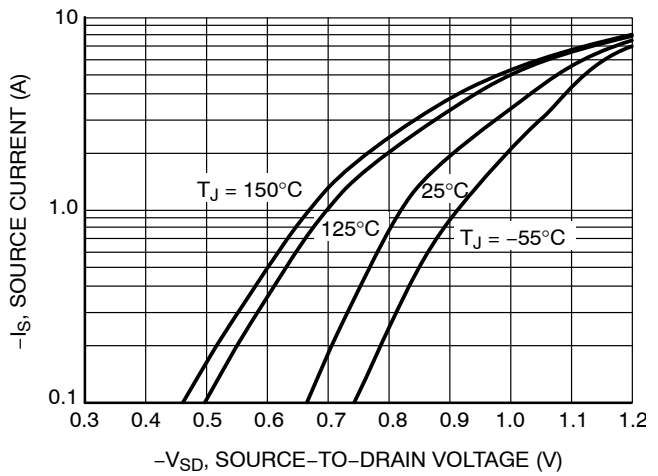


Figure 10. Diode Forward Voltage vs. Current

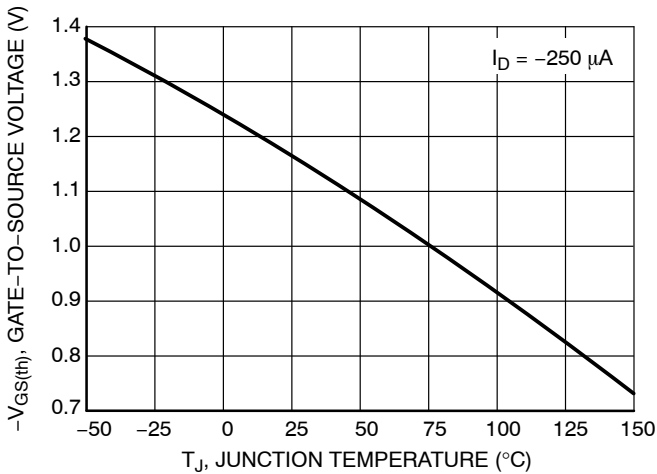


Figure 11. Threshold Voltage

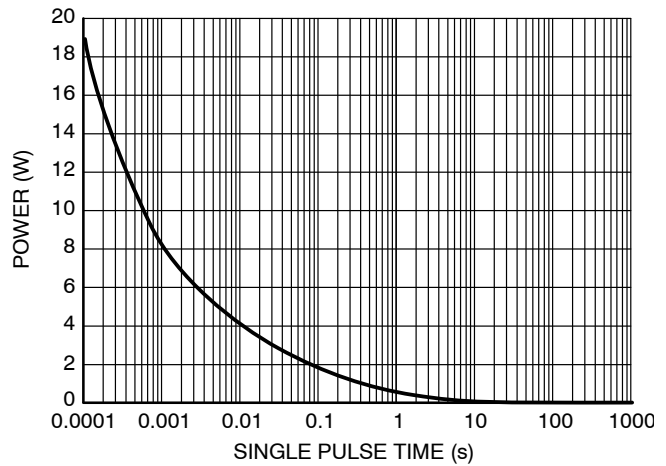


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL PERFORMANCE CURVES

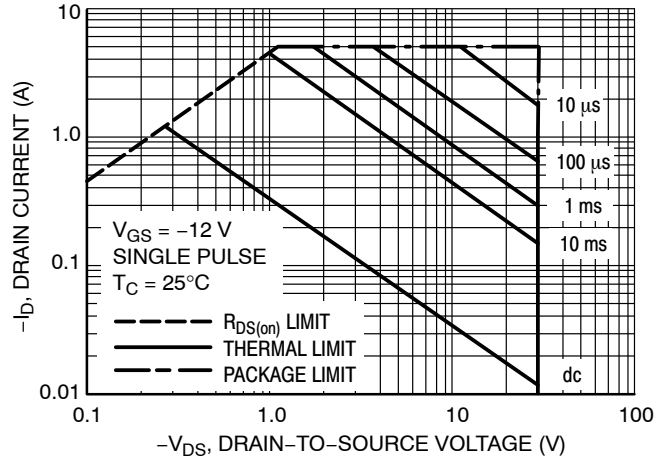


Figure 13. Maximum Rated Forward Biased Safe Operating Area

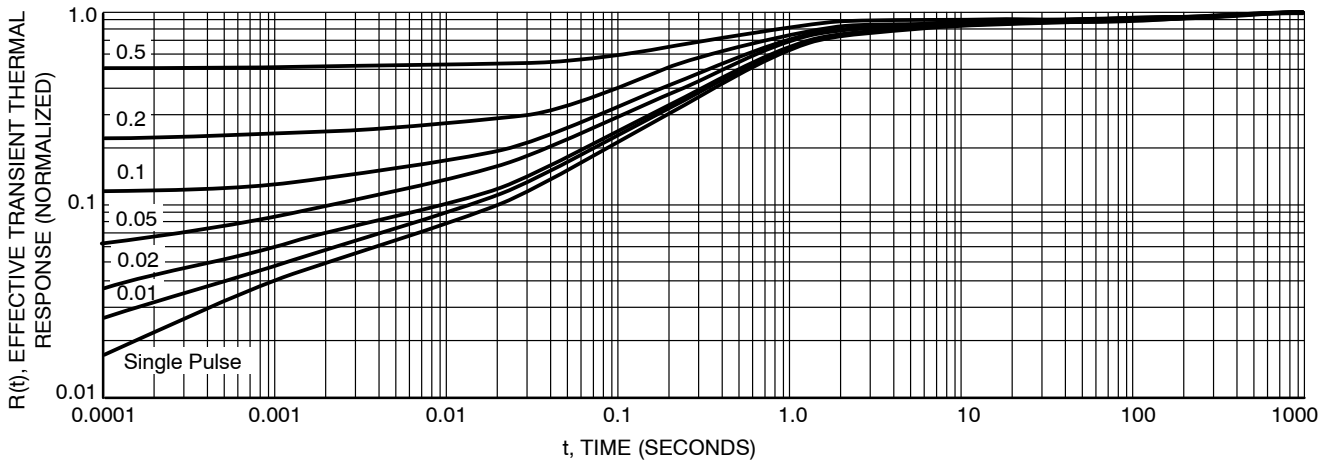


Figure 14. FET Thermal Response

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 4:1

SC-70 (SOT-323) CASE 419 ISSUE R

DATE 11 OCT 2022



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH

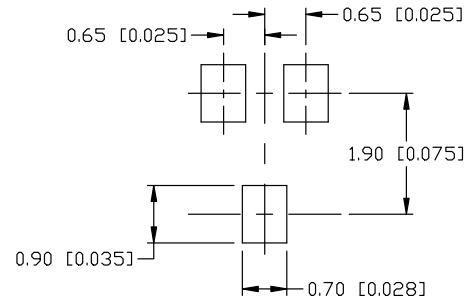
DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	0.70 REF			0.028 BSC		
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.00	2.20	0.071	0.080	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1	0.65 BSC			0.026 BSC		
L	0.20	0.38	0.56	0.008	0.015	0.022
H _E	2.00	2.10	2.40	0.079	0.083	0.095

GENERIC MARKING DIAGRAM



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.



* For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

SOLDERING FOOTPRINT

- | | | | | | |
|---|---|---|--|---|---|
| STYLE 1:
CANCELLED | STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE | STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE | STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE | |
| STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR | STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR | STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN | STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE-ANODE | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE-CATHODE | STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE |

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