

## Inverter Grade Thyristors (Hockey PUK Version), 330 A


**A-PUK (TO-200AB)**
**FEATURES**

- Metal case with ceramic insulator
- All diffused design
- Center amplifying gate
- Guaranteed high  $dV/dt$
- International standard case A-PUK (TO-200AB)
- Guaranteed high  $dI/dt$
- High surge current capability
- Low thermal impedance
- High speed performance
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)


**RoHS  
COMPLIANT**
**PRIMARY CHARACTERISTICS**

Package	A-PUK (TO-200AB)
Circuit configuration	Single SCR
$I_{T(AV)}$	330 A
$V_{DRM}/V_{RRM}$	1000 V, 1200 V
$V_{TM}$	2.07 V
$I_{TSM}$ at 50 Hz	4680 A
$I_{TSM}$ at 60 Hz	4900 A
$I_{GT}$	200 mA
$T_C/T_{hs}$	55 °C

**TYPICAL APPLICATIONS**

- Inverters
- Choppers
- Induction heating
- All types of force-commutated converters

**MAJOR RATINGS AND CHARACTERISTICS**

PARAMETER	TEST CONDITIONS	VALUES	UNITS
$I_{T(AV)}$		330	A
	$T_{hs}$	55	°C
$I_{T(RMS)}$		610	A
	$T_{hs}$	25	°C
$I_{TSM}$	50 Hz	4680	A
	60 Hz	4900	
$i^2t$	50 Hz	110	kA <sup>2</sup> s
	60 Hz	100	
$V_{DRM}/V_{RRM}$		1000 to 1200	V
$t_q$	Range	15 to 30	μs
$T_J$		-40 to 125	°C

**ELECTRICAL SPECIFICATIONS**
**VOLTAGE RATINGS**

TYPE NUMBER	VOLTAGE CODE	$V_{DRM}/V_{RRM}$ , MAXIMUM REPETITIVE PEAK VOLTAGE V	$V_{RSM}$ , MAXIMUM NON-REPETITIVE PEAK VOLTAGE V	$I_{DRM}/I_{RRM}$ MAXIMUM AT $T_J = T_J$ MAXIMUM mA
VS-ST173C..C	10	1000	1100	40
	12	1200	1300	



CURRENT CARRYING CAPABILITY							
FREQUENCY							UNITS
50 Hz	760	660	1200	1030	5570	4920	A
400 Hz	730	590	1260	1080	2800	2460	
1000 Hz	600	490	1200	1030	1620	1390	
2500 Hz	350	270	850	720	800	680	
Recovery voltage $V_r$	50		50		50		V
Voltage before turn-on $V_d$	$V_{DRM}$		$V_{DRM}$		$V_{DRM}$		
Rise of on-state current $di/dt$	50		-		-		A/μs
Heatsink temperature	40	55	40	55	40	55	°C
Equivalent values for RC circuit	47/0.22		47/0.22		47/0.22		Ω/μF

ON-STATE CONDUCTION					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled		330 (120)	A
				55 (85)	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25 °C heatsink temperature double side cooled		610	A
Maximum peak, one half cycle, non-repetitive surge current	$I_{TSM}$	t = 10 ms	No voltage reapplied	4680	
				t = 8.3 ms	
		t = 10 ms	100 % $V_{RRM}$ reapplied	3940	
				t = 8.3 ms	4120
Maximum $I^2t$ for fusing	$I^2t$	t = 10 ms	No voltage reapplied	110	kA <sup>2</sup> s
				t = 8.3 ms	
		t = 10 ms	100 % $V_{RRM}$ reapplied	77	
				t = 8.3 ms	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied		1100	kA <sup>2</sup> √s
Maximum peak on-state voltage	$V_{TM}$	$I_{TM} = 600$ A, $T_J = T_J$ maximum, $t_p = 10$ ms sine wave pulse		2.07	V
Low level value of threshold voltage	$V_{T(TO)1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		1.55	
High level value of threshold voltage	$V_{T(TO)2}$	$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		1.61	
Low level value of forward slope resistance	$r_{t1}$	$(16.7\% \times \pi \times I_{T(AV)} < I < \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		0.87	mΩ
High level value of forward slope resistance	$r_{t2}$	$(I > \pi \times I_{T(AV)})$ , $T_J = T_J$ maximum		0.77	
Maximum holding current	$I_H$	$T_J = 25$ °C, $I_T > 30$ A		600	mA
Typical latching current	$I_L$	$T_J = 25$ °C, $V_A = 12$ V, $R_a = 6$ Ω, $I_G = 1$ A		1000	

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum non-repetitive rate of rise of turned on current	$di/dt$	$T_J = T_J$ maximum, $V_{DRM} = \text{rated } V_{DRM}$ , $I_{TM} = 2 \times di/dt$		1000	A/μs
Typical delay time	$t_d$	$T_J = 25$ °C, $V_{DM} = \text{rated } V_{DRM}$ , $I_{TM} = 50$ A DC, $t_p = 1$ μs Resistive load, gate pulse: 10 V, 5 Ω source		1.1	μs
Maximum turn-off time	minimum	$t_q$	$T_J = T_J$ maximum, $I_{TM} = 300$ A, commutating $di/dt = 20$ A/μs $V_R = 50$ V, $t_p = 500$ μs, $dV/dt$ : see table in device code	15	
	maximum			30	



<b>BLOCKING</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum critical rate of rise of off-state voltage	dV/dt	T <sub>J</sub> = T <sub>J</sub> maximum, linear to 80 % V <sub>DRM</sub> , higher value available on request	500	V/μs
Maximum peak reverse and off-state leakage current	I <sub>RRM</sub> , I <sub>DRM</sub>	T <sub>J</sub> = T <sub>J</sub> maximum, rated V <sub>DRM</sub> /V <sub>RRM</sub> applied	40	mA

<b>TRIGGERING</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum peak gate power	P <sub>GM</sub>	T <sub>J</sub> = T <sub>J</sub> maximum, f = 50 Hz, d% = 50	60	W
Maximum average gate power	P <sub>G(AV)</sub>		10	
Maximum peak positive gate current	I <sub>GM</sub>	T <sub>J</sub> = T <sub>J</sub> maximum, t <sub>p</sub> ≤ 5 ms	10	A
Maximum peak positive gate voltage	+ V <sub>GM</sub>		20	V
Maximum peak negative gate voltage	- V <sub>GM</sub>		5	
Maximum DC gate current required to trigger	I <sub>GT</sub>	T <sub>J</sub> = 25 °C, V <sub>A</sub> = 12 V, R <sub>a</sub> = 6 Ω	200	mA
Maximum DC gate voltage required to trigger	V <sub>GT</sub>		3	V
Maximum DC gate current not to trigger	I <sub>GD</sub>	T <sub>J</sub> = T <sub>J</sub> maximum, rated V <sub>DRM</sub> applied	20	mA
Maximum DC gate voltage not to trigger	V <sub>GD</sub>		0.25	V

<b>THERMAL AND MECHANICAL SPECIFICATIONS</b>				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum operating junction temperature range	T <sub>J</sub>		-40 to 125	°C
Maximum storage temperature range	T <sub>Stg</sub>		-40 to 150	
Maximum thermal resistance, junction to heatsink	R <sub>thJ-hs</sub>	DC operation single side cooled	0.17	K/W
		DC operation double side cooled	0.08	
Maximum thermal resistance, case to heatsink	R <sub>thC-hs</sub>	DC operation single side cooled	0.033	
		DC operation double side cooled	0.017	
Mounting force, ± 10 %			4900 (500)	N (kg)
Approximate weight			50	g
Case style		See dimensions - link at the end of datasheet	A-PUK (TO-200AB)	

<b>ΔR<sub>thJ-hs</sub> CONDUCTION</b>						
CONDUCTION ANGLE	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDITIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.015	0.016	0.011	0.011	T <sub>J</sub> = T <sub>J</sub> maximum	K/W
120°	0.018	0.019	0.019	0.019		
90°	0.024	0.024	0.026	0.026		
60°	0.035	0.035	0.036	0.037		
30°	0.060	0.060	0.060	0.061		

**Note**

- The table above shows the increment of thermal resistance R<sub>thJ-hs</sub> when devices operate at different conduction angles than DC

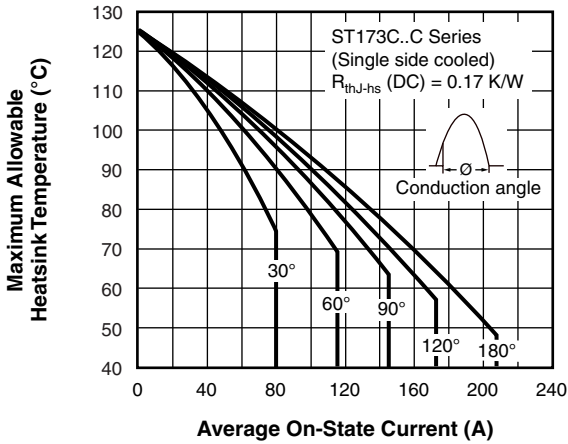


Fig. 1 - Current Ratings Characteristics

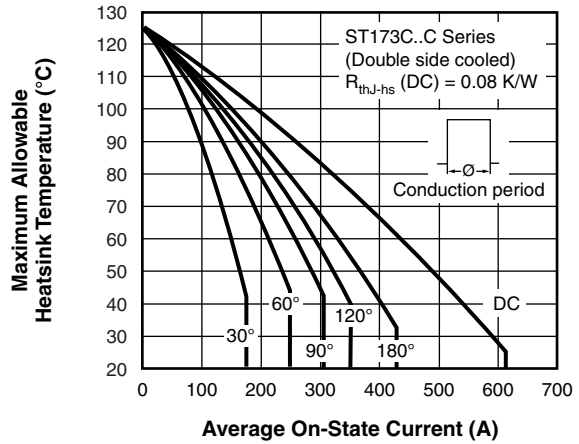


Fig. 4 - Current Ratings Characteristics

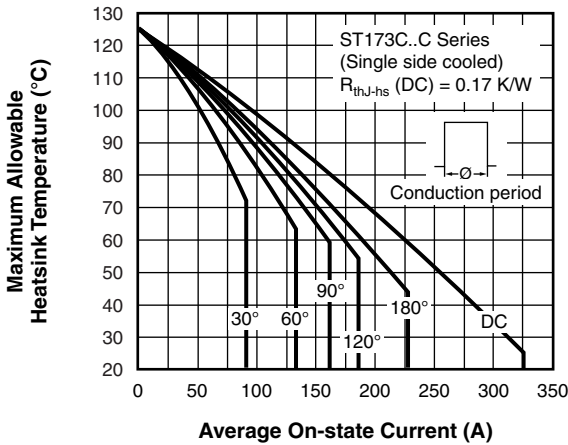


Fig. 2 - Current Ratings Characteristics

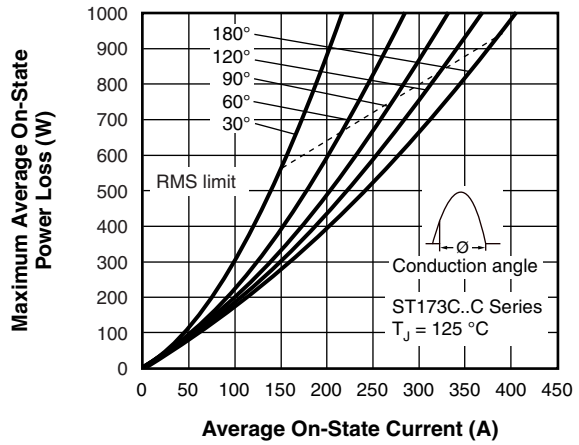


Fig. 5 - On-State Power Loss Characteristics

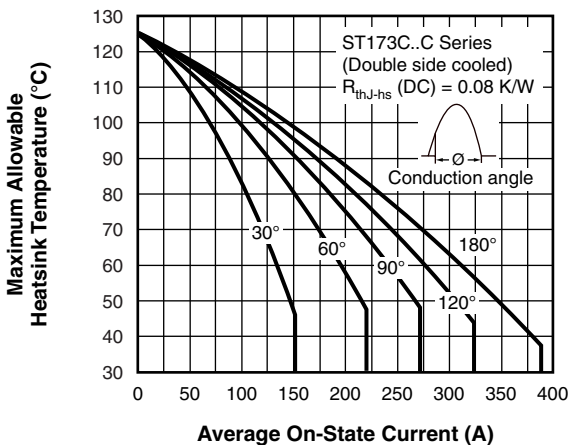


Fig. 3 - Current Ratings Characteristics

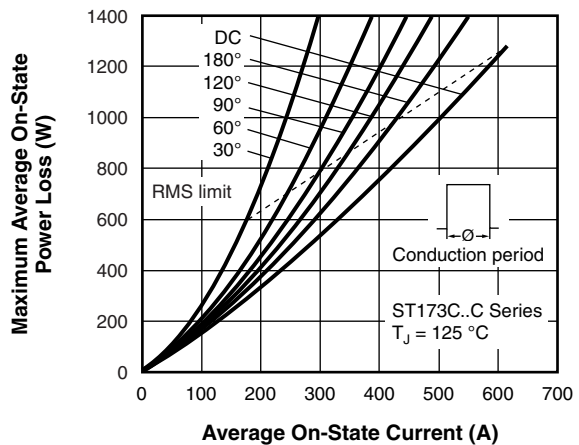


Fig. 6 - On-State Power Loss Characteristics

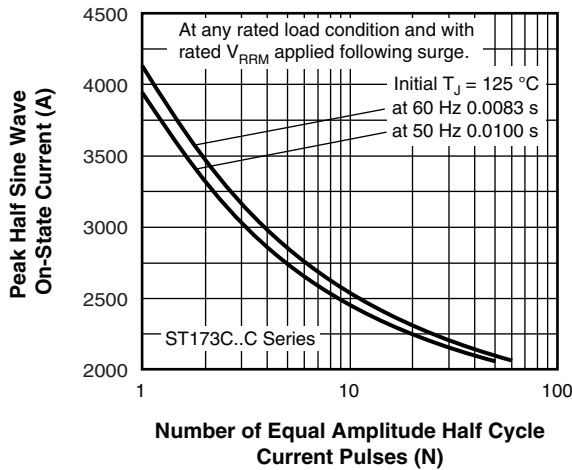


Fig. 7 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

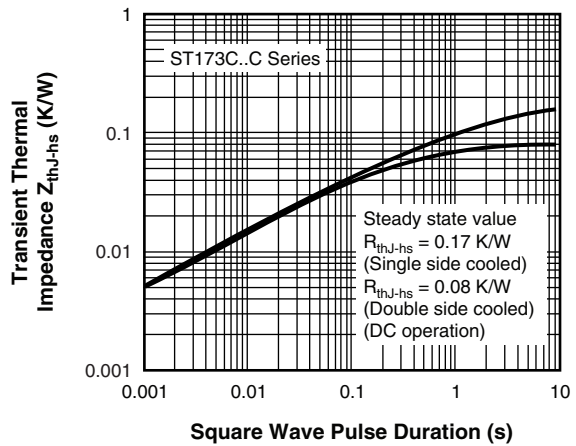


Fig. 10 - Thermal Impedance  $Z_{thJ-hs}$  Characteristics

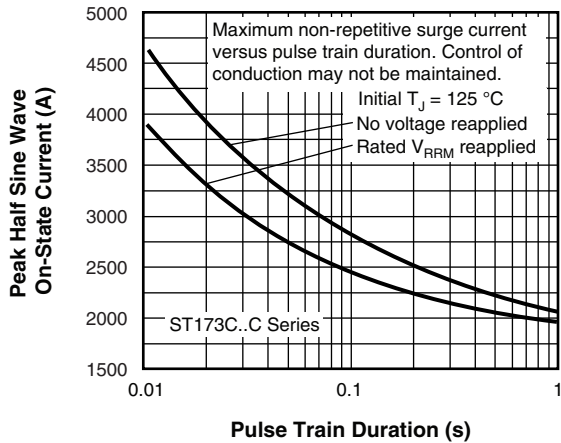


Fig. 8 - Maximum Non-Repetitive Surge Current Single and Double Side Cooled

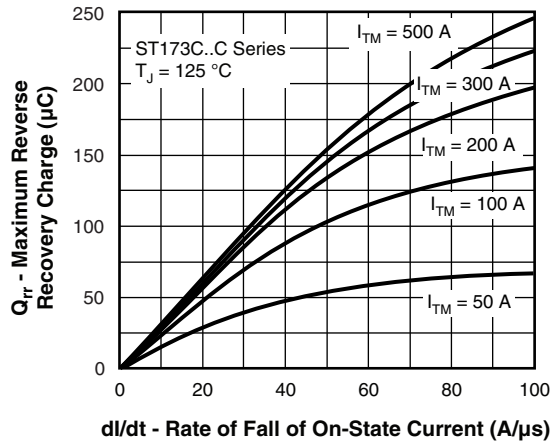


Fig. 11 - Reverse Recovered Charge Characteristics

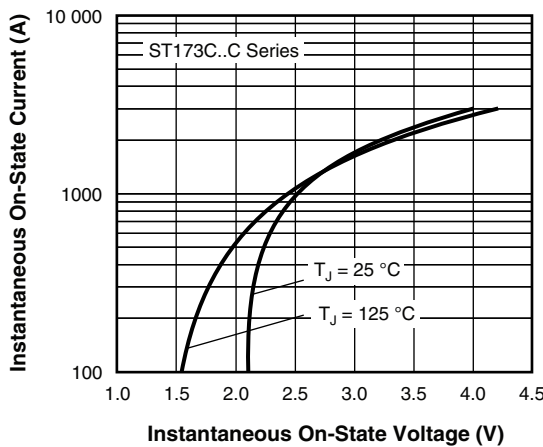


Fig. 9 - On-State Voltage Drop Characteristics

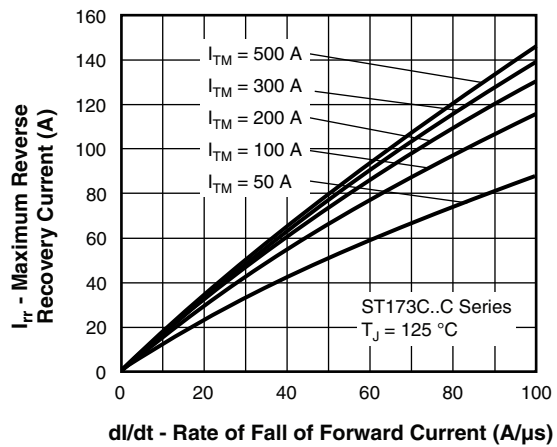


Fig. 12 - Reverse Recovered Current Characteristics

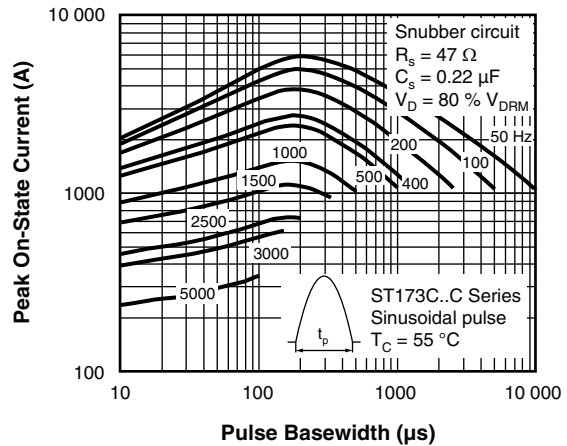
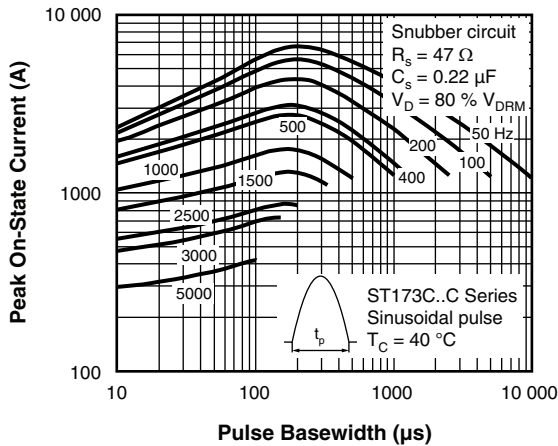


Fig. 13 - Frequency Characteristics

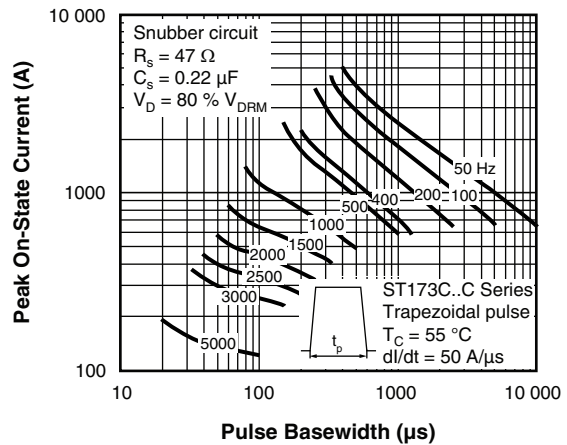
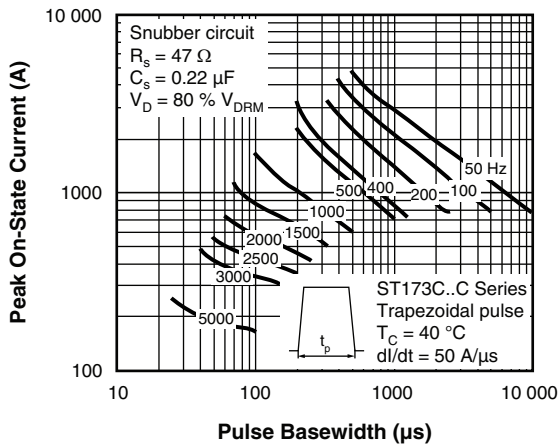


Fig. 14 - Frequency Characteristics

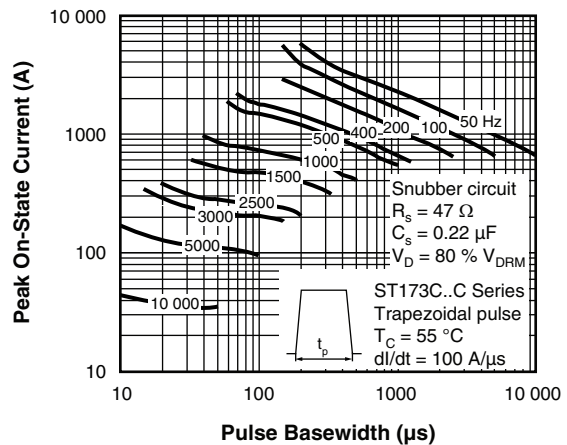
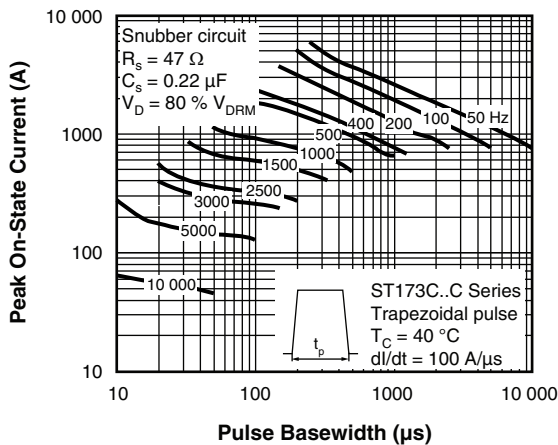


Fig. 15 - Frequency Characteristics

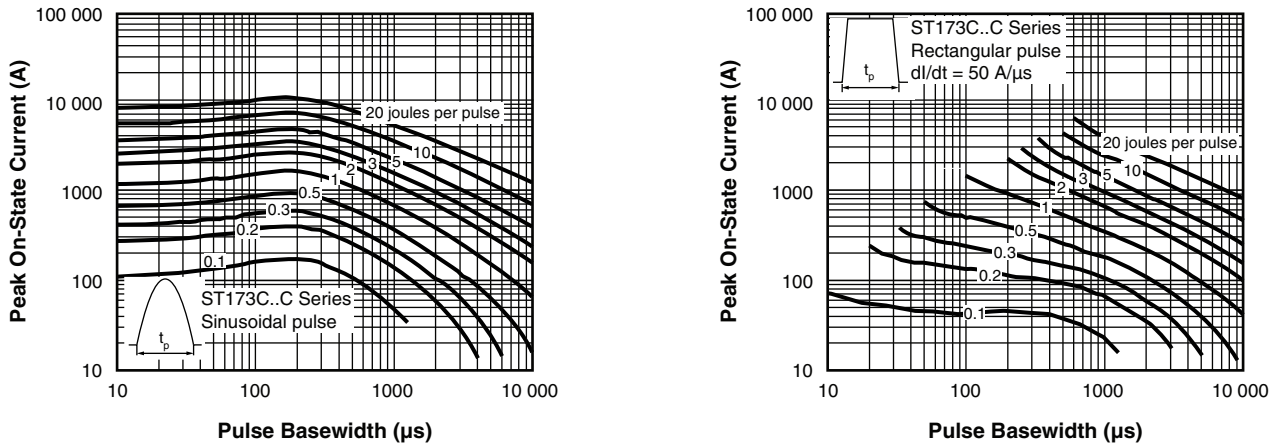


Fig. 16 - Maximum On-State Energy Power Loss Characteristics

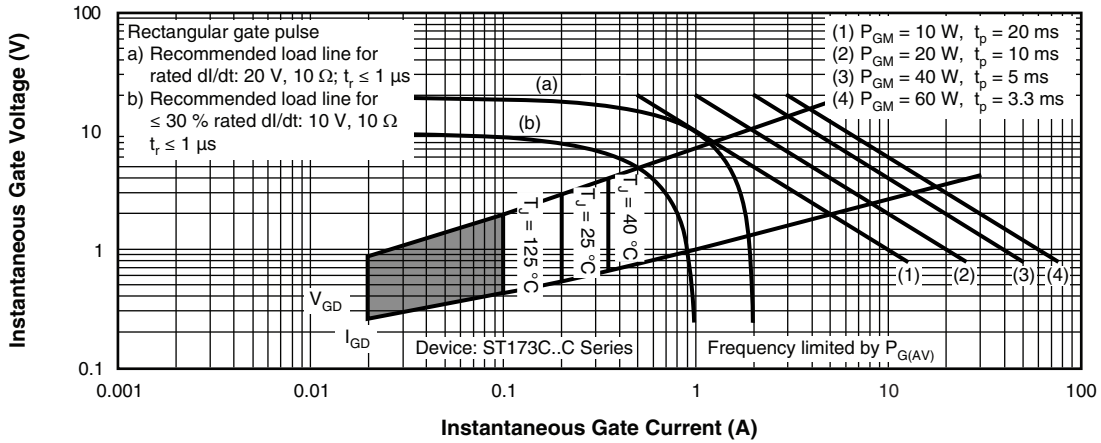
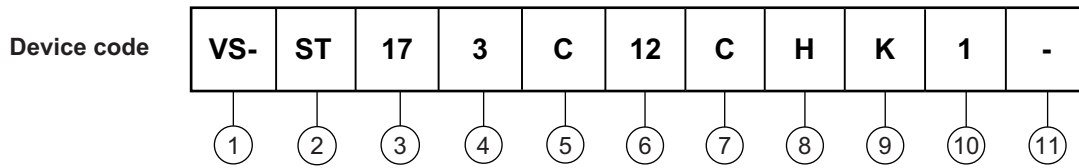


Fig. 17 - Gate Characteristics



## ORDERING INFORMATION TABLE



- 1** - Vishay Semiconductors product
- 2** - Thyristor
- 3** - Essential part number
- 4** - 3 = fast turn-off
- 5** - C = ceramic PUK
- 6** - Voltage code x 100 =  $V_{RRM}$  (see Voltage Ratings table)
- 7** - C = PUK case A-PUK (TO-200AB)
- 8** - Reapplied dV/dt code (for  $t_q$  test condition)
- 9** -  $t_q$  code
- 10** - 0 = eyelet terminals  
(gate and aux. cathode unsoldered leads)  
1 = fast-on terminals  
(gate and aux. cathode unsoldered leads)  
2 = eyelet terminals  
(gate and aux. cathode soldered leads)  
3 = fast-on terminals  
(gate and aux. cathode soldered leads)
- 11** - Critical dV/dt:
  - None = 500 V/ $\mu$ s (standard value)
  - L = 1000 V/ $\mu$ s (special selection)

dV/dt - $t_q$ combinations available					
dV/dt (V/ $\mu$ s)	20	50	100	200	400
$t_q$ ( $\mu$ s)	15	CL	--	--	--
	18	CP	DP	EP	<b>FP</b> *
	20	CK	DK	EK	<b>FK</b> *
	25	CJ	DJ	EJ	FJ
	30	--	DH	EH	FH

\* Standard part number.  
All other types available only on request.

LINKS TO RELATED DOCUMENTS	
Dimensions	<a href="http://www.vishay.com/doc?95074">www.vishay.com/doc?95074</a>

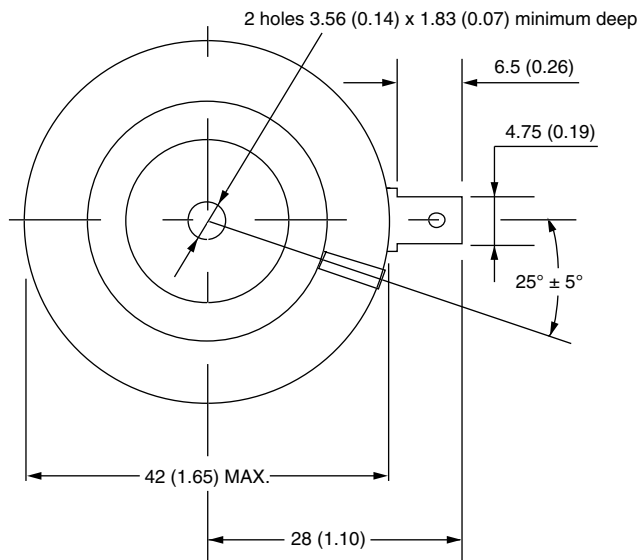
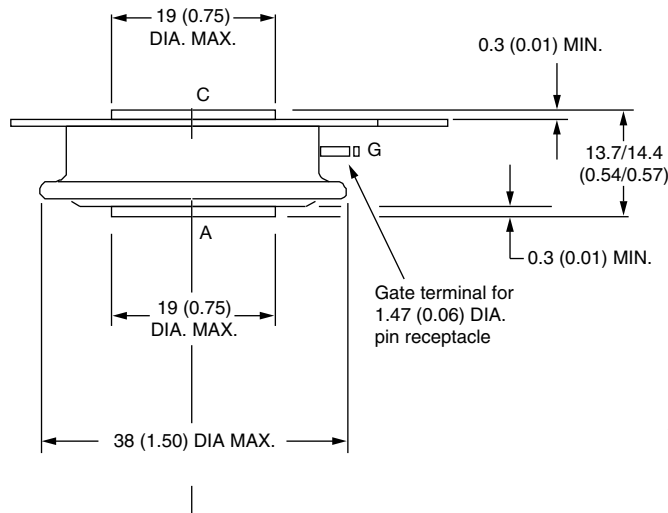




## A-PUK (TO-200AB)

### DIMENSIONS in millimeters (inches)

Anode to gate  
Creepage distance: 7.62 (0.30) minimum  
Strike distance: 7.12 (0.28) minimum



Quote between upper and lower pole pieces has to be considered after application of mounting force (see thermal and mechanical specification)



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