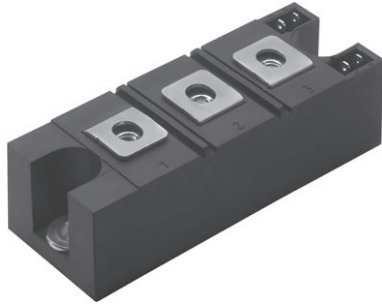



Thyristor/Thyristor, 150 A (INT-A-PAK Power Module)


INT-A-PAK

FEATURES

- Electrically isolated by DBC ceramic (Al_2O_3)
- 3500 V_{RMS} isolating voltage
- Industrial standard package
- High surge capability
- Glass passivated chips
- Simple mounting
- UL approved file E78996 
- Designed and qualified for multiple level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

PRIMARY CHARACTERISTICS

$I_{\text{T(AV)}}$	150 A
Type	Modules - thyristor, standard
Package	INT-A-PAK

APPLICATIONS

- Battery charges
- Welders
- Power converters

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{\text{T(AV)}}$	85 °C	150	A
$I_{\text{T(RMS)}}$		330	A
I_{TSM}	50 Hz	4000	
	60 Hz	4200	
I^2t	50 Hz	80	kA ² s
	60 Hz	73	
$I^2\sqrt{t}$		800	kA ² √s
$V_{\text{DRM}}/V_{\text{RRM}}$		400	V
T_{Stg}	Range	-40 to +150	°C
T_{J}	Range	-40 to +125	

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

TYPE NUMBER	$V_{\text{RRM}}/V_{\text{DRM}}$, MAXIMUM REPETITIVE PEAK REVERSE VOLTAGE V	$V_{\text{RSM}}/V_{\text{DSM}}$, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V	$I_{\text{RRM}}/I_{\text{DRM}}$ AT 125 °C mA
VS-VSKT152/04PbF	400	500	50



ON-STATE CONDUCTION					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average on-state current at case temperature	$I_{T(AV)}$	180° conduction half sine wave		150	A
				85	°C
Maximum RMS on-state current	$I_{T(RMS)}$	As AC switch		330	A
Maximum peak, one-cycle on-state, non-repetitive surge current	I_{TSM}	t = 10 ms	No voltage reapplied	4000	
		t = 8.3 ms		4200	
		t = 10 ms	100 % V_{RRM} reapplied	3350	
		t = 8.3 ms		3500	
Maximum I^2t for fusing	I^2t	t = 10 ms	No voltage reapplied	80	kA ² s
		t = 8.3 ms		73	
		t = 10 ms	100 % V_{RRM} reapplied	56	
		t = 8.3 ms		51	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 ms to 10 ms, no voltage reapplied		800	kA ² √s
Value of threshold voltage	$V_{T(TO)}$	T_J maximum		0.82	V
On-state slope resistance	r_t			1.44	mΩ
Maximum on-state voltage drop	V_{TM}	$I_{pk} = \pi \times I_{T(AV)}$, $T_J = 25\text{ °C}$		1.48	V
Maximum holding current	I_H	$T_J = 25\text{ °C}$, anode supply = 6 V, resistive load, gate open circuit		200	mA
Maximum latching current	I_L	$T_J = 25\text{ °C}$, anode supply = 6 V, resistive load		400	

SWITCHING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Typical delay time	t_{gd}	$T_J = 25\text{ °C}$	Gate current = 1 A, $di_g/dt = 1\text{ A}/\mu\text{s}$ $V_d = 0.67\% V_{DRM}$	1	μs
Typical rise time	t_{gr}			2	
Typical turn-off time	t_q	$I_{TM} = 300\text{ A}$, $-di/dt = 15\text{ A}/\mu\text{s}$; $T_J = T_J$ maximum $V_R = 50\text{ V}$; $dV/dt = 20\text{ V}/\mu\text{s}$; gate 0 V, 100 Ω		50 to 200	

BLOCKING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak reverse and off-state leakage current	I_{RRM} , I_{DRM}	$T_J = 125\text{ °C}$		50	mA
RMS insulation voltage	V_{INS}	50 Hz, circuit to base, all terminals shorted, t = 1 s		3500	V
Critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, exponential to 67 % rated V_{DRM}		1000	V/μs



TRIGGERING					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum peak gate power	P_{GM}	$t_p \leq 5$ ms, $T_J = T_J$ maximum		12	W
Maximum average gate power	$P_{G(AV)}$	$f = 50$ Hz, $T_J = T_J$ maximum		3	
Maximum peak gate current	I_{GM}	$t_p \leq 5$ ms, $T_J = T_J$ maximum		3	A
Maximum peak negative gate voltage	$-V_{GT}$			10	V
Maximum required DC gate voltage to trigger	V_{GT}	$T_J = -40$ °C	Anode supply = 6 V, resistive load; $R_a = 1$ Ω	4	
		$T_J = 25$ °C		2.5	
		$T_J = T_J$ maximum		1.7	
Maximum required DC gate current to trigger	I_{GT}	$T_J = -40$ °C		270	mA
		$T_J = 25$ °C		150	
		$T_J = T_J$ maximum		80	
Maximum gate voltage that will not trigger	V_{GD}	$T_J = T_J$ maximum, rated V_{DRM} applied		0.3	V
Maximum gate current that will not trigger	I_{GD}			10	mA
Maximum rate of rise of turned-on current	di/dt	$T_J = T_J$ maximum, $I_{TM} = 400$ A rated V_{DRM} applied		300	A/ μ s

THERMAL AND MECHANICAL SPECIFICATIONS				
PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction operating temperature range	T_J		-40 to +125	°C
Maximum storage temperature range	T_{Stg}		-40 to +150	
Maximum thermal resistance, junction to case per junction	R_{thJC}	DC operation	0.18	K/W
Maximum thermal resistance, case to heatsink per module	R_{thCS}	Mounting surface smooth, flat and greased	0.05	
Mounting torque ± 10 %	IAP to heatsink busbar to IAP	A mounting compound is recommended and the torque should be rechecked after a period of 3 hours to allow for the spread of the compound. Lubricated threads.	4 to 6	Nm
Approximate weight			200	g
			7.1	oz.
Case style			INT-A-PAK	

ΔR CONDUCTION PER JUNCTION											
DEVICES	SINUSOIDAL CONDUCTION AT T_J MAXIMUM					RECTANGULAR CONDUCTION AT T_J MAXIMUM					UNITS
	180°	120°	90°	60°	30°	180°	120°	90°	60°	30°	
VSKT152/04PbF	0.007	0.010	0.013	0.016	0.017	0.009	0.012	0.014	0.016	0.017	K/W

Note

- Table shows the increment of thermal resistance R_{thJC} when devices operate at different conduction angles than DC

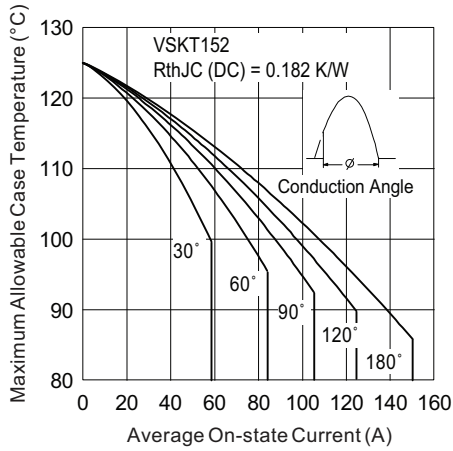


Fig. 1 - Current Ratings Characteristics

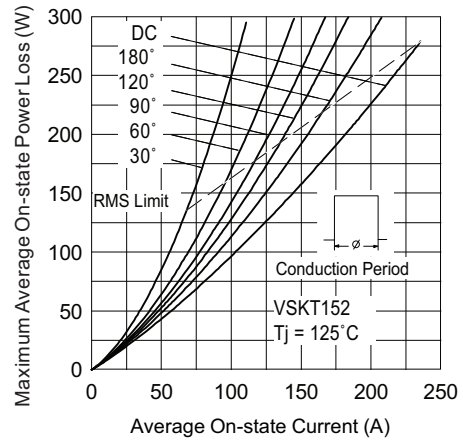


Fig. 4 - Forward Power Loss Characteristics

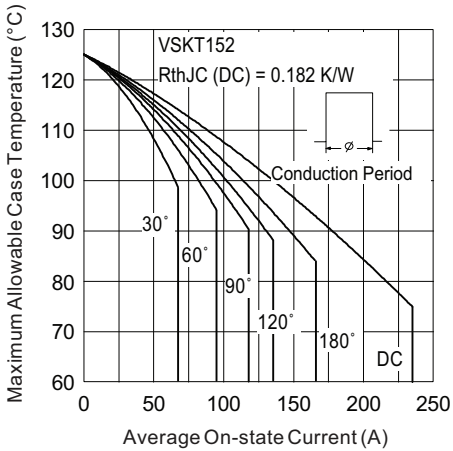


Fig. 2 - Current Ratings Characteristics

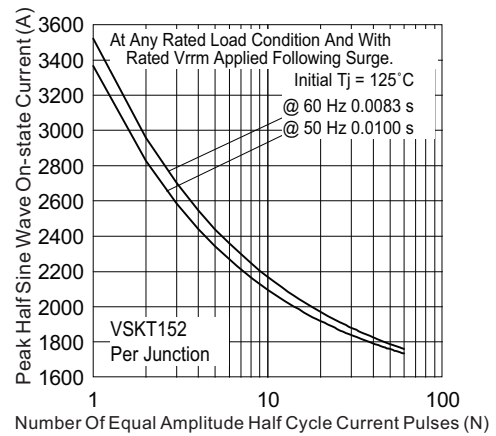


Fig. 5 - Maximum Non-Repetitive Surge Current

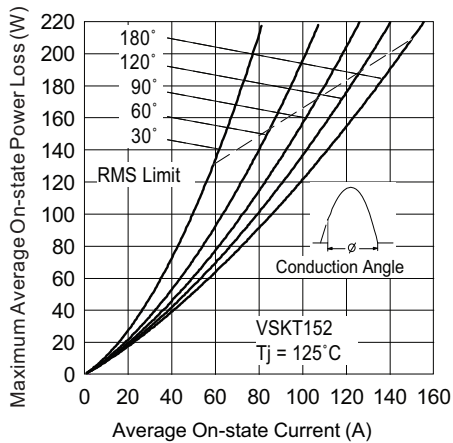


Fig. 3 - Forward Power Loss Characteristics

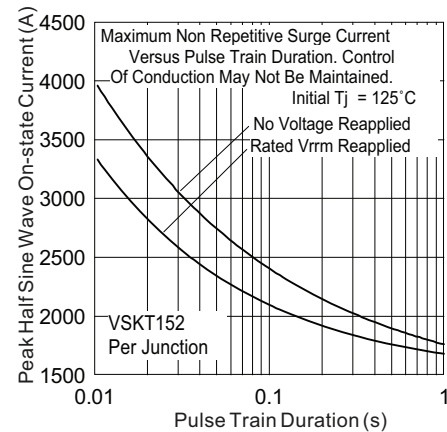


Fig. 6 - Maximum Non-Repetitive Surge Current

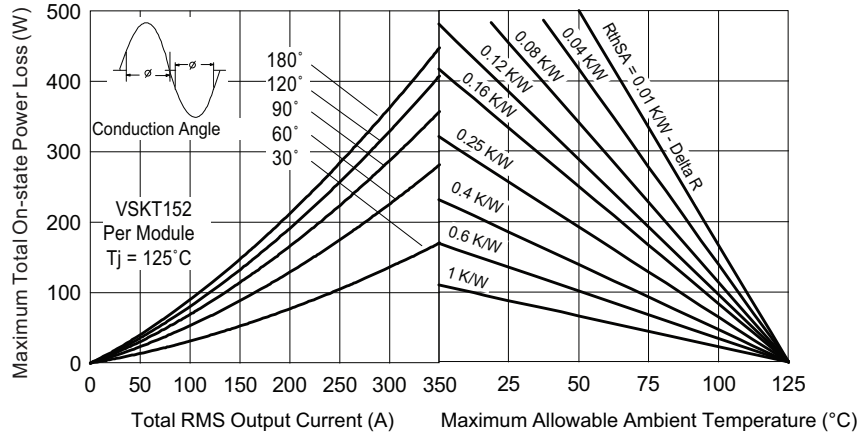


Fig. 7 - On-State Power Loss Characteristics

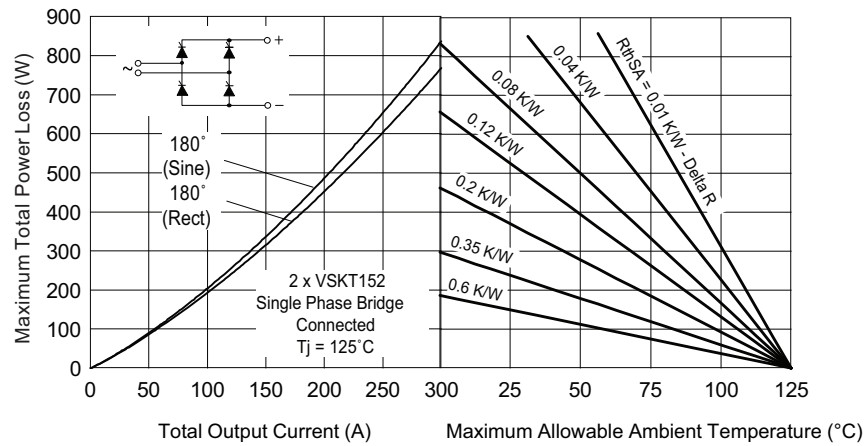


Fig. 8 - On-State Power Loss Characteristics

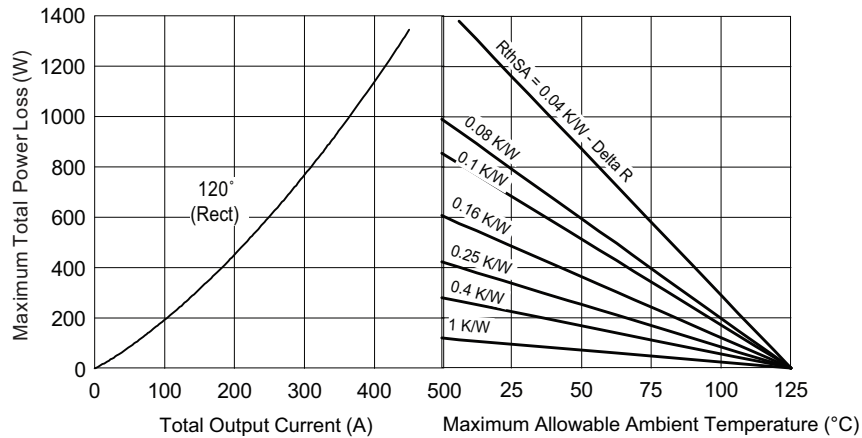


Fig. 9 - On-State Power Loss Characteristics

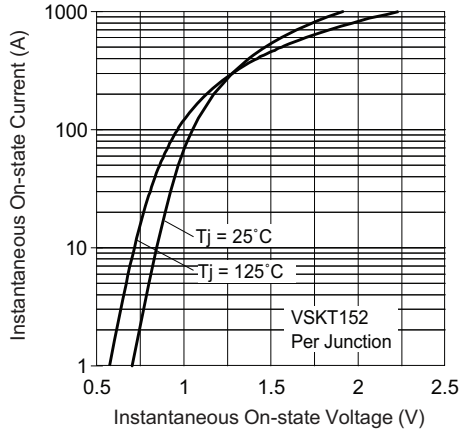


Fig. 10 - On-State Voltage Drop Characteristics

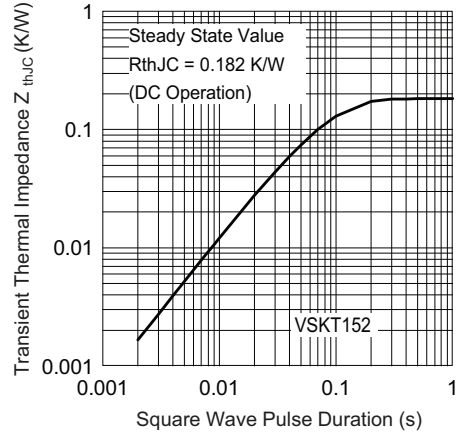


Fig. 11 - Thermal Impedance Z_{thJC} Characteristics

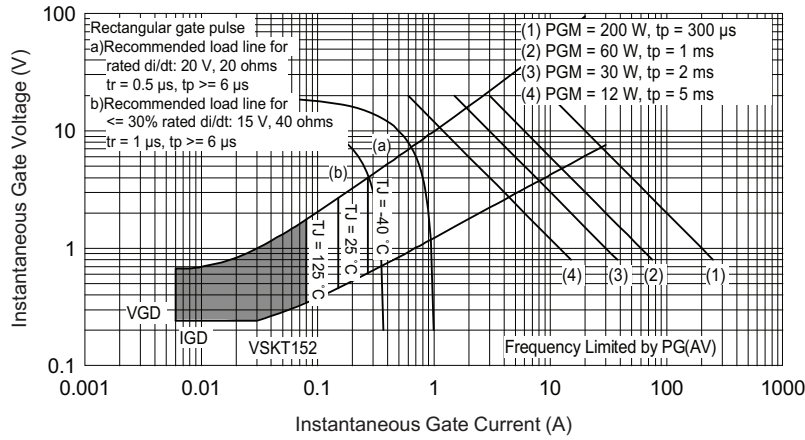


Fig. 12 - Gate Characteristics



ORDERING INFORMATION TABLE

Device code	VS-VS	KT	152	04	PbF
	①	②	③	④	⑤
	1	2	3	4	5
	- Vishay Semiconductors product	- Circuit configuration	- Current rating	- Voltage rating (04 = 400 V)	- PbF = Lead (Pb)-free

Note

- To order the optional hardware go to www.vishay.com/doc?95172

CIRCUIT CONFIGURATION		
CIRCUIT DESCRIPTION	CIRCUIT CONFIGURATION CODE	CIRCUIT DRAWING
Two SCRs doubler circuit	T	

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95067

INT-A-PAK IGBT/Thyristor

DIMENSIONS in millimeters (inches)





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