

NTMFS4985NF

MOSFET – Power, Single, N-Channel, SO-8 FL 30 V, 65 A

Features

- Integrated Schottky Diode
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb-Free and are RoHS Compliant

Applications

- CPU Power Delivery
- Synchronous Rectification for DC-DC Converters
- Low Side Switching
- Telecom Secondary Side Rectification

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

| Parameter | Symbol | Value | Unit |
|--|----------------|--------------------------|------------------|
| Drain-to-Source Voltage | V_{DSS} | 30 | V |
| Gate-to-Source Voltage | V_{GS} | ± 20 | V |
| Continuous Drain Current $R_{\theta JA}$ (Note 1) | I_D | $T_A = 25^\circ\text{C}$ | 23.9 |
| | | $T_A = 85^\circ\text{C}$ | 17.2 |
| Power Dissipation $R_{\theta JA}$ (Note 1) | P_D | 3.04 | W |
| Continuous Drain Current $R_{\theta JA} \leq 10$ sec | I_D | $T_A = 25^\circ\text{C}$ | 36 |
| | | $T_A = 85^\circ\text{C}$ | 26 |
| Power Dissipation $R_{\theta JA}, t \leq 10$ sec | P_D | 7.0 | W |
| Continuous Drain Current $R_{\theta JA}$ (Note 2) | I_D | $T_A = 25^\circ\text{C}$ | 17.5 |
| | | $T_A = 85^\circ\text{C}$ | 12.6 |
| Power Dissipation $R_{\theta JA}$ (Note 2) | P_D | 1.63 | W |
| Continuous Drain Current $R_{\theta JC}$ (Note 1) | I_D | $T_C = 25^\circ\text{C}$ | 65 |
| | | $T_C = 85^\circ\text{C}$ | 47 |
| Power Dissipation $R_{\theta JC}$ (Note 1) | P_D | 22.73 | W |
| Pulsed Drain Current | I_{DM} | 195 | A |
| Current limited by package | $I_{Dmaxpkg}$ | 100 | A |
| Operating Junction and Storage Temperature | T_J, T_{STG} | -55 to +150 | $^\circ\text{C}$ |
| Source Current (Body Diode) | I_S | 64 | A |
| Drain to Source dV/dt | dV/dt | 6 | V/ns |

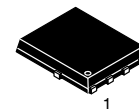
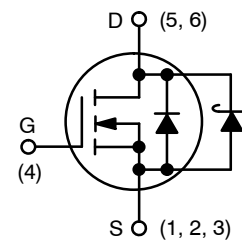


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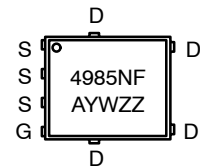
| $V_{(BR)DSS}$ | $R_{DS(ON)} \text{ MAX}$ | $I_D \text{ MAX}$ |
|---------------|--------------------------|-------------------|
| 30 V | 3.4 m Ω @ 10 V | 65 A |
| | 5.0 m Ω @ 4.5 V | |

N-CHANNEL MOSFET



SO-8 FLAT LEAD
CASE 488AA
STYLE 1

MARKING DIAGRAM



4895NF = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

| Device | Package | Shipping† |
|----------------|------------------|--------------------|
| NTMFS4985NFT1G | SO-8FL (Pb-Free) | 1500 / Tape & Reel |
| NTMFS4985NFT3G | SO-8FL (Pb-Free) | 5000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

| Parameter | Symbol | Value | Unit |
|---|--------|-------|------------------|
| Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 50\text{ V}$, $V_{GS} = 10\text{ V}$, $I_L = 33\text{ A}_{pk}$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$) | EAS | 54 | mJ |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | T_L | 260 | $^\circ\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|------|
| Junction-to-Case (Drain) | $R_{\theta JC}$ | 5.5 | °C/W |
| Junction-to-Ambient – Steady State (Note 1) | $R_{\theta JA}$ | 41.15 | |
| Junction-to-Ambient – Steady State (Note 2) | $R_{\theta JA}$ | 76.9 | |
| Junction-to-Ambient – $t \leq 10$ sec | $R_{\theta JA}$ | 17.86 | |

1. Surface-mounted on FR4 board using 1 sq-in pad, 2 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size of 100 mm².

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|-------------------|--|----|----|-----------|---------------|
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 1.0\text{ mA}$ | 30 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | $I_D = 10\text{ mA}$, referenced to 25°C | | 15 | | mV/°C |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$ $T_J = 25^\circ\text{C}$ | | | 500 | μA |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$ | | | ± 100 | nA |

ON CHARACTERISTICS (Note 3)

| | | | | | | | |
|--|------------------|---|---------------------|-----|-----|-------|------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = 1.0\text{ mA}$ | 1.2 | 1.6 | 2.3 | V | |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | $I_D = 10\text{ mA}$, referenced to 25°C | | 5.0 | | mV/°C | |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 30\text{ A}$ | | 2.7 | 3.4 | m Ω |
| | | | $I_D = 15\text{ A}$ | | 2.7 | | |
| | | $V_{GS} = 4.5\text{ V}$ | $I_D = 30\text{ A}$ | | 4.0 | 5.0 | |
| | | | $I_D = 15\text{ A}$ | | 4.0 | | |
| Forward Transconductance | g_{FS} | $V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$ | | 43 | | S | |

CHARGES AND CAPACITANCES

| | | | | | | |
|------------------------------|--------------|--|---|------|------|----|
| Input Capacitance | C_{ISS} | $V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$ | | 2100 | | pF |
| Output Capacitance | C_{OSS} | | | 900 | | |
| Reverse Transfer Capacitance | C_{RSS} | | | 60 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$ | | 14.2 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | 1.8 | | |
| Gate-to-Source Charge | Q_{GS} | | | 5.9 | | |
| Gate-to-Drain Charge | Q_{GD} | | | 4.2 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | | $V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$ | | 30.5 | |

SWITCHING CHARACTERISTICS (Note 4)

| | | | | | | |
|---------------------|--------------|---|--|-----|--|----|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$ | | 11 | | ns |
| Rise Time | t_r | | | 32 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 21 | | |
| Fall Time | t_f | | | 6.0 | | |

3. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
4. Switching characteristics are independent of operating junction temperatures.

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ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|--------------|---|-----|------|-----|------|
| SWITCHING CHARACTERISTICS (Note 4) | | | | | | |
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$ | | 8.5 | | ns |
| Rise Time | t_r | | | 26.5 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 26 | | |
| Fall Time | t_f | | | 4.5 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|----------|--|---------------------------|------|------|-----|---|
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0\text{ V},$ $I_S = 2\text{ A}$ | $T_J = 25^\circ\text{C}$ | | 0.4 | 0.7 | V |
| | | | $T_J = 125^\circ\text{C}$ | | 0.33 | | |
| Reverse Recovery Time | t_{RR} | $V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 2\text{ A}$ | | 36.5 | | ns | |
| Charge Time | t_a | | | 18 | | | |
| Discharge Time | t_b | | | 18.5 | | | |
| Reverse Recovery Charge | Q_{RR} | | | 32 | | nC | |

PACKAGE PARASITIC VALUES

| | | | | | | |
|-------------------|-------|--------------------------|--|------|--|----|
| Source Inductance | L_S | $T_A = 25^\circ\text{C}$ | | 0.65 | | nH |
| Drain Inductance | L_D | | | 0.20 | | |
| Gate Inductance | L_G | | | 1.5 | | |
| Gate Resistance | R_G | | | 1.0 | | |

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

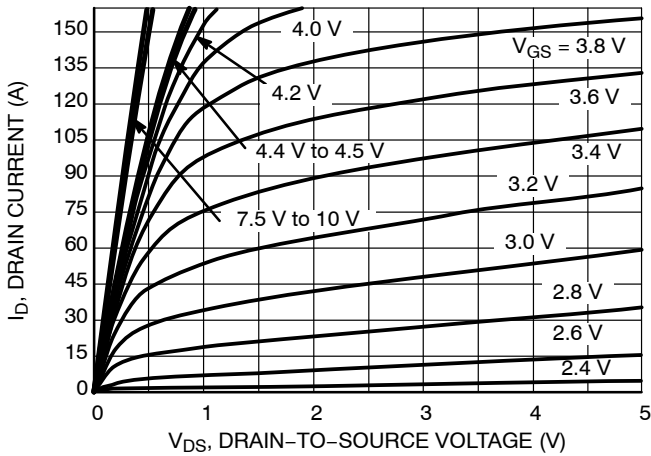


Figure 1. On-Region Characteristics

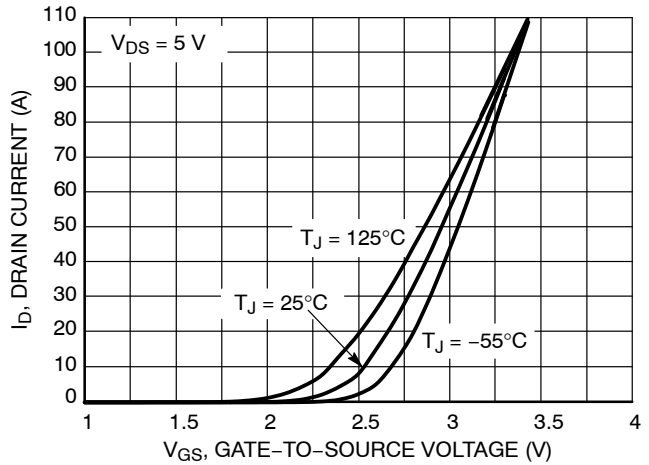


Figure 2. Transfer Characteristics

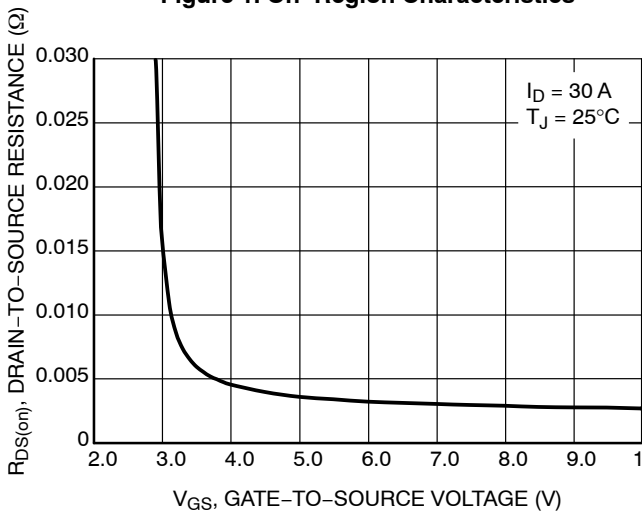


Figure 3. On-Resistance vs. Gate-to-Source Voltage

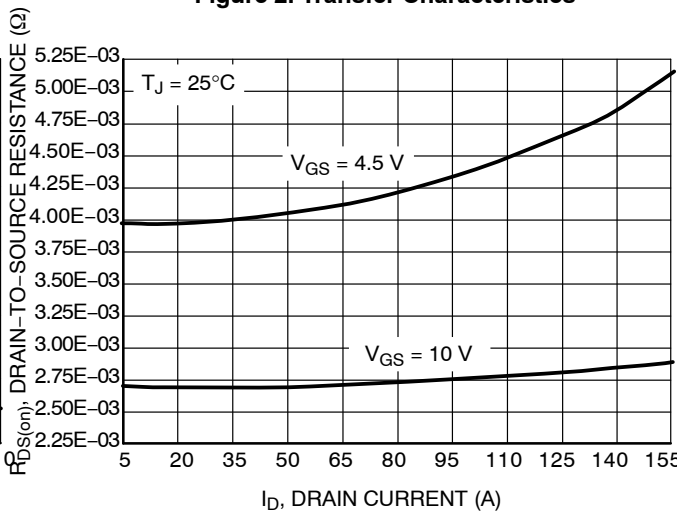


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

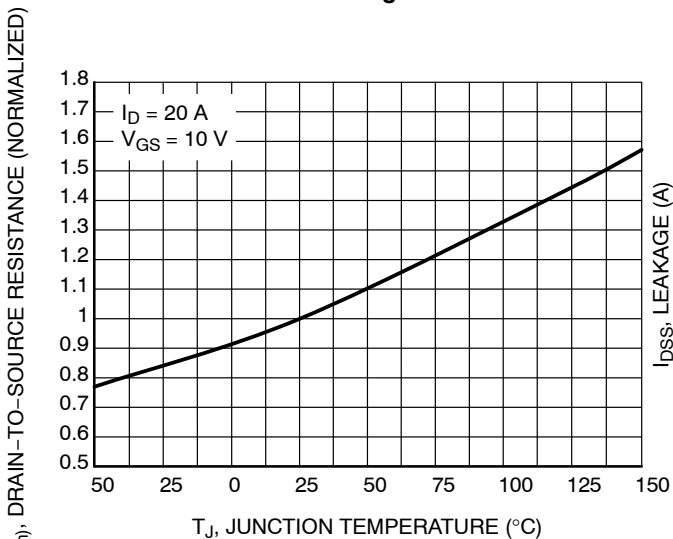


Figure 5. On-Resistance Variation with Temperature

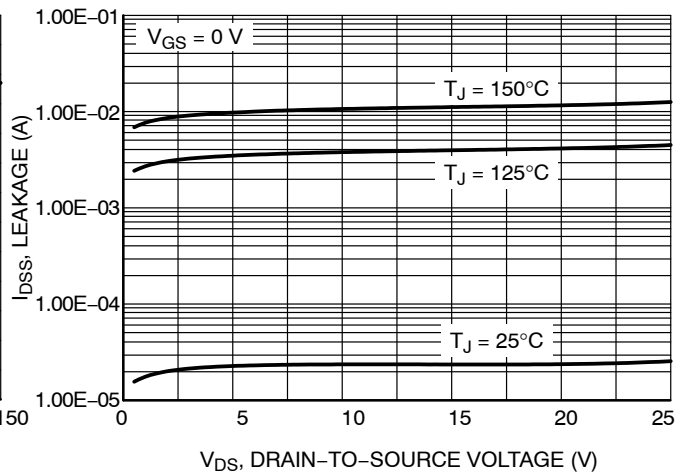


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

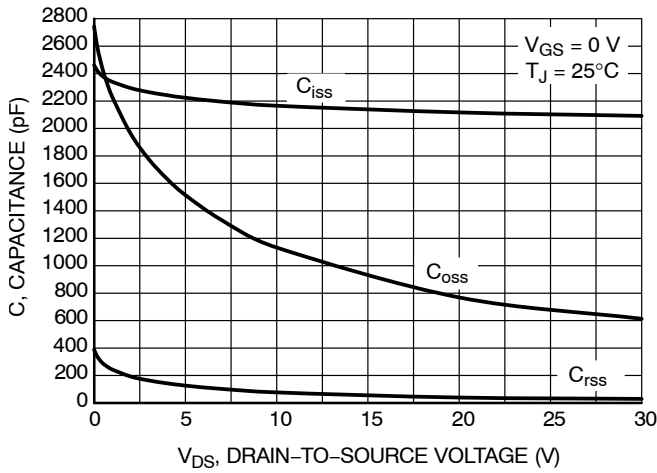


Figure 7. Capacitance Variation

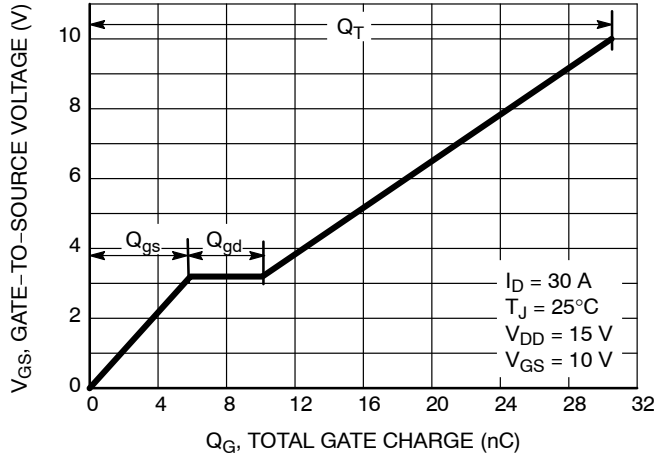


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

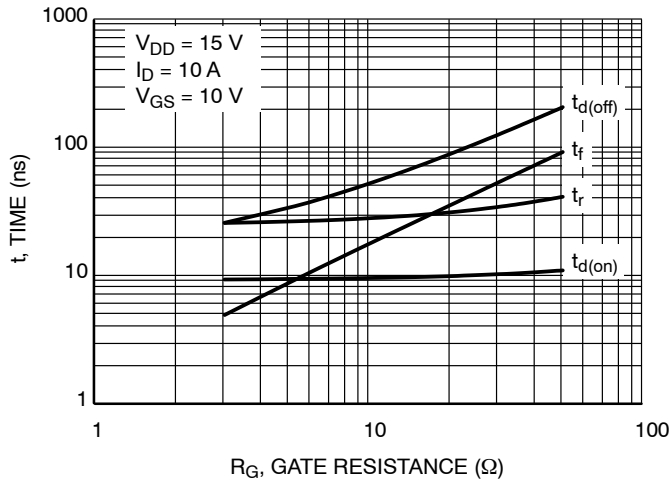


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

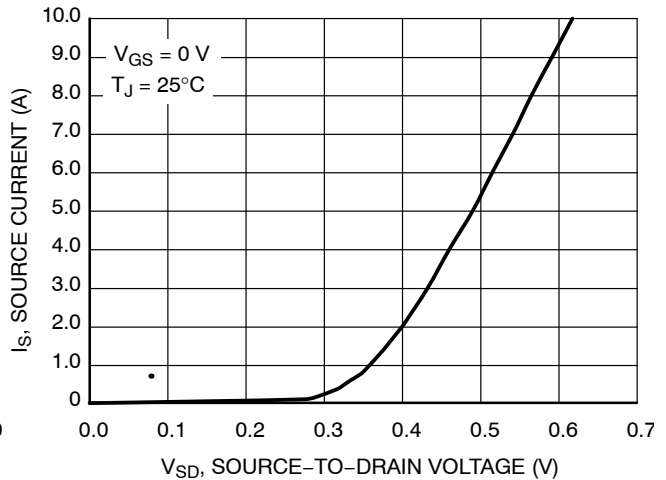


Figure 10. Diode Forward Voltage vs. Current

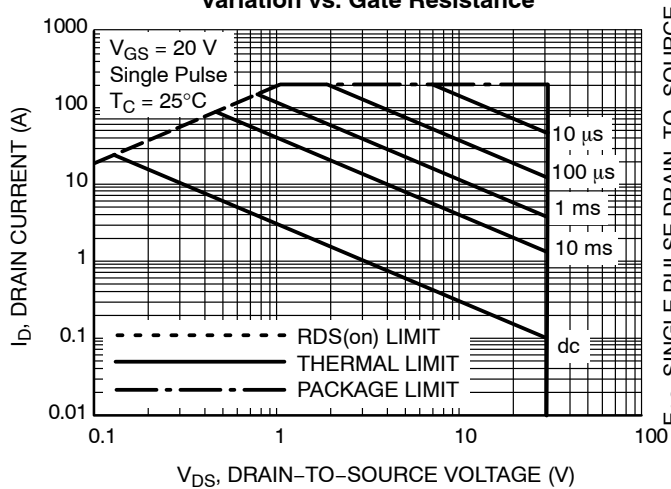


Figure 11. Maximum Rated Forward Biased Safe Operating Area

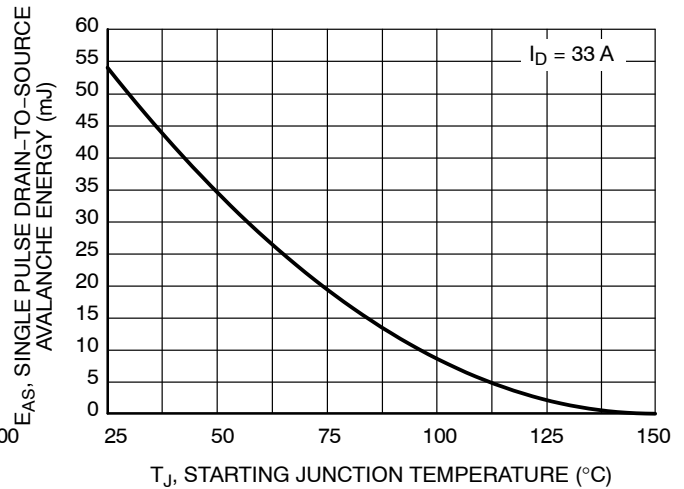


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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TYPICAL PERFORMANCE CURVES

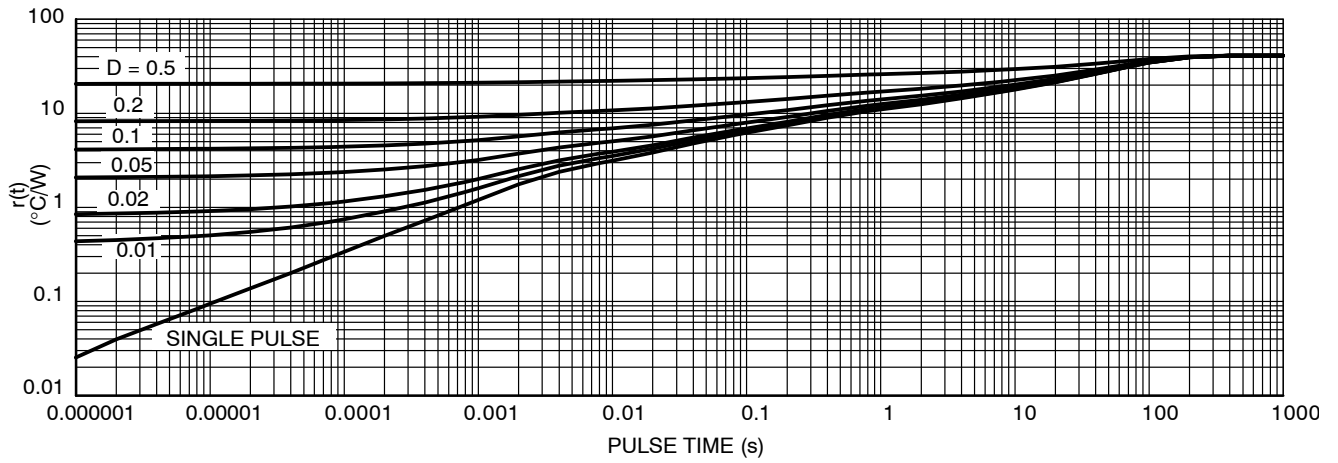
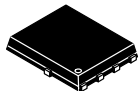


Figure 13. Thermal Response

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

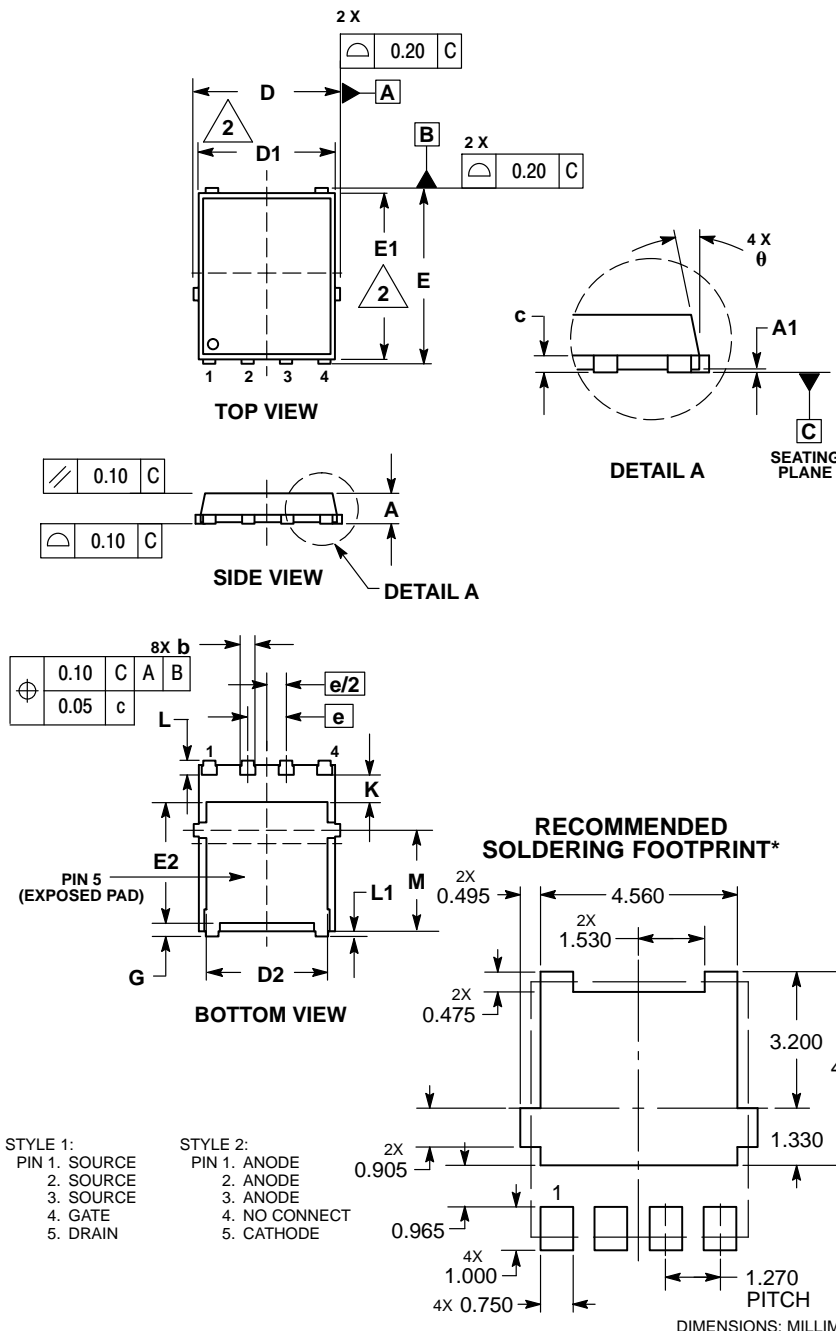
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SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

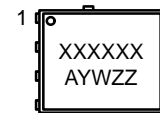


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

| MILLIMETERS | | | |
|-------------|-----------|-------|------|
| DIM | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | --- | 0.05 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.23 | 0.28 | 0.33 |
| D | 5.00 | 5.15 | 5.30 |
| D1 | 4.70 | 4.90 | 5.10 |
| D2 | 3.80 | 4.00 | 4.20 |
| E | 6.00 | 6.15 | 6.30 |
| E1 | 5.70 | 5.90 | 6.10 |
| E2 | 3.45 | 3.65 | 3.85 |
| e | 1.27 BSC | | |
| G | 0.51 | 0.575 | 0.71 |
| K | 1.20 | 1.35 | 1.50 |
| L | 0.51 | 0.575 | 0.71 |
| L1 | 0.125 REF | | |
| M | 3.00 | 3.40 | 3.80 |
| θ | 0° | --- | 12° |

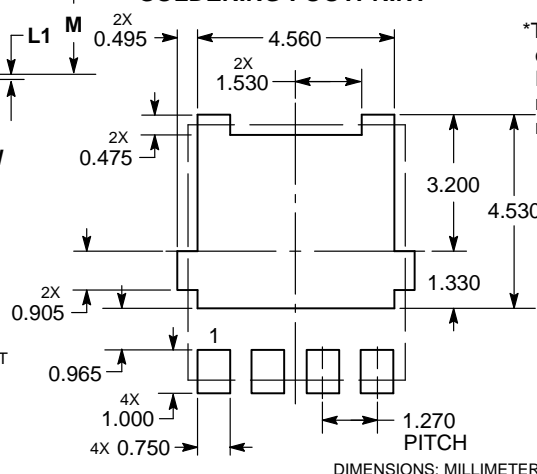
GENERIC MARKING DIAGRAM*



- XXXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*



- STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
- STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|------------------|--------------------------|--|
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| DESCRIPTION: | DFN5 5x6, 1.27P (SO-8FL) | PAGE 1 OF 1 |

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