

# $\mu$ PA2813T1L

P-channel MOSFET

-30 V, -27 A, 6.2 mΩ

R07DS0763EJ0102 Rev.1.02 May. 28, 2013

# **Description**

The  $\mu$ PA2813T1L is P-channel MOS Field Effect Transistor designed for DC/DC converter and power management applications of portable equipment.

## **Features**

- $V_{DSS} = -30 \text{ V } (T_A = 25^{\circ}\text{C})$
- Low on-state resistance
  - R<sub>DS(on)</sub> = 6.2 mΩ MAX. (V<sub>GS</sub> = -10 V, I<sub>D</sub> = -27 A)
- 4.5 V Gate-drive available
- Small & thin type surface mount package with heat spreader
- Pb-free and Halogen free



8-pin HVSON(3333)

## **Ordering Information**

Part No.	Lead Plating	Packing	Package
μPA2813T1L-E2-AT *1	Pure Sn	Tape 3000 p/reel	8-pin HVSON (3333)
			typ. 0.028 g

Note: \*1. Pb-free (This product does not contain Pb in external electrode and other parts.)

## Absolute Maximum Ratings $(T_A = 25^{\circ}C)$

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V <sub>GS</sub> = 0 V)	$V_{DSS}$	-30	V
Gate to Source Voltage (V <sub>DS</sub> = 0 V)	$V_{GSS}$	∓20	V
Drain Current (DC) (T <sub>C</sub> = 25°C)	I <sub>D(DC)</sub>	∓27	Α
Drain Current (pulse) *1	I <sub>D(pulse)</sub>	∓108	Α
Total Power Dissipation *2	P <sub>T1</sub>	1.5	W
Total Power Dissipation (PW = 10 sec) *2	P <sub>T2</sub>	3.8	W
Total Power Dissipation (T <sub>C</sub> = 25°C)	P <sub>T3</sub>	52	W
Channel Temperature	T <sub>ch</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	−55 to +150	°C
Single Avalanche Current *3	I <sub>AS</sub>	23	Α
Single Avalanche Energy *3	E <sub>AS</sub>	54	mJ

## **Thermal Resistance**

Channel to Ambient Thermal Resistance  $^{*2}$   $R_{th(ch-A)}$  83.3 °C/W Channel to Case (Drain) Thermal Resistance  $R_{th(ch-C)}$  2.4 °C/W

Notes: \*1. PW  $\leq$  10  $\mu$ s, Duty Cycle  $\leq$  1%

\*2. Mounted on a glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mmt

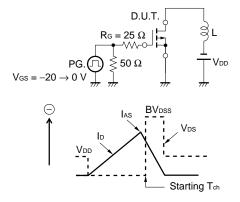
\*3. Starting  $T_{ch}$  = 25°C,  $V_{DD}$  = -15 V,  $R_G$  = 25  $\Omega$ ,  $V_{GS}$  = -20  $\rightarrow$  0 V, L = 100  $\mu H$ 

# Electrical Characteristics (T<sub>A</sub> = 25°C)

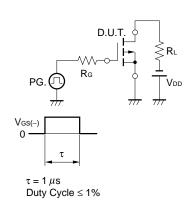
Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			-1	μΑ	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$
Gate Leakage Current	I <sub>GSS</sub>			∓100	nA	$V_{GS} = \mp 20 \text{ V}, V_{DS} = 0 \text{ V}$
Gate Cut-off Voltage	$V_{GS(off)}$	-1.0		-2.5	V	$V_{DS} = -10 \text{ V}, I_{D} = -1 \text{ mA}$
Forward Transfer Admittance *1	y <sub>fs</sub>	8.0			S	$V_{DS} = -10 \text{ V}, I_{D} = -13.5 \text{ A}$
Drain to Source On-state	R <sub>DS(on)1</sub>		4.8	6.2	mΩ	$V_{GS} = -10 \text{ V}, I_D = -27 \text{ A}$
Resistance *1	R <sub>DS(on)2</sub>		9	13	mΩ	$V_{GS} = -4.5 \text{ V}, I_D = -13.5 \text{ A}$
Input Capacitance	C <sub>iss</sub>		3130		pF	$V_{DS} = -10 \text{ V},$
Output Capacitance	Coss		1490		pF	$V_{GS} = 0 V$ ,
Reverse Transfer Capacitance	C <sub>rss</sub>		1290		pF	f = 1 MHz
Turn-on Delay Time	t <sub>d(on)</sub>		16		ns	$V_{DD} = -15 \text{ V}, I_D = -13.5 \text{ A},$
Rise Time	t <sub>r</sub>		41		ns	$V_{GS} = -10 \text{ V},$
Turn-off Delay Time	$t_{d(off)}$		196		ns	$R_G = 10 \Omega$
Fall Time	t <sub>f</sub>		234		ns	
Total Gate Charge	$Q_G$		80		nC	V <sub>DD</sub> = -24 V,
Gate to Source Charge	$Q_{GS}$		9		nC	$V_{GS} = -10 \text{ V},$
Gate to Drain Charge	$Q_{GD}$		42		nC	I <sub>D</sub> = -27 A
Body Diode Forward Voltage *1	$V_{F(S-D)}$		0.9		V	I <sub>F</sub> = 27 A, V <sub>GS</sub> = 0 V
Reverse Recovery Time	t <sub>rr</sub>		173		ns	I <sub>F</sub> = 27 A, V <sub>GS</sub> = 0 V,
Reverse Recovery Charge	Q <sub>rr</sub>		270		nC	di/dt = 100 A/μs

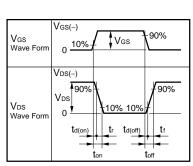
Note: \*1. Pulsed

## **TEST CIRCUIT 1 AVALANCHE CAPABILITY**



## **TEST CIRCUIT 2 SWITCHING TIME**



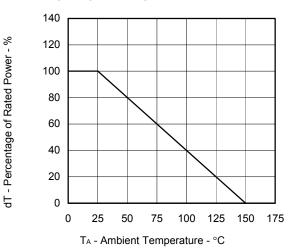


## **TEST CIRCUIT 3 GATE CHARGE**

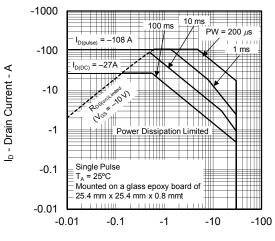
$$\begin{array}{c|c} D.U.T. \\ \hline \\ IG = -2 \text{ mA} \\ \hline \\ \hline \\ PG. \\ \hline \\ \end{array}$$

# Typical Characteristics ( $T_A = 25^{\circ}C$ )

DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

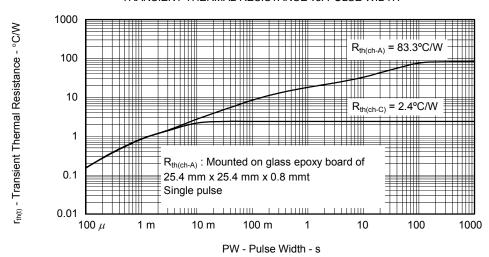


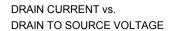
#### FORWARD BIAS SAFE OPERATING AREA

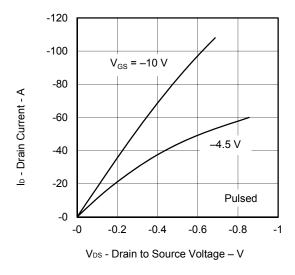


VDS - Drain to Source Voltage - V

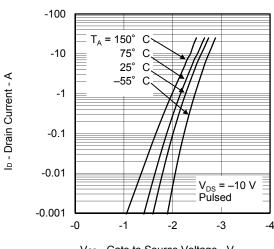
#### TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH







### FORWARD TRANSFER CHARACTERISTICS



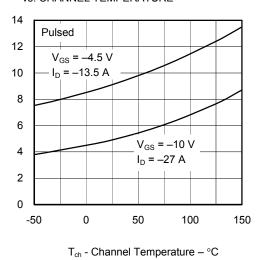
 $V_{\text{GS}}$  - Gate to Source Voltage - V

## GATE CUT-OFF VOLTAGE vs.CHANNEL **TEMPERATURE** -3 $V_{\text{GS(th)}}$ - Gate to Source Threshold Voltage - V-2 -1 Pulsed $V_{DS} = -10 V$ $I_D = -1 \text{ mA}$ -0 -50 0 50 100 150 Tch - Channel Temperature - °C

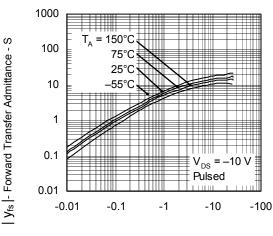
# DRAIN TO SOURCE ON-STATE RESISTANCE vs.

# DRAIN CURRENT To pour to provide the series of the series

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

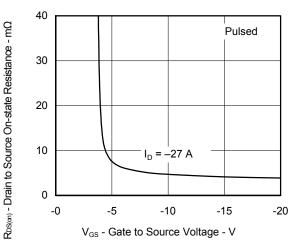


# FORWARD TRANSFER ADMITANCE vs. DRAIN CURRENT

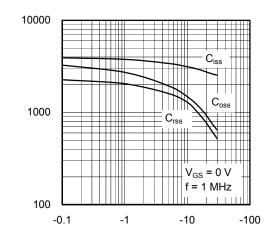


ID - Drain Current - A

# DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



#### CAPACITANCE vs. DRAIN TOSOURCE VOLTAGE

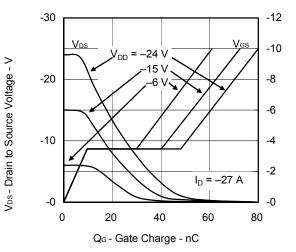


V<sub>DS</sub> - Drain to Source Voltage - V

 $R_{\text{DS(on)}}$  - Drain to Source On-state Resistance -  $m\Omega$ 

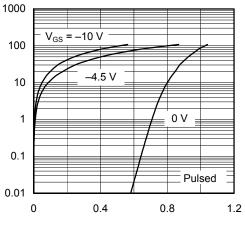
Ciss, Coss, Crss - Capacitance - pF

## DYNAMIC INPUT/OUTPUT CHARACTERISTICS



Vos - Gate to Source Voltage - V

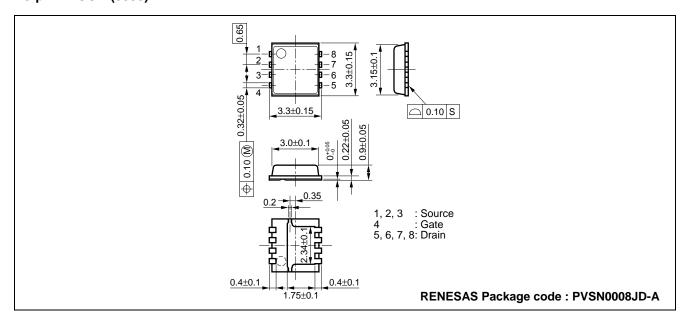
## SOURCE TO DRAIN DIODE FORWARD VOLTAGE



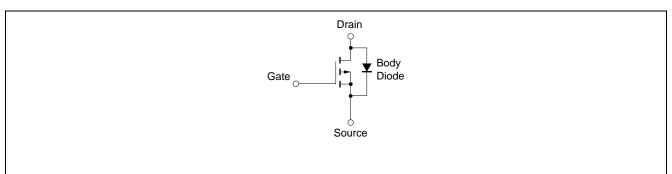
V<sub>F(S-D)</sub> - Source to Drain Voltage - V

# Package Drawings (Unit: mm)

## 8-pin HVSON (3333)



## **Equivalent Circuit**



**Remark** Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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