IXYS

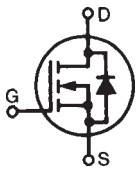
PolarHV™ HiPerFET Power MOSFET ISOPLUS247™

(Electrically Isolated Back Surface)

IXFR 180N15P

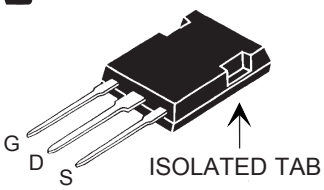
N-Channel Enhancement Mode
Avalanche Rated
Fast Intrinsic Diode

V_{DSS} = 150 V
I_{D25} = 100 A
$R_{DS(on)}$ ≤ 13 mΩ
t_{rr} ≤ 200 ns



Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25° C to 175° C	150	V
V_{DGR}	T_J = 25° C to 175° C; R_{GS} = 1 MΩ	150	V
V_{GSS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_C = 25° C	100	A
$I_{D(RMS)}$	External Lead current limit	75	A
I_{DM}	T_C = 25° C, pulse width limited by T_{JM}	380	A
I_{AR}	T_C = 25° C	60	A
E_{AR}	T_C = 25° C	100	mJ
E_{AS}	T_C = 25° C	4	J
dv/dt	$I_S \le I_{DM}$, di/dt ≤100 A/μs, $V_{DD} \le V_{DSS}$, T_J ≤150° C, R_G = 4 Ω	10	V/ns
P_D	T_C = 25° C	300	W
T_J		-55 ... +175	°C
T_{JM}		175	°C
T_{stg}		-55 ... +150	°C
T_L	1.6 mm (0.062 in.) from case for 10 s	300	°C
V_{ISOL}	50/60 Hz, RMS, 1 minute	2500	V~
F_d	Mounting force	20..120 / 4.5..26	N/lb
Weight		5	g

ISOPLUS247 (IXFR)
E153432



G = Gate D = Drain
S = Source

Symbol (T_J = 25° C, unless otherwise specified)	Test Conditions	Characteristic Values Min.	Typ.	Max.	
V_{DSS}	V_{GS} = 0 V, I_D = 250 μA	150			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 4 mA	2.5		5.0	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±100	nA
I_{DSS}	$V_{DS} = V_{DSS}$, V_{GS} = 0 V			25	μA
	T_J = 150° C			1.5	mA
$R_{DS(on)}$	V_{GS} = 10 V, $I_D = I_T$, Note 1			13	mΩ

Features

- International standard isolated package
- UL recognized package
- Silicon chip on Direct-Copper-Bond substrate
  - High power dissipation
  - Isolated mounting surface
  - 2500V electrical isolation
- Unclamped Inductive Switching (UIS) rated
- Low package inductance
  - easy to drive and to protect
- Fast intrinsic diode

Advantages

- Easy to mount
- Space savings
- High power density

Symbol	Test Conditions (T_J = 25° C, unless otherwise specified)	Characteristic Values Min.	Typ.	Max.	
g_{fs}	V_{DS} = 10 V; I_D = I_T, Notes 1, 2	55	86		S
C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		7000		pF
C_{oss}			2250		pF
C_{rss}			515		pF
$t_{d(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = 60A R_G = 3.3 Ω (External)		30		ns
t_r			32		ns
$t_{d(off)}$			150		ns
t_f			36		ns
$Q_{g(on)}$	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS}, I_D = I_T		240		nC
Q_{gs}			55		nC
Q_{gd}			140		nC
R_{thJC}				0.5	°C/W
R_{thCS}			0.15		°C/W

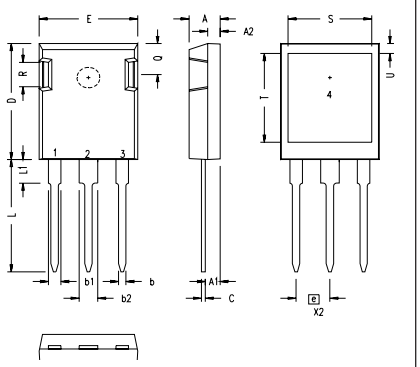
Source-Drain Diode

Symbol	Test Conditions (T_J = 25° C, unless otherwise specified)	Characteristic Values min.	typ.	max.	
I_S	V_{GS} = 0 V			180	A
I_{SM}	Repetitive			380	A
V_{SD}	I_F = I_S, V_{GS} = 0 V, Note 1			1.5	V
t_{rr}	I_F = 25A, -di/dt = 100 A/μs			200	ns
Q_{RM}	V_R = 100V, V_{GS} = 0V		0.6		μC
I_{RM}			6		A

Notes:

1. Pulse test, t ≤300 μs, duty cycle d ≤ 2 %;
2. Test current I_T = 90 A.

ISOPLUS247 Outline



SYM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b1	.075	.084	1.91	2.13
b2	.115	.123	2.92	3.12
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
E	.620	.635	15.75	16.13
e	.215 BSC		5.45 BSC	
L	.780	.800	19.81	20.32
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83
S	.520	.540	13.21	13.72
T	.620	.640	15.75	16.26
U	.065	.080	1.65	2.03

1 – GATE
2 – DRAIN (COLLECTOR)
3 – SOURCE (EMITTER)
4 – NO CONNECTION

NOTE: This drawing will meet all dimensions requirement of JEDEC outline TO-247AD except screw hole.

Fig. 1. Output Characteristics @ 25ºC

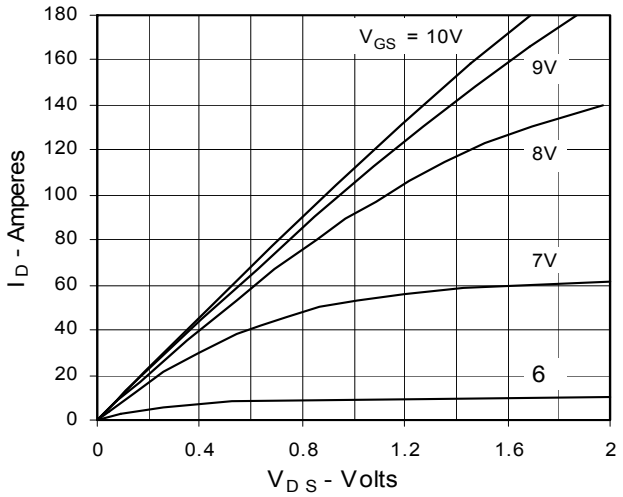


Fig. 2. Extended Output Characteristics @ 25ºC

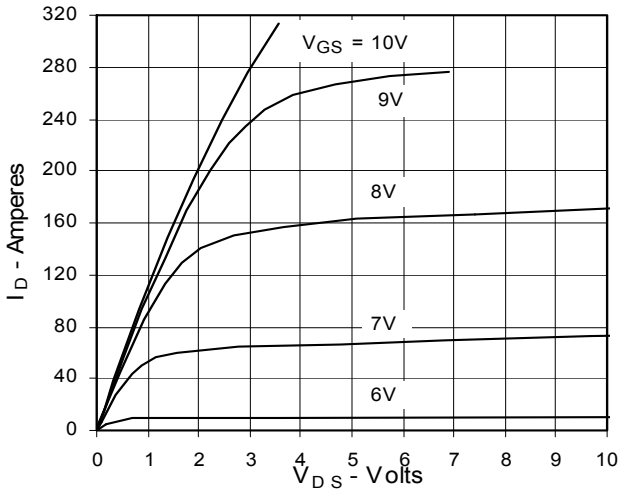


Fig. 3. Output Characteristics @ 150ºC

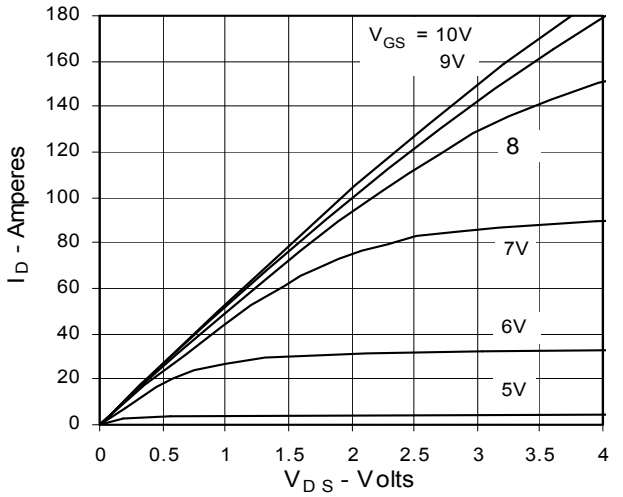


Fig. 4. $R_{DS(on)}$ Normalized to I_D = 90A Value vs. Junction Temperature

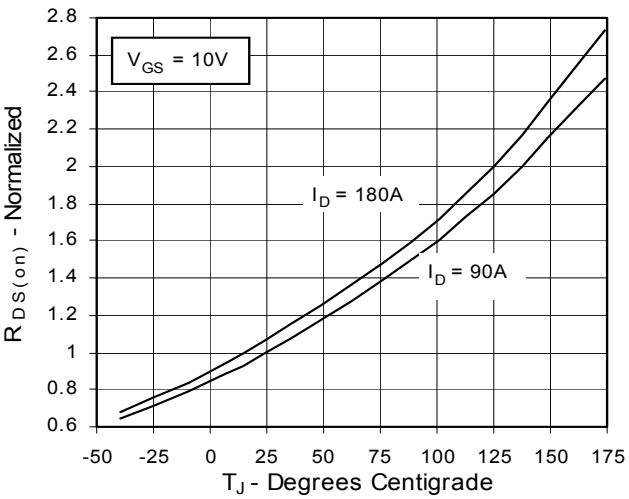


Fig. 5. $R_{DS(on)}$ Normalized to I_D = 90A Value vs. Drain Current

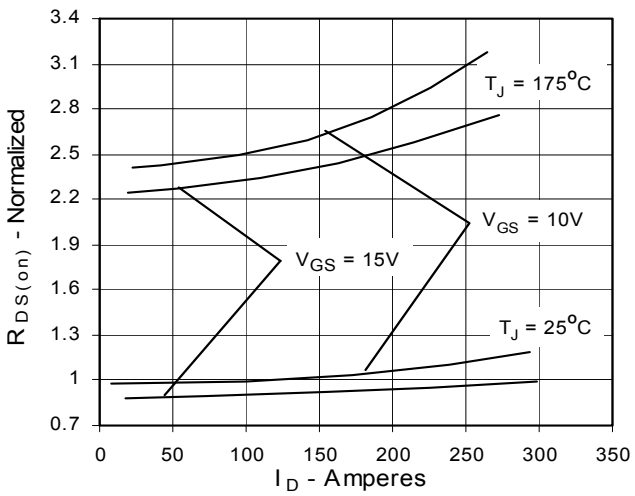


Fig. 6. Drain Current vs. Case Temperature

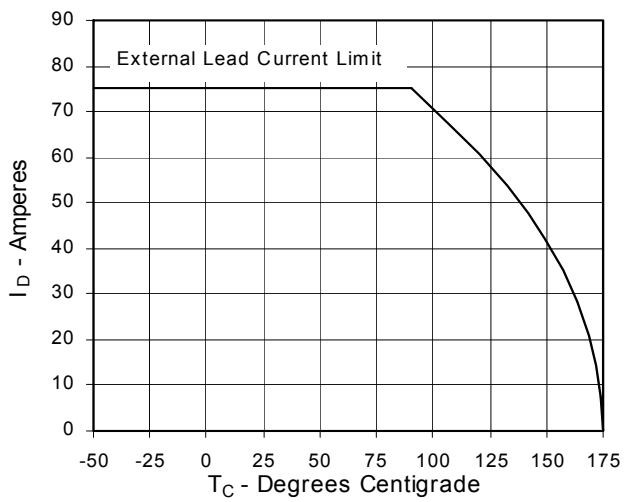


Fig. 7. Input Admittance

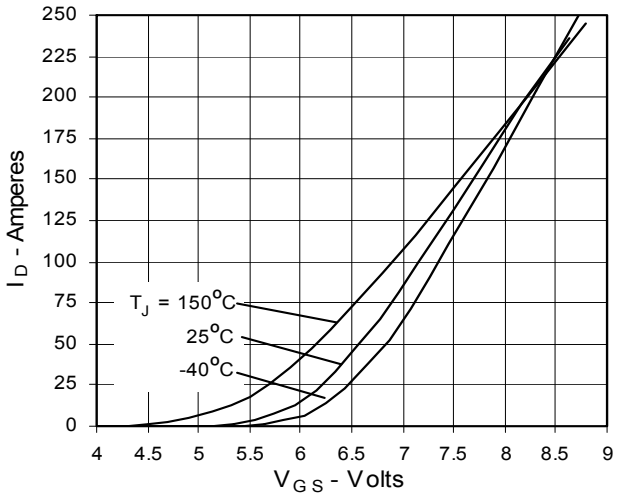


Fig. 8. Transconductance

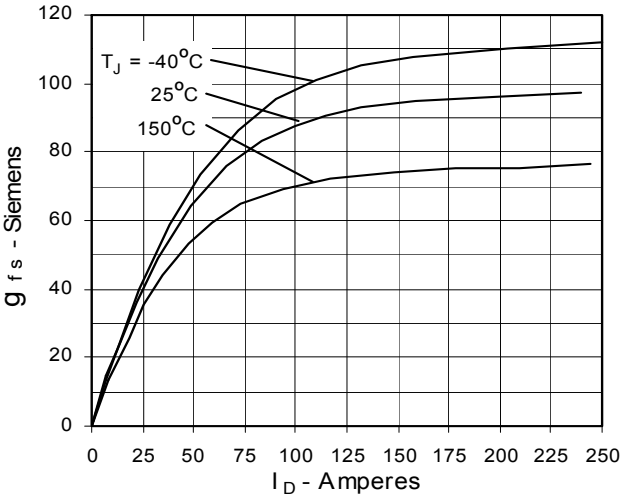


Fig. 9. Source Current vs. Source-To-Drain Voltage

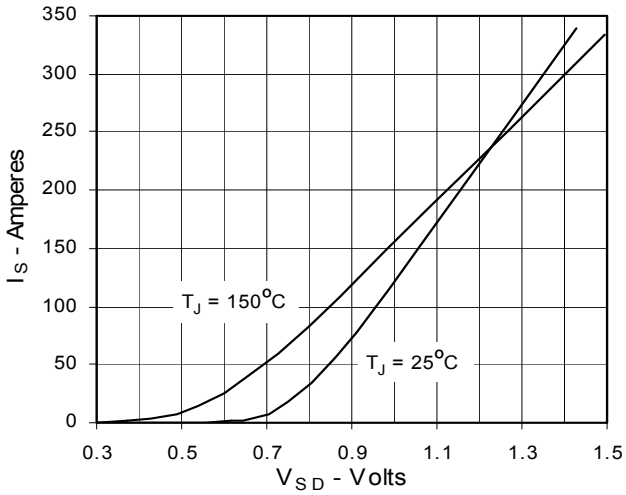


Fig. 10. Gate Charge

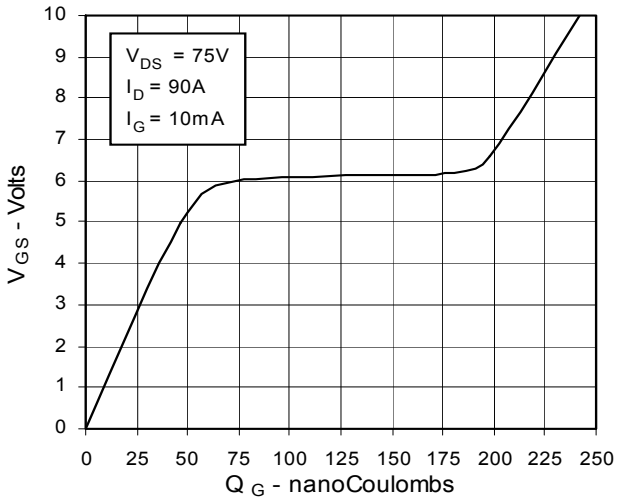


Fig. 11. Capacitance

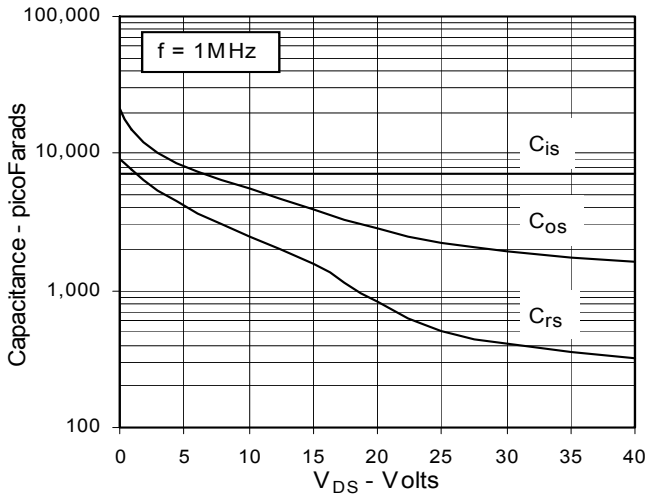


Fig. 12. Forward-Bias Safe Operating Area

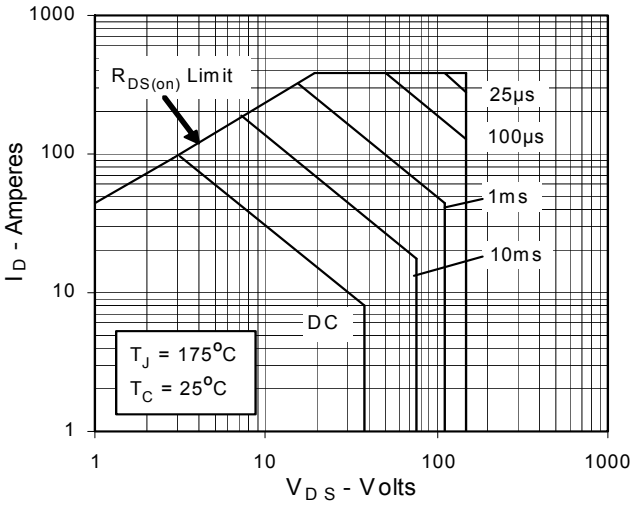


Fig. 13. Maximum Transient Thermal Resistance