

# IRFBA1404PPbF

HEXFET® Power MOSFET

## Typical Applications

- Industrial Motor Drive

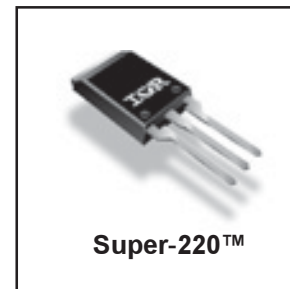
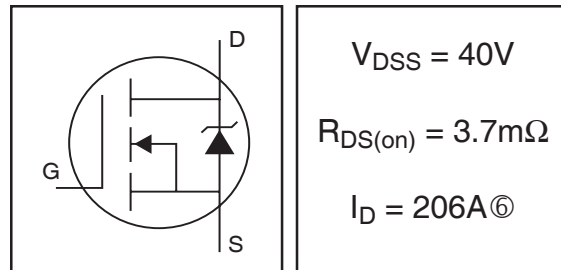
## Benefits

- Advanced Process Technology
- Ultra Low On-Resistance
- Increase Current Handling Capability
- 175°C Operating Temperature
- Fast Switching
- Dynamic dv/dt Rating
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free

## Description

This Stripe Planar design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this MOSFET are a 175°C junction operating temperature, fast switching speed and improved ruggedness in single and repetitive avalanche. The Super-220™ is a package that has been designed to have the same mechanical outline and pinout as the industry standard TO-220 but can house a considerably larger silicon die. The result is significantly increased current handling capability over both the TO-220 and the much larger TO-247 package. The combination of extremely low on-resistance silicon and the Super-220™ package makes it ideal to reduce the component count in multiparalleled TO-220 applications, reduce system power dissipation, upgrade existing designs or have TO-247 performance in a TO-220 outline.

These benefits make this design an extremely efficient and reliable device for use in a wide variety of applications.



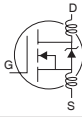
## Absolute Maximum Ratings

|                           | Parameter                                    | Max.                     | Units |
|---------------------------|--|--------------------------|-------|
| $I_D @ T_C = 25^\circ C$  | Continuous Drain Current, $V_{GS} @ 10V$     | 206 <sup>(6)</sup>       | A     |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$     | 145 <sup>(6)</sup>       |       |
| $I_{DM}$                  | Pulsed Drain Current <sup>(1)</sup>          | 650                      |       |
| $P_D @ T_C = 25^\circ C$  | Power Dissipation                            | 300                      | W     |
|                           | Linear Derating Factor                       | 2.0                      | W/°C  |
| $V_{GS}$                  | Gate-to-Source Voltage                       | $\pm 20$                 | V     |
| $E_{AS}$                  | Single Pulse Avalanche Energy <sup>(2)</sup> | 480                      | mJ    |
| $I_{AR}$                  | Avalanche Current <sup>(1)</sup>             | See Fig.12a, 12b, 14, 15 | A     |
| $E_{AR}$                  | Repetitive Avalanche Energy <sup>(1)</sup>   |                          | mJ    |
| dv/dt                     | Peak Diode Recovery dv/dt <sup>(3)</sup>     | 5.0                      | V/ns  |
| $T_J$                     | Operating Junction and                       | -40 to + 175             | °C    |
| $T_{STG}$                 | Storage Temperature Range                    | -55 to + 175             |       |
|                           | Soldering Temperature, for 10 seconds        | 300 (1.6mm from case )   |       |
|                           | Recommended clip force                       | 20                       | N     |

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International  
IR Rectifier

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

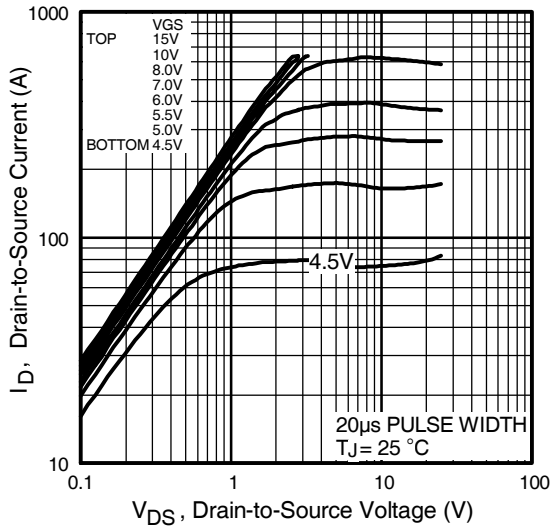
|                                      | Parameter                            | Min. | Typ.  | Max. | Units | Conditions   |
|--------------------------------------|--------------------------------------|------|-------|------|-------|--|
| V <sub>(BR)DSS</sub>                 | Drain-to-Source Breakdown Voltage    | 40   | —     | —    | V     | V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA   |
| ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub> | Breakdown Voltage Temp. Coefficient  | —    | 0.036 | —    | V/°C  | Reference to 25°C, I <sub>D</sub> = 1mA  |
| R <sub>DS(on)</sub>                  | Static Drain-to-Source On-Resistance | —    | —     | 3.7  | mΩ    | V <sub>GS</sub> = 10V, I <sub>D</sub> = 95A ④  |
| V <sub>GS(th)</sub>                  | Gate Threshold Voltage               | 2.0  | —     | 4.0  | V     | V <sub>DS</sub> = 10V, I <sub>D</sub> = 250μA  |
| g <sub>fs</sub>                      | Forward Transconductance             | 106  | —     | —    | S     | V <sub>DS</sub> = 25V, I <sub>D</sub> = 60A  |
| I <sub>DSS</sub>                     | Drain-to-Source Leakage Current      | —    | —     | 20   | μA    | V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V  |
|                                      |                                      | —    | —     | 250  |       | V <sub>DS</sub> = 32V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C                  |
| I <sub>GSS</sub>                     | Gate-to-Source Forward Leakage       | —    | —     | 200  | nA    | V <sub>GS</sub> = 20V  |
|                                      | Gate-to-Source Reverse Leakage       | —    | —     | -200 |       | V <sub>GS</sub> = -20V   |
| Q <sub>g</sub>                       | Total Gate Charge                    | —    | 160   | 200  | nC    | I <sub>D</sub> = 95A   |
| Q <sub>gs</sub>                      | Gate-to-Source Charge                | —    | 35    | —    |       | V <sub>DS</sub> = 32V  |
| Q <sub>gd</sub>                      | Gate-to-Drain ("Miller") Charge      | —    | 42    | 60   |       | V <sub>GS</sub> = 10V  |
| t <sub>d(on)</sub>                   | Turn-On Delay Time                   | —    | 17    | —    | ns    | V <sub>DD</sub> = 20V  |
| t <sub>r</sub>                       | Rise Time                            | —    | 140   | —    |       | I <sub>D</sub> = 95A   |
| t <sub>d(off)</sub>                  | Turn-Off Delay Time                  | —    | 72    | —    |       | R <sub>G</sub> = 2.5Ω  |
| t <sub>f</sub>                       | Fall Time                            | —    | 26    | —    |       | R <sub>D</sub> = 0.21Ω ④   |
| L <sub>D</sub>                       | Internal Drain Inductance            | —    | 2.0   | —    | nH    | Between lead,<br>6mm (0.25in.)<br>from package<br>and center of die contact          |
| L <sub>S</sub>                       | Internal Source Inductance           | —    | 5.0   | —    |       |  |
| C <sub>iss</sub>                     | Input Capacitance                    | —    | 7360  | —    | pF    | V <sub>GS</sub> = 0V   |
| C <sub>oss</sub>                     | Output Capacitance                   | —    | 1680  | —    |       | V <sub>DS</sub> = 25V  |
| C <sub>rss</sub>                     | Reverse Transfer Capacitance         | —    | 240   | —    |       | f = 1.0MHz, See Fig. 5   |
| C <sub>oss</sub>                     | Output Capacitance                   | —    | 6630  | —    |       | V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz                             |
| C <sub>oss</sub>                     | Output Capacitance                   | —    | 1490  | —    |       | V <sub>GS</sub> = 0V, V <sub>DS</sub> = 32V, f = 1.0MHz                              |
| C <sub>oss eff.</sub>                | Effective Output Capacitance ⑤       | —    | 1540  | —    |       | V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 32V                                    |

## Source-Drain Ratings and Characteristics

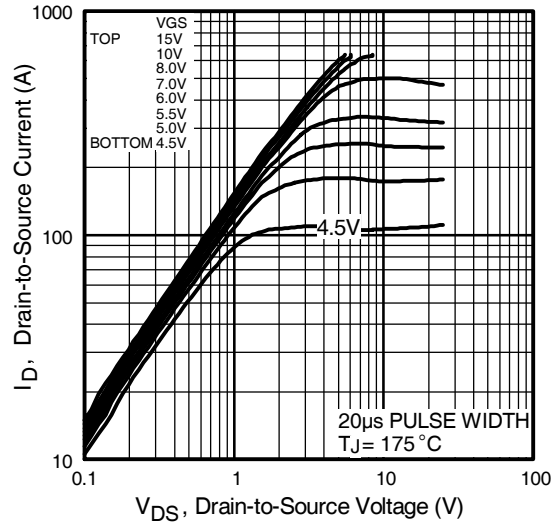
|                 | Parameter                                 | Min.   | Typ. | Max. | Units | Conditions  |
|-----------------|---|--|------|------|-------|---|
| I <sub>S</sub>  | Continuous Source Current<br>(Body Diode) | —  | —    | 206⑥ | A     | MOSFET symbol<br>showing the<br>integral reverse<br>p-n junction diode. |
| I <sub>SM</sub> | Pulsed Source Current<br>(Body Diode) ①   | —  | —    | 650  |       |   |
| V <sub>SD</sub> | Diode Forward Voltage                     | —  | —    | 1.3  | V     | T <sub>J</sub> = 25°C, I <sub>S</sub> = 95A, V <sub>GS</sub> = 0V ④     |
| t <sub>rr</sub> | Reverse Recovery Time                     | —  | 71   | 110  | ns    | T <sub>J</sub> = 25°C, I <sub>F</sub> = 95A                             |
| Q <sub>rr</sub> | Reverse Recovery Charge                   | —  | 180  | 270  | nC    | di/dt = 100A/μs ④   |
| t <sub>on</sub> | Forward Turn-On Time                      | Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> ) |      |      |       |   |

## Thermal Resistance

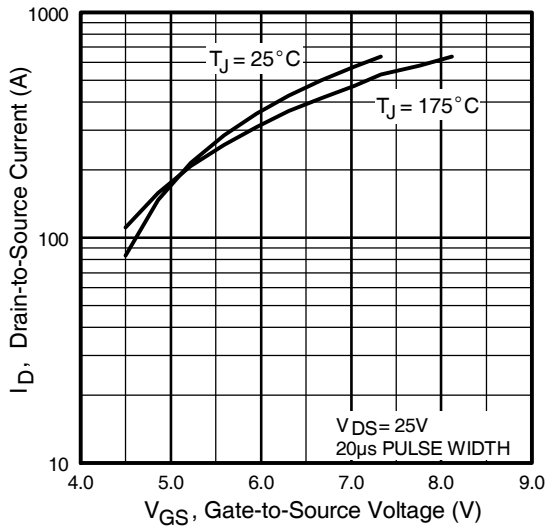
|                  | Parameter                           | Typ. | Max. | Units |
|------------------|-------------------------------------|------|------|-------|
| R <sub>θJC</sub> | Junction-to-Case                    | —    | 0.50 | °C/W  |
| R <sub>θCS</sub> | Case-to-Sink, Flat, Greased Surface | 0.5  | —    |       |
| R <sub>θJA</sub> | Junction-to-Ambient                 | —    | 58   |       |



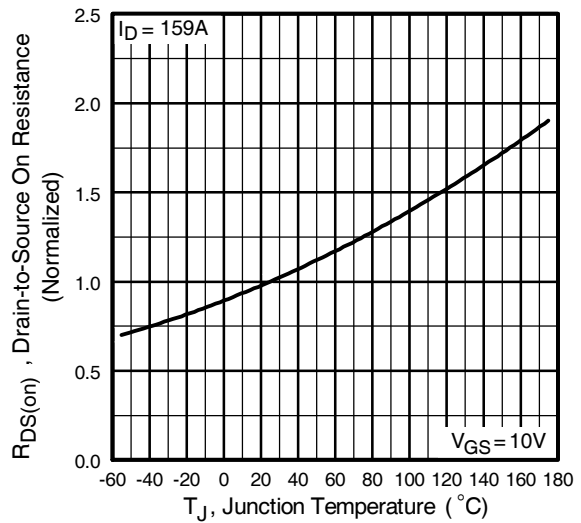
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



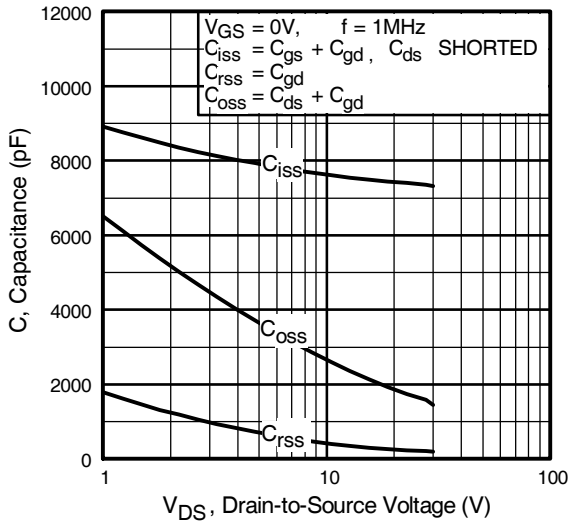
**Fig 3.** Typical Transfer Characteristics



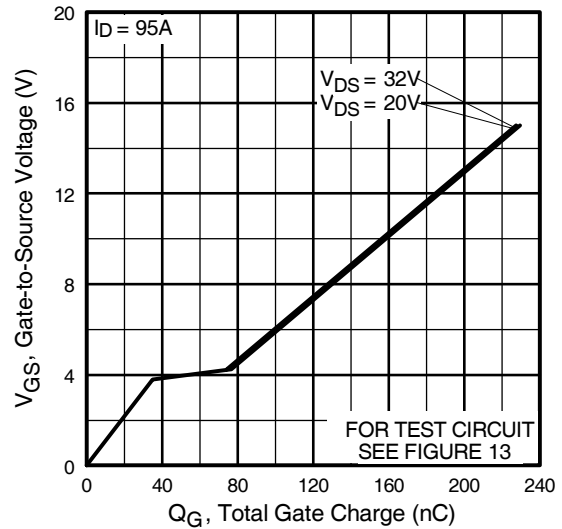
**Fig 4.** Normalized On-Resistance Vs. Temperature

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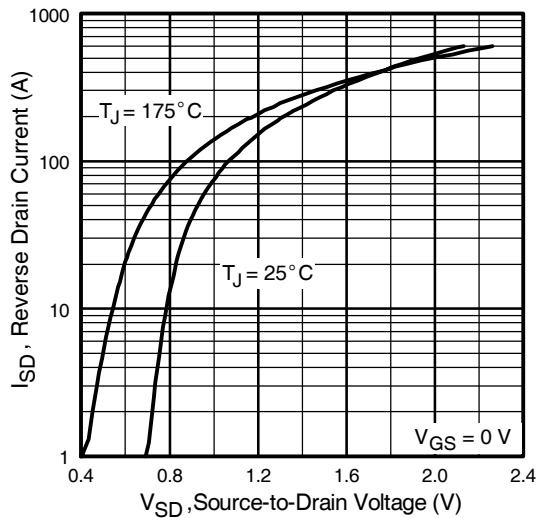
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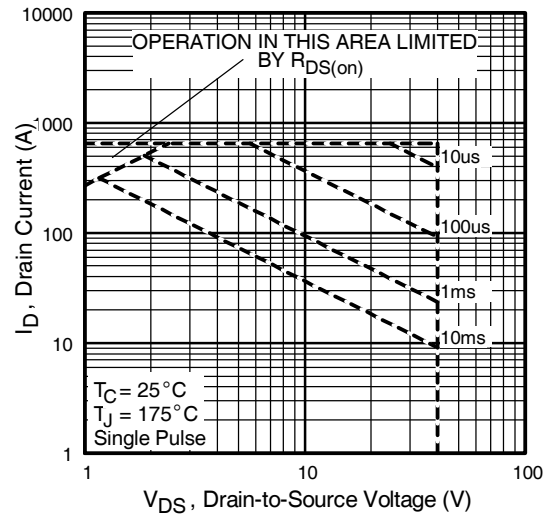
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



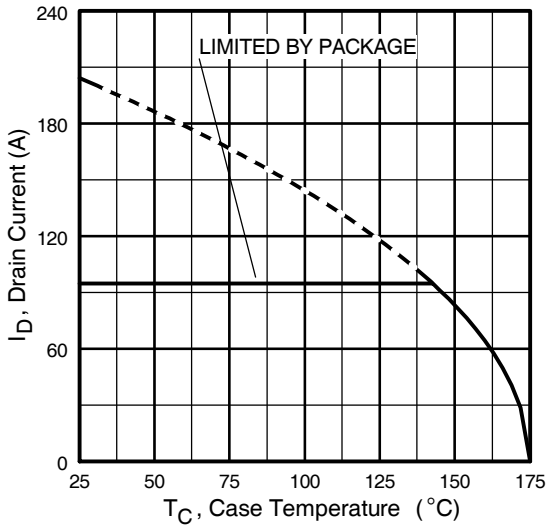
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



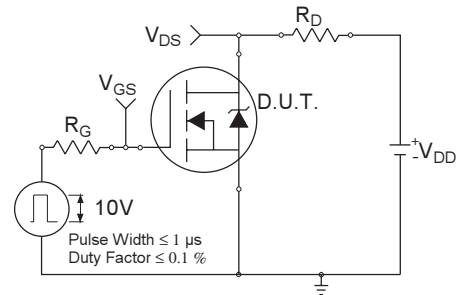
**Fig 7.** Typical Source-Drain Diode Forward Voltage



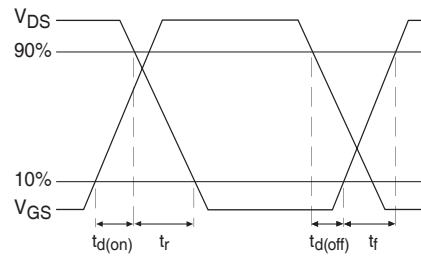
**Fig 8.** Maximum Safe Operating Area



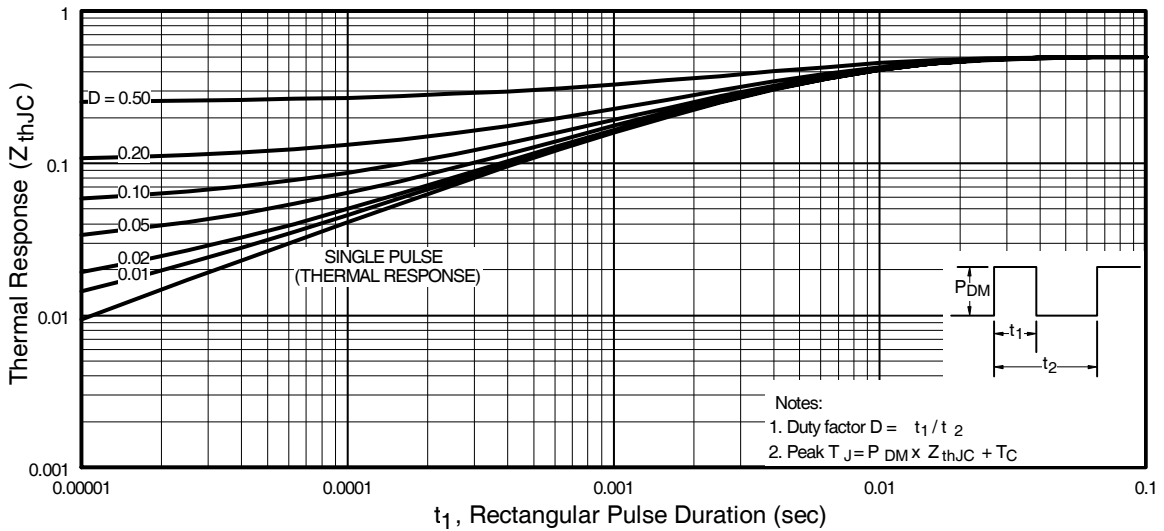
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



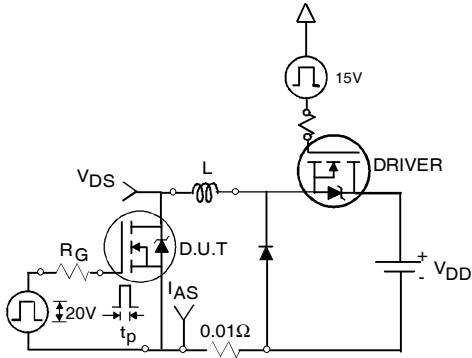
**Fig 10b.** Switching Time Waveforms



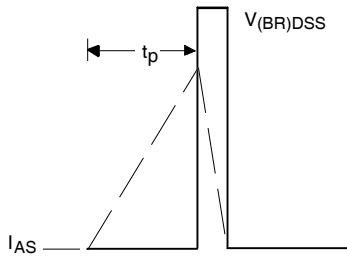
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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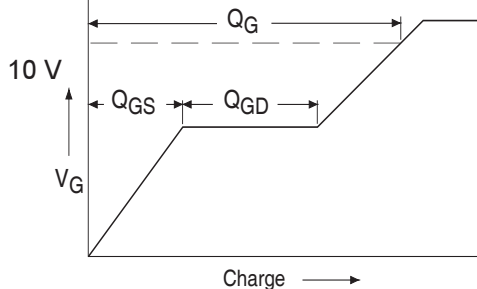
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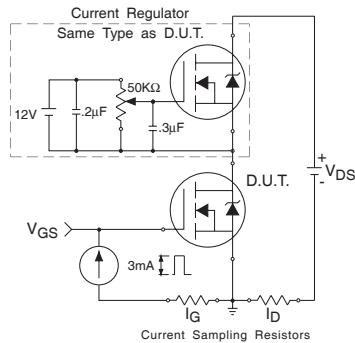
**Fig 12a.** Unclamped Inductive Test Circuit



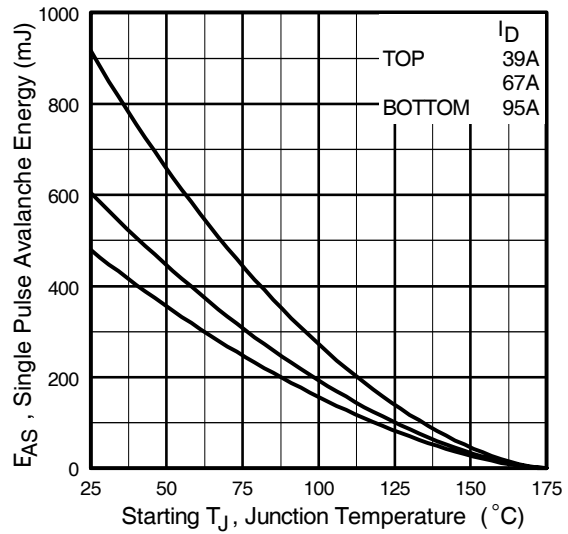
**Fig 12b.** Unclamped Inductive Waveforms



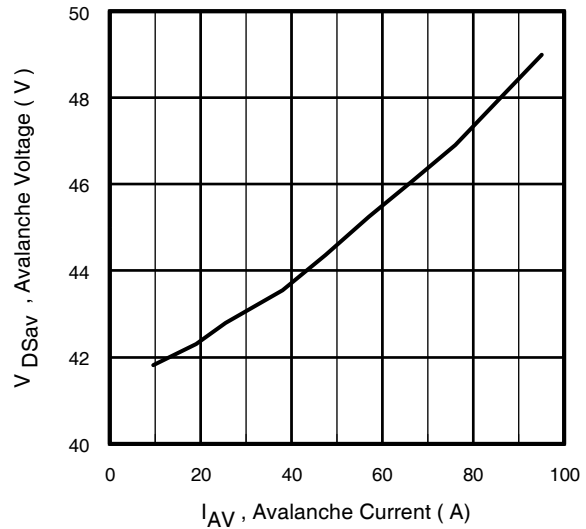
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 12d.** Typical Drain-to-Source Voltage Vs. Avalanche Current

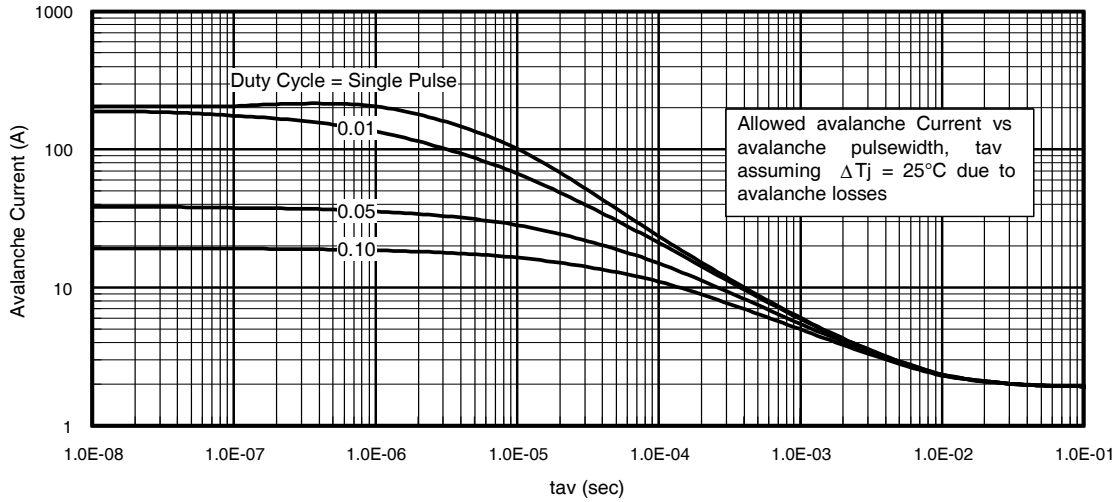


Fig 14. Typical Avalanche Current Vs.Pulsewidth

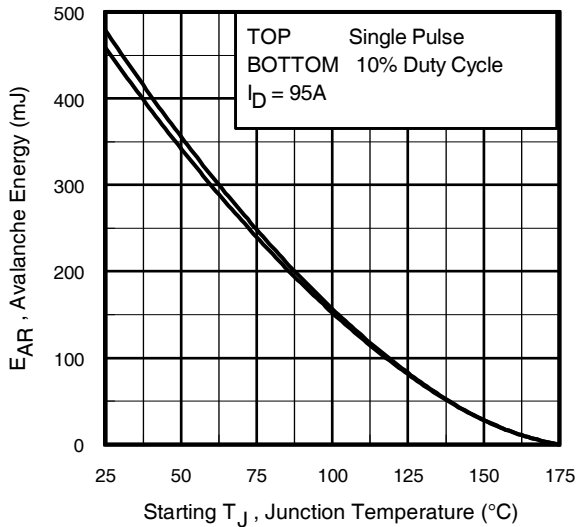


Fig 15. Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

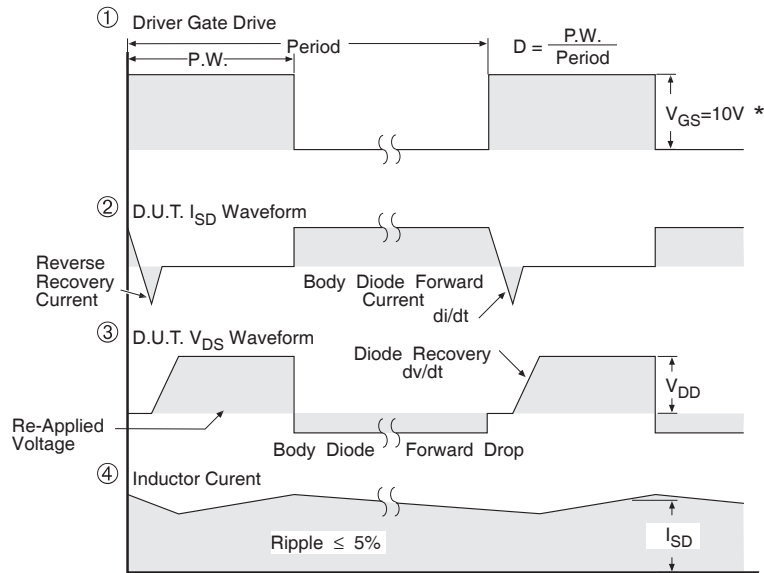
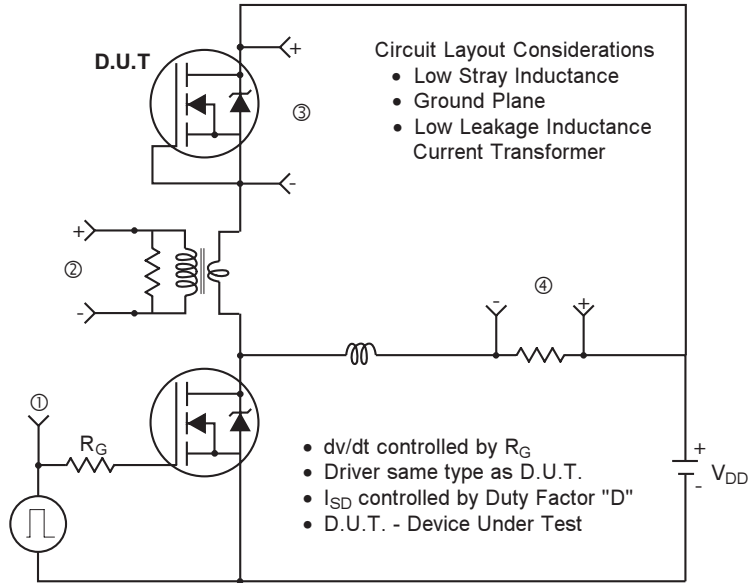
1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = \frac{1}{2} ( 1.3 \cdot BV \cdot I_{av} ) = \frac{\Delta T}{Z_{thJC}}$$

$$I_{av} = \frac{2\Delta T}{[1.3 \cdot BV \cdot Z_{th}]}$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

## Peak Diode Recovery dv/dt Test Circuit

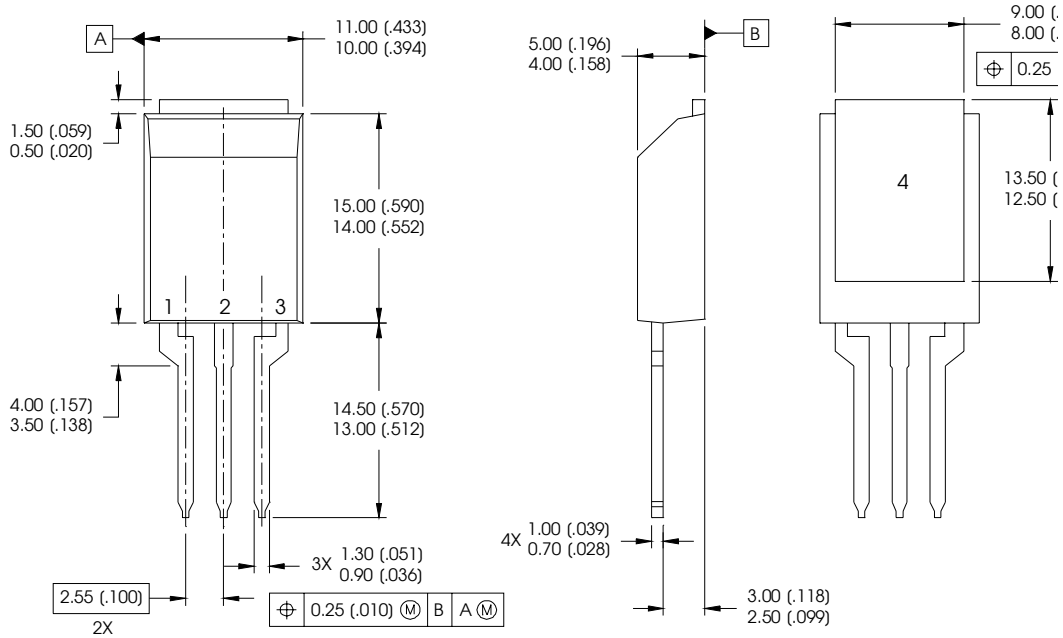


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 16.** For N-Channel HEXFET® Power MOSFETs



## Super-220™ ( TO-273AA ) Package Outline



**NOTES:**

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. OUTLINE CONFORMS TO JEDEC OUTLINE TO-273AA.

**LEAD ASSIGNMENTS**

| <u>MOSFET</u> | <u>IGBT</u>   |
|---------------|---------------|
| 1 – GATE      | 1 – GATE      |
| 2 – DRAIN     | 2 – COLLECTOR |
| 3 – SOURCE    | 3 – EMITTER   |
| 4 – DRAIN     | 4 – COLLECTOR |

**Notes:**

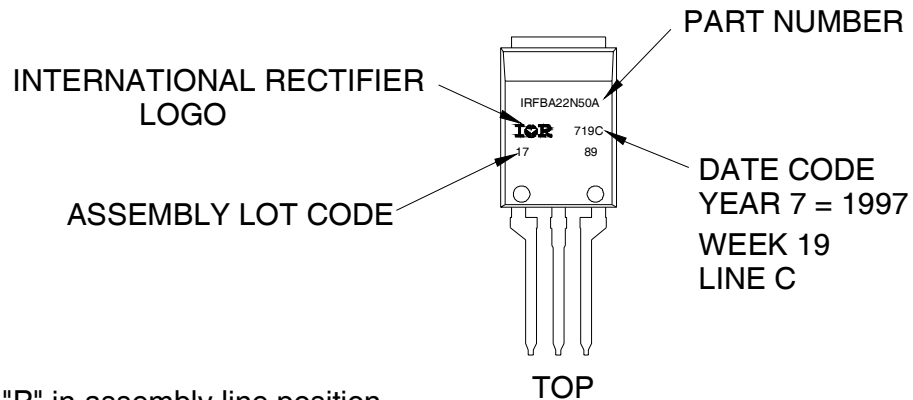
- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.11\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 95\text{A}$ .
- ③  $I_{SD} \leq 95\text{A}$ ,  $di/dt \leq 150\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ . Refer to AN-1001
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 95A.

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## Super-220 (TO-273AA) Part Marking Information

EXAMPLE: THIS IS AN IRFBA22N50A WITH  
ASSEMBLY LOT CODE 1789  
ASSEMBLED ON WW 19, 1997  
IN THE ASSEMBLY LINE "C"



Note: "P" in assembly line position  
indicates "Lead-Free"

Super-220™ not recommended for surface mount application

### Notes:

1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

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